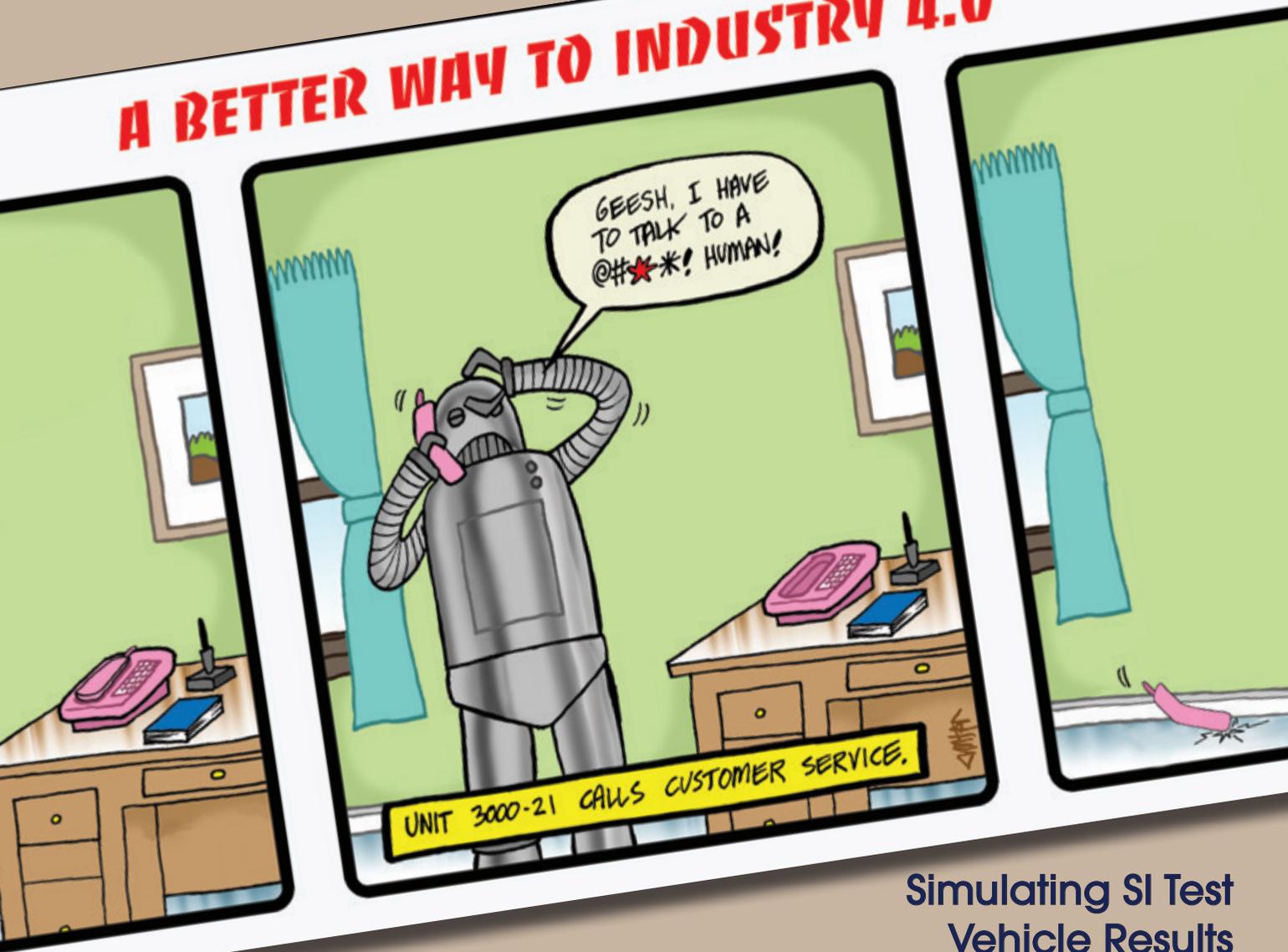


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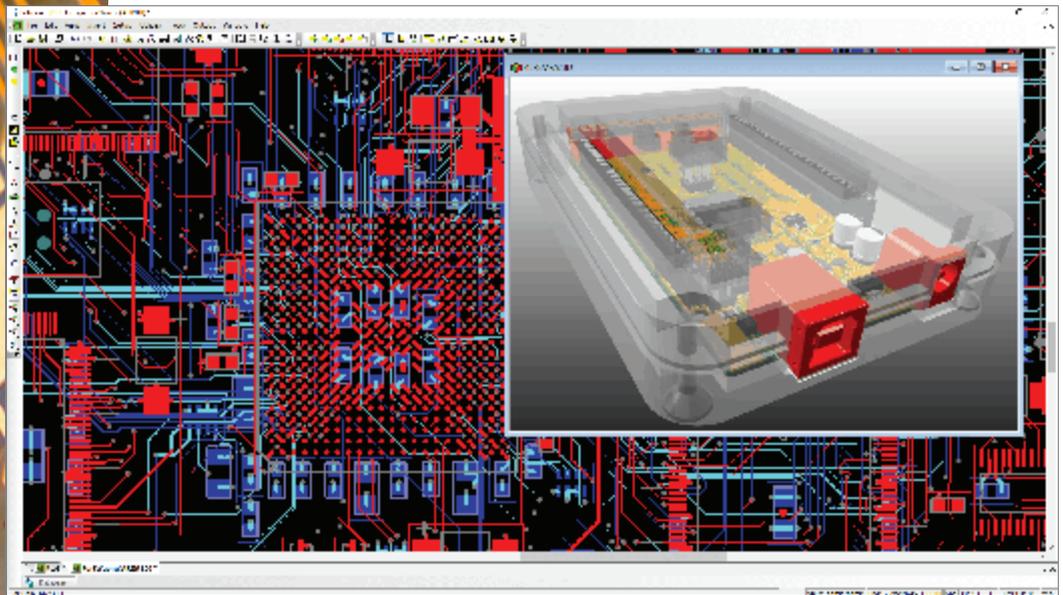
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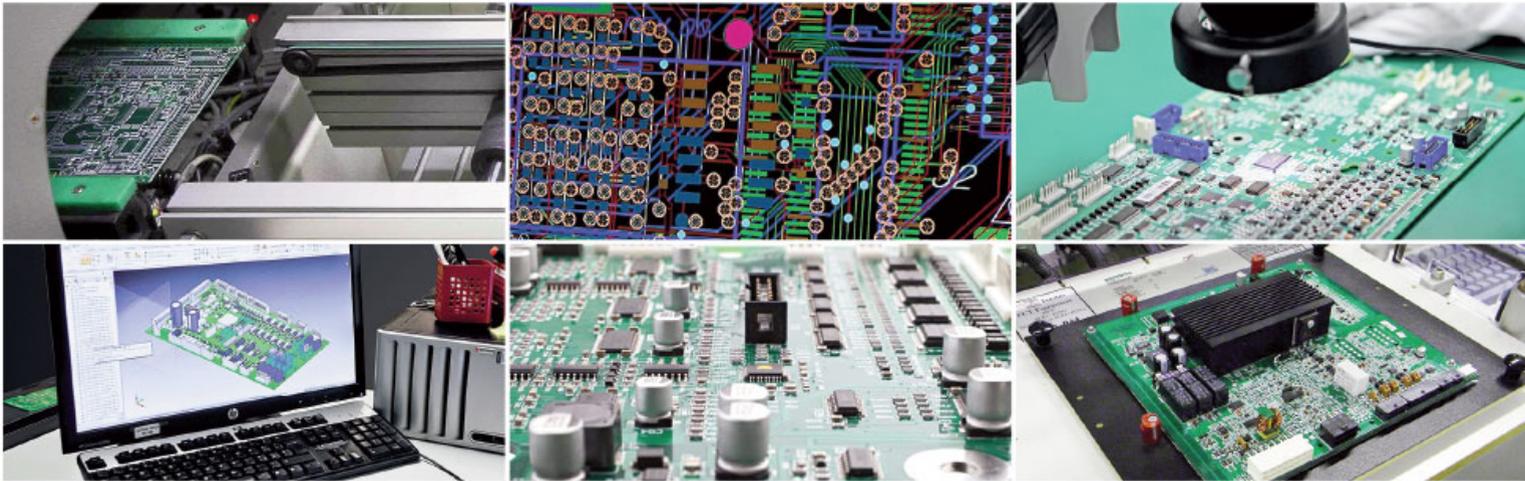


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## XJTAG® Boundary Scan Helps Industrial Technology Leader Test the Untestable

**“Lack of access to I/O pins can challenge the test coverage achievable using probes alone. Eutron chose XJTAG boundary scan to raise coverage to the level required. The intuitive user interface lets engineers test parts of their boards that can not be reached any other way, effectively testing the untestable.”**

Eutron is an electronic manufacturing services and solutions (EMS<sup>2</sup>) company headquartered outside Bergamo, northern Italy. With extensive competencies for building the “intelligent world”, the organisation’s technical skills include hardware and software design, and state-of-the-art manufacturing. All assemblies must be built and tested to high standards, for deployment in challenging environments such as smart factories, smart cities, and smart infrastructure.

Hardware designers everywhere know that pushing the limits of functionality can often compromise testability. Component packages such as BGAs, flip-chip CSPs, and LGAs have I/O pins that are difficult or impossible to access with test probes, while space for test points is always needed either for other components or to be removed to save space. Components that contain internal boundary scan circuitry, however, can be tested without direct probing. The XJTAG boundary scan test system can also control the I/O pins of non-JTAG devices that are on the same nets as devices connected to the scan chain. In this way, XJTAG can test connections that are untestable using other techniques.

Eutron has invested in the XJTAG system for this very reason, as Test Engineer Luca Gherardi explains, “We are using XJTAG to test processing modules that contain a combination of DDR and flash memory chips, FPGAs, logic devices, various encoders, and off-board interfaces such as RS-232 and CAN transceivers,” he says. “There

are often connections that cannot be probed. XJTAG can reach them and helps us test a high proportion of each board quickly and efficiently.”

Engineers can write tests easily in XJTAG’s system using high-level instructions, without spending time learning the finer points of boundary scan such as how to construct low-level test vectors. And with features such as the automatically

generated Connection Test and device-centric library scripts, XJTAG handles any board design changes during development efficiently, and enables custom tests to be reused in future projects.

The XJTAG user interface is clear and intuitive, which helps maximise the benefits of boundary scan testing. “The user interface makes an instant impression and is one of the most powerful aspects of XJTAG,” agrees Luca Gherardi.

“We can debug to see exactly what the tests are doing, and the tests themselves rapidly diagnose opens, shorts and stuck faults. The Layout and Schematic Viewers help quickly troubleshoot any failed boards.”

In addition to testing inaccessible connections, XJTAG can test a high percentage of connections extremely quickly thereby enabling simpler in-circuit test routines and lower-cost fixtures. In addition, XJTAG provides test coverage analysis for each board, and XJTAG DFT Assistant software extensions/plugins are available for popular EDA tools including Altium Designer, OrCAD Capture, Mentor Xpedition and PADS, and Zuken CR-8000 to help users analyse and increase test coverage before the first prototype is produced.

Luca Gherardi summarises, “The XJTAG system’s configurability, clarity and ease of use help us deliver the extremely high quality and reliability our customers need.”

## opinion



**Luca Gherardi**  
Test Engineer  
Eutron

“There are often connections that cannot be probed. XJTAG can reach them and helps us test a high proportion of each board quickly and efficiently.”

“The user interface makes an instant impression and is one of the most powerful aspects of XJTAG. We can debug to see exactly what the tests are doing, and the tests themselves rapidly diagnose opens, shorts and stuck faults. The Layout and Schematic Viewers help quickly troubleshoot any failed boards.”

“XJTAG’s clarity and ease of use helps us deliver the extremely high quality and reliability our customers need.”

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<b>Customers</b>	Diverse range of market sectors including automation, automotive, energy, instrumentation, telecom...
<b>Locations</b>	Pradalunga, Italy & Kunshan, China
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FIRST PERSON

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by NILESH BADWE, KEVIN BYRD, OU JIN and PUBUDU GOONETILLEKE



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**Stencil Design and Void Reduction**  
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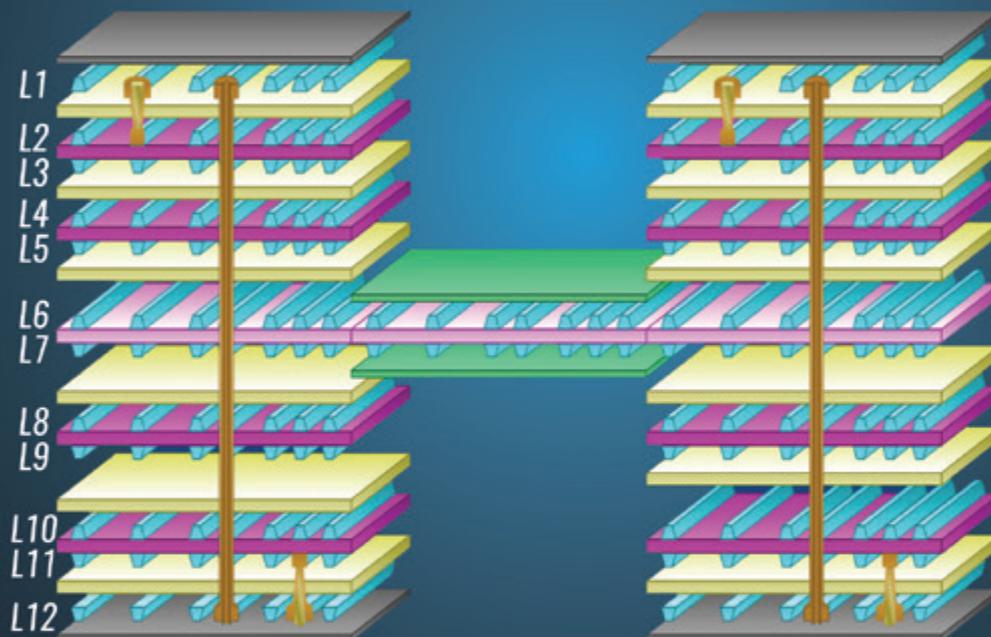


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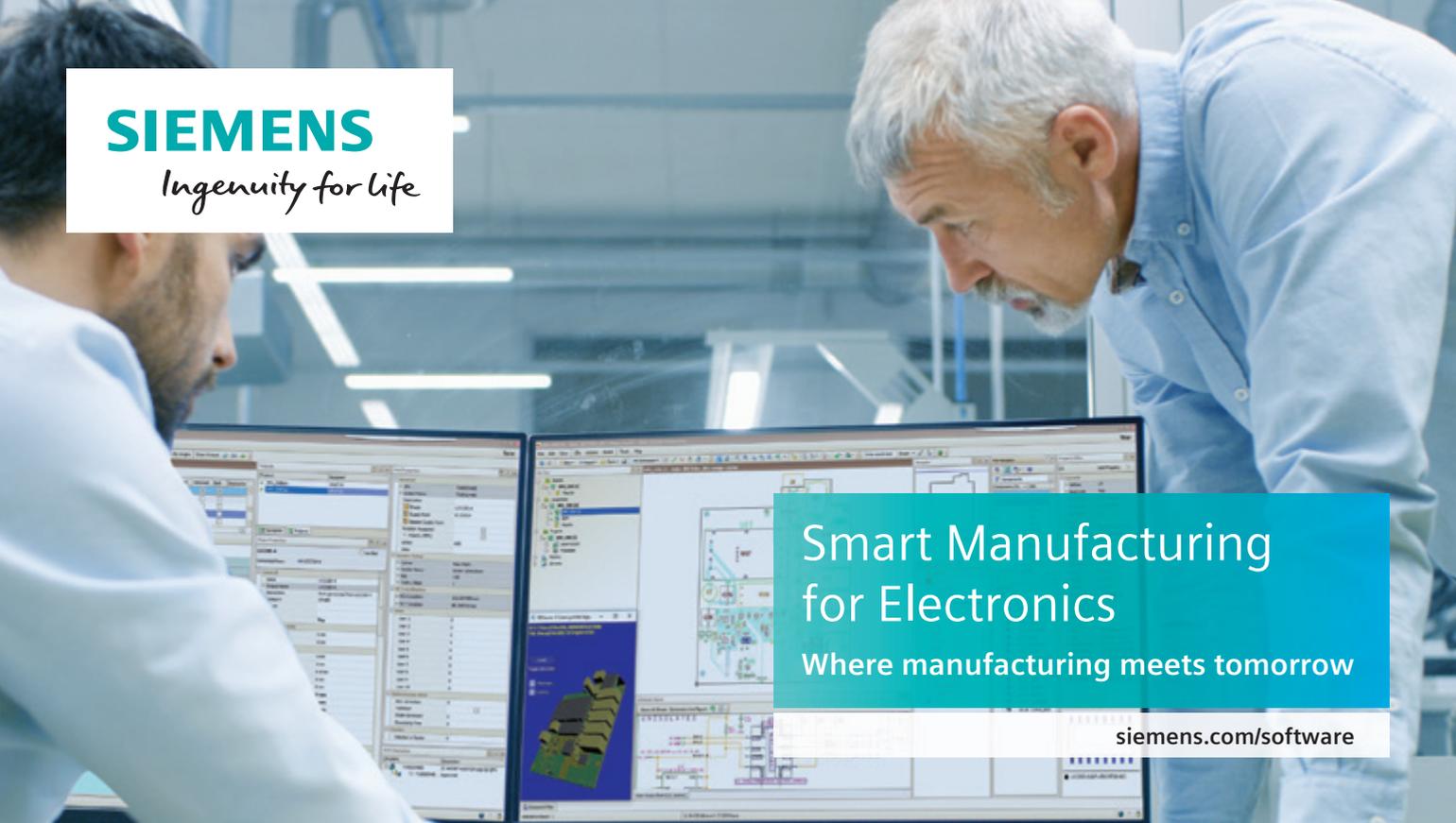


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# Designing a New Start

**T**HE Designers Council is dead. Long live the Designers Council!

As the calendar turned to January, IPC and the entity formerly known as the Designers Council amicably parted ways.

The event, which happened quietly after months of discussions, ended a long and productive chapter in the printed circuit design industry history.

As detailed in our 25-year retrospective on the organization in 2017 (<https://pcdandf.com/pcdesign/index.php/editorial/menu-features/12246-designer-council-1712>), the Designers Council began as an independent grassroots movement in locales across the US and Europe. Originally a confederacy of like-minded individuals who somehow found the energy and time to commit to bringing their colleagues together, it quickly spun into a top-down organization under the auspices of IPC.

Dieter Bergman, my late colleague at IPC and a former designer himself, was at the forefront of that movement. Bergman knew firsthand the need for designers to gain access to industry standards and, more importantly, the knowledge behind them, in order to keep up with the demands of customers and management. Back then, training was generally provided by older, experienced mentors in the same company. As conferences such as PCB West emerged, education became somewhat more structured and formalized, but there remained a need for on-demand training and at the point of use.

Bergman, along with Gary Ferrari (who eventually became executive director of the Designers Council) and dozens of others, developed a formal curriculum based on the IPC design specs and over the course of many, many meetings – I know, as I was present to record the minutes, make the copies, get the coffee, and basically supply anything short of back massages – shaped those documents and other supporting sources into a training class and certification exam. Today, some 6,000 or so certifications later, the CID (certified interconnect designer) designation is recognized worldwide.

For most of its 25 years, the Designers Council operated almost as a standalone entity, alongside and contributing to IPC, but with its own management structure. The latest development has IPC making the organization more like its other committees. The new program, called IPC Design, is said to encompass many different aspects of the programs IPC has. Teresa Rowe, senior director, assembly and standards technology, tells me IPC Drive will have a new advisory group made up of representatives from major geographical

regions and headed by Karen McConnell of Northrop Grumman. The certification program will remain as is for now, IPC added.

Meanwhile, the former executive board of the Designers Council is launching its own organization, called the Printed Circuit Engineering Association (PCEA). In a statement, the 10 founding directors said the new association plans to support IPC and its efforts, including in the standards arena. But it will work with other electronics industry organizations and standards bodies as well. (See the full letter at [pcdandf.com](https://pcdandf.com) under the PCEA section.)

For its part, IPC wants to continue a local chapter model, but plans to bifurcate the effort by establishing professional and student chapters. The former, IPC says, will serve to support and mentor the latter, as part of IPC's larger effort to prospect potential STEM students for future employment in electronics design and manufacturing.

It's a good goal. I am eager to see, however, how the new PCEA works out, now that it is free of any constraints of IPC. Trade associations do a lot of good work, but as they gain in size and develop new goals and strategies, it sometimes works against them. My sense in talking to many of the former directors of the Designers Council is the time had come for both groups to start anew. After 25 years, designers have taken their rightful place as essential cogs in the product development chain. Bergman's vision has been realized, and it's time for the next chapter to begin.



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@mikebuetow

P.S. See us this month at IPC Apex Expo, booth #2748. And check out PCB2Day, our popular training series, with separate workshops on design engineering and assembly coming to Austin, TX, in late March. Visit [pcb2day.com](https://pcb2day.com) for details.



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## PCDF People

Elmatica named **Joseph Milsom** IT developer.

MFLEX named **Dale Wesselmann** business development manager.

Uyemura promoted **Patrick Valentine**, Ph.D., to director of technology. He joined Uyemura in 2015 to lead the company's continuous improvement program and has held technical and executive roles in the PCB and chip industries since 1980. He is a Six Sigma Master Black Belt.

## PCDF Briefs

**AT&S** will invest €30 million (\$33.4 million) over the next two fiscal years to upgrade its site in Ansan, South Korea.

**Avnet** is launching a new partner program designed to provide developers with a place to build complete IoT solutions, enabling them to scale their business in a quick and cost-effective manner.

India's government is considering a proposal to sweeten an export incentive scheme for smartphone manufacturers by offering 6% duty credit scrips, replacing the current 4% scrip, as part of a target to increase smartphone exports to \$110 billion by 2025 from \$3 billion now, per reports.

**Novoset** signed a licensing agreement with **Shin-Etsu Chemical** for the manufacturing of new hydrocarbon resins for 5G-related electronics, aerospace and automotive applications.

Major Chinese PCB fabricators are reportedly speeding up capacity expansions seeking to better meet fast-growing demand for applications to 5G, terminal devices and automotive electronics in China.

**PCB Connect** opened a North American headquarters in Sharon, MA, the PCB supplier's 16th global location.

**PCB Scrap Recovery**, a Mexican engineering firm, has developed and patented a circuit board processing system marked by low resource use and simplicity.

**Recom Power** is launching digital models for its entire product catalog in collaboration with **SnapEDA**.

**Samsung Electronics** reportedly will increase PCB orders to **DAP** and **Korea Circuit** after the withdrawal of **Semco** from the HDI PCB market.

**Tramonto Circuits** reported on-time delivery in 2019 increased to 99.14%.

## UP Media Group Announces PCB2Day Workshops on PCB Design, SMT

**ATLANTA, GA** – UP Media Group announced dates for its popular PCB2Day workshop series for spring 2020.

Two-day workshops on surface mount technology and design and engineering of printed circuit boards will take place in Austin, TX, in March.

Design Essentials for PCB Engineers is a two-day workshop for design engineers covering fine-pitch BGA design, DfM, component selection and placement, routing, and impedance control. Presenter Susy Webb is a senior PCB designer with 40 years of experience in coastal and oceanographic oil exploration and monitoring equipment, point-to-point microwave network systems, and CPCI and ATX computer motherboards. She is a regular speaker at PCB WEST, IPC Apex Expo and international design conferences and consults for individual companies and Designers Council chapters in several countries.

SMT Assembly Boot Camp is a two-day practical overview combining lecture, videos and discussion of the different processes, equipment and materials used in through-hole and SMT. The presenter is Phil Zarrow, a 35-year veteran with extensive hands-on experience with setup and troubleshooting through-hole and SMT processes throughout the world at OEMs and contract assemblers.

SMT Assembly Boot Camp will be held March 24-25 in Austin, and Design Essentials for PCB Engineers will be held March 26-27 in Austin. For more information or to register visit [pcb2day.com](http://pcb2day.com).

PCD&F and CIRCUITS ASSEMBLY are media partners for the event. Design Essentials for PCB Engineers event is sponsored by EMA Design Automation, and SMT Assembly Boot Camp is sponsored by FHP Reps. – MB

## Hitachi Chemical to End Most Laminate Manufacturing

**TOKYO** – Hitachi Chemical will cease manufacturing of several laminate products by the end of 2022, even as the company prepares for acquisition by an entity backed by Showa Denko K.K.

Hitachi Chemical will end production of CEM-3, some FR-4 products, and mass lam products by September 2022, according to reports. The company will continue to manufacture high-end materials for IC substrates and high-frequency materials, sources told PCD&F.

The decision to exit lower-end materials production appears to be driven by lower demand and pricing pressure tied to competition from lower-cost regions. Also, the current margins do not support investment in new manufacturing equipment, sources told PCD&F.

On Dec. 18, the board of directors of Hitachi Chemical issued a statement in support of a tender offer by HC Holdings K.K., a wholly owned subsidiary of Showa Denko. That deal is expected to close in 2022. It has been suggested Hitachi is jettisoning the lower-end materials to beef up its bottom line prior to the acquisition. – MB

## SEMCO to Shut Down HDI Ops in China

**JIANGSU, CHINA** – Samsung Electro-Mechanics plans to shut down its HDI PCB manufacturing facility here as a result of poor profits, according to reports.

The site will cease production and sales, and the company will sell its assets there. The news comes after Samsung decided to stop smartphone manufacturing operations in China as well.

Samsung-EM is the second major fabricator in recent months to announce cessa-

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**Unimicron Technology** and **Nan Ya PCB** are likely to become top-choice partners to provide advanced ABF substrates to Chinese microprocessor makers, according to industry sources.

**Ventec** increased its PTFE laminate manufacturing capabilities following a strategic investment in a new state-of-the-art high-temperature press and layup/breakdown line at its Suzhou manufacturing plant.

## CA People

Circuit-Tech promoted **Anastassia Ramesur** to team lead business development.



Intervala named **Jon Saunders** vice president of operations, Hudson plant. He has 25 years' experience in electronics assembly, including Sanmina, Altron and most recently Varitron.

**Phil Zarrow** will present a two-day SMT Assembly Boot Camp, a practical workshop on processes and materials used in through-hole and SMT, in Austin, TX, on Mar. 24–25.

Universal Instruments promoted **Kevin Clue** to general manager, North American field operations.



Yamaha appointed **David Suh** product manager, Inspection Products. He has over 20 years' experience in electronics assembly in inspection, test engineering, field service, support, and training.

## CA Briefs

**BYD Electronics** is expected to replace **Guangda** as the exclusive assembly supplier for **Apple's** iPod Touch.

**EMS Components Assembly** signed a P500-million loan agreement with **Development Bank of the Philippines** to finance expansion.

**Foxconn** called untrue a report in an Indian newspaper that it has canceled a plan to invest \$5 billion in India due to an "internal dispute" with **Apple**.

**Foxconn** reportedly is gearing up to promote its AGV (automated guided vehicle) solutions in Taiwan through its affiliated **Asia Pacific Telecom (APT)** and **FHnet** to help manufacturers "smartize" their operations.

**HP** rejected **Xerox's** latest terms on the grounds that the offer still undervalues

tion of HDI production. LG Innotek also said it would stop producing HDI boards later this year. – CD

## No More Silica: Startup Believes It Has Better Answer to Keeping Boards Dry

**TAMPA, FL** – Moisture is the bane of the circuit board, and millions of dollars are spent on packaging materials each year to keep parts dry. But while components can be packaged and handled in trays, standard practice remains to treat each PCB as an individual unit, storing them with silica gel desiccant bags to soak up unwanted moisture.

Dan Jenkins, CEO of startup company Steel Camel, says it's past time to move on from inexpensive and relatively ineffective silica gel bags. Industry standards, however, must be brought up to date, he adds.

"Industry specifications are quite confusing and complicated, because the military spec MIL-D-3464 is way out of date and the test devices don't exist to the public or even branches of military," notes Jenkins. "And while the far majority of suppliers of desiccant beads claim they pass the mil spec, they cannot prove they meet it and have never submitted to the military for qualification. Military equipment manufacturers are only requiring manufacturers to meet the spec, so everyone is using a silica gel desiccant which does not work that well, and is most likely not qualified under MIL-D-3464."

Steel Camel's patented technology relies on a water-absorbent packet made of sheets of a cotton fabric through which moisture can penetrate. Once it does, the water is absorbed by a sodium poly-2-propenoate (sodium salt) compound.

A company video ([youtube.com/watch?v=kli3OMrFUD4](https://www.youtube.com/watch?v=kli3OMrFUD4)) tells the story: The introduction of the novel desiccant turns 8oz. of water into a solid block in about 45 sec.

Common silica gel desiccant bags cost 25 to 30 cents in the US and eight to 12 cents in China, Jenkins says. Because the quality of the Chinese-made bags can be poor, some US companies will buy silica gel bags in the US and ship them to China in 55-gal. drums. A similar size bag of Steel Camel is 10 to 15 times the cost, Jenkins allows. "We desiccate much, much more volume of air, however, and we do it more effectively!"

Indeed, in testing performed by Channelview, TX-based Standard Testing Laboratories, a report from which was shared with PCD&F/CIRCUITS ASSEMBLY, the novel desiccant performed far superior to silica gel.

In STL's tests, 10 g each of silica gel granules and the novel desiccant were placed in separate beakers and titrated with water until the first indication of free water was observed. Silica gel showed visual free water after 13ml of added water, while the novel desiccant did not have free water even after 2000ml of water was added. In a separate test of condensate formation using sealed one-gallon jars containing 10g of the respective desiccants and 20ml of water, the jars were temperature-cycled from 40° to 75°F on a daily basis for a week. The silica gel granules showed condensate formation each day; the novel desiccant showed no condensate formation at all.

The *de facto* standard practice at many companies is to individually wrap each board with a desiccant bag and humidity card. The bags are then vacuumed-sealed, which, Jenkins points out, can trap in moist air. Steel Camel's product needs air to desiccate, thus eliminating tight shrink-wrap or vacuum packing.

Steel Camel's bag has a simple seal, which eliminates the vacuum step. It also accommodates more boards per packaging, thus improving economies-of-scale and reducing packaging waste.

Another difference between traditional silica gel bead and Steel Camel is the indicator. The Silica Gel is rigid; therefore, a color indicator is used to help determine when to change. The Steel Camel bags expands from a flat pillow to a blown-up pillow, so visual and feel inspection techniques are used during inspection to determine when to change.

One multinational fabricator is testing Steel Camel's technology by putting 15 to 20 boards in a bundle, loosely wrapped, and adding the novel absorbent. Jenkins is

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**IMET Electronics** merged with **TJM Electronics**.

**Intervala** has acquired **Varitron's** EMS operations in Hudson, NH.

**IPC** signaled its approval of the US House's vote to ratify the USMCA trade agreement and advocated for the Senate to do the same.

**Jabil Circuit India** has leased 60,000 sq. ft. of light manufacturing and assembling facility at an industrial park in Pune for its plastic and metal parts manufacturing division, Jabil Green Point.

**Japan Display** is discussing the sale of its main smartphone screen factory to **Apple** and **Sharp** for as much as \$820 million, the Nikkei business daily reported.

**Katek** will take over SMT production of the **Huf Group**.

**Kitron** won \$8.7 million in orders for off-shore wind-related electronics.

**Libra Industries** and **Gemcity Engineering & Manufacturing** have merged and will operate as Libra Industries going forward.

For **Mirtec**, 2019 was the most successful year in its corporate history and the ninth consecutive year of record sales revenue for the North America division.

**Nordson Select** appointed **EMC3 Group** sales representative in Florida.

**Pillarhouse** appointed **EAP** distributor in Florida.

**Pine Electronics** purchased a **Parmi** Xceed AOI.

**Quanta**, **Pegatron**, **Wistron** and **Flex** have begun crossing manufacturing AR glasses, and Foxconn has established a department for developing smart hardware, according to reports.

**Quester Tangent** installed a **Universal Instruments** FuzionXC2-37 surface mount platform in its Saanichton, BC, manufacturing facility.

The Tamil Nadu government is planning to develop four electronics manufacturing clusters in Chennai, Tiruvallur, Hosur and Kancheepuram by 2023.

**Voxx Electronics**, a car electronics manufacturer, has acquired all the inventory, patents and trademarks of **Rosen Electronics**.

**Wistron's** board has approved up to \$300 million in spending to set up and outfit a new wholly owned subsidiary in Vietnam.

actively looking for additional companies to conduct comparison tests; contact him at [djenkins@steelcamel.com](mailto:djenkins@steelcamel.com).

## Purchase Price for AsteelFlash Set at \$450M

**PARIS** – Following a vote by AsteelFlash's shareholders, the investment group behind Universal Scientific Industrial will pay \$450 million in cash as stock to acquire AsteelFlash.

Sun Moonlight Investment Control agreed to the terms in mid-December. The pending deal was first reported by CIRCUITS ASSEMBLY in December.

Under terms of the deal, 89.6% of the payment will be in cash, and the remainder in private company Huanxu shares. Following the acquisition, which is expected to close in the third quarter of 2020, AsteelFlash will become a subsidiary of USI, which also goes by the Chinese name of Huanxu Electronics. AsteelFlash's existing operations management team will be retained, according to public reports.

The deal is subject to approval by the governments of China, the US and the European Union.

Sun Moonlight is a major shareholder of USI/Huanxu Electronics. The two companies will be merged following the transaction, with AsteelFlash handling smaller runs and USI performing the volume builds.

AsteelFlash has 17 production sites in 10 countries, including France, Germany, the UK, Tunisia, China, Taiwan, Czech Republic, Poland, Mexico and the US. It had sales of about \$1 billion last year, according to the CIRCUITS ASSEMBLY EMS Top 50, and profits of \$70 million to \$80 million.

USI has plants in Taiwan, Mexico, China, Poland, and a joint venture in Brazil. – *MB*

## Ametek's Ride on Reading About to End

**BERWYN, PA** – Ametek is selling Reading Alloys to Kymera International for \$250 million, according to reports.

Reading Alloys makes alloys and specialty materials for the aerospace, defense and industrial markets. Ametek acquired the company in 2008. Reading Alloys' sales have doubled since then to some \$160 million. Reading employs about 120 people.

Kymera is a specialty materials company based in Research Triangle Park, NC. The all-cash deal is expected to close this quarter. – *CD*

## US Congress to Approve Funds For R&D on Pb-Free Electronics

**BANNOCKBURN, IL** – The US House and Senate in December approved a defense spending bill that includes \$5 million for research and development on the issues surrounding Pb-free electronics in mission-critical applications.

The bill and the specific funding is supported by IPC, which advocated for its passage and believe it will save the defense industry millions down the road.

"The migration of the commercial industry to Pb-free electronics has introduced technical and supply-chain concerns in the aerospace, defense and high-performance sectors that can only be addressed through greater, more focused public-private R&D," said Chris Mitchell, IPC vice president of global government relations. "The funds in this bill will help support the much-needed collective effort and help ensure mission-critical systems have full access to cutting-edge electronics from a robust global supply chain."

IPC and its partners believe a five-year \$40 million investment in a public-private R&D program would yield more than \$100 million in US defense savings per year and improve military readiness and overall innovation. – *CD*



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## Sumitronics Manufacturing Launches Cambodian Ops

**POIPET CITY, CAMBODIA** – Sumitronics Manufacturing (Cambodia) launched operations in Poipet PPSEZ. The firm previously reached a land lease deal in April 2018.

The company said it would contribute to the development of the industrial sector in Cambodia.

Japanese ambassador Masahiro Mikami said Sumitronics' facilities contribute to the Thailand-Plus-One strategy. Thailand-Plus-One refers to Japanese firms increasing revenue by expanding their supply chain network in Thailand toward Cambodia, Laos, and Myanmar.

Poipet now has 17 factories, eight belonging to Japanese companies, and boasts 7,500 jobs. Poipet PPSEZ is owned by Phnom Penh SEZ and boasts access to the border crossing. – CD

## Abstracts Sought for PCB West 2020

**ATLANTA** – UP Media Group Inc. seeks abstracts for PCB West 2020, to be held Sept. 8-11 in Santa Clara, CA. The event includes a four-day technical conference and one-day exhibition to be held at the Santa Clara (CA) Convention Center.

PCB West annually provides a conference and exhibition focused on the design and manufacture of PCBs, HDI, electronics assembly and circuit board test. The event annually attracts nearly 2,000 attendees.

Papers and presentations of the following durations are sought for the technical conference: one-hour lectures and presentations; two-hour workshops; and half-day (3.5 hour) and full-day seminars. Preference is given to presentations of 2 hours in length or more, and no presentations of less than one hour will be considered.

Abstracts of 100 to 300 words and speaker biographies should be submitted to <https://pcbwest.com/abstract-submission-guidelines> by Feb. 28.

## IPC Releases E-Textiles Standard

**BANNOCKBURN, IL** – IPC in December announced the release of a new standard that defines the makeup and testing of electronics textiles.

Developed through input from 140 members of the IPC D-72 Textiles Materials Subcommittee, IPC-8921, *Requirements for Woven and Knitted Electronics Textiles (E-Textiles) Integrated with Conductive Fibers, Conductive Yarns and/or Wires*, establishes classifications and designations for e-textiles integrated with e-fibers, e-yarns and e-wires and standardizes key characteristics, durability testing and industry test methods. Key characteristics include electrical resistance, electromagnetic immunity, thermal conductivity, coefficient of thermal expansion, specific heat capacity, thermal shock resistance, outgassing, Tg and melting point. – CD



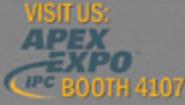



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**ALL IN STORE**

**Trends in the US electronics equipment market (shipments only).**

	% CHANGE			
	Sept.	Oct.	Nov.	YTD%
Computers and electronics products	-0.3	0.3	0.4	3.5
Computers	-7.1	1.1	-0.2	-24.2
Storage devices	-11.3	28.7	20.0	23.3
Other peripheral equipment	2.4	0.6	9.1	6.0
Nondefense communications equipment	0.2	-0.8	-0.4	10.3
Defense communications equipment	-0.4	-8.5	3.8	-5.9
A/V equipment	-3.9	2.3	-14.4	21.6
Components <sup>1</sup>	-1.5	-0.2	3.7	4.3
Nondefense search and navigation equipment	-5.7	4.8	-0.6	2.0
Defense search and navigation equipment	1.4	0.6	2.3	3.4
Medical, measurement and control	0.3	0.6	-2.4	-0.3

<sup>1</sup>Revised. <sup>2</sup>Preliminary. <sup>3</sup>Includes semiconductors. Seasonally adjusted. Source: U.S. Department of Commerce Census Bureau, Jan. 3, 2019

**US MANUFACTURING INDICES**

	AUG.	SEPT.	OCT.	NOV.	DEC.
PMI	49.1	47.8	48.3	48.1	47.2
New orders	47.2	47.3	49.1	47.2	46.8
Production	49.5	47.3	46.2	49.1	43.2
Inventories	49.9	46.9	48.9	45.5	46.5
Customer inventories	44.9	45.5	47.8	45.0	41.1
Backlogs	46.3	45.1	44.1	43.0	43.3

Source: Institute for Supply Management, Jan. 3, 2019

**KEY COMPONENTS**

	JULY	AUG.	SEPT.	OCT.	NOV.
Semiconductor equipment billings <sup>1</sup>	-14.6%	-10.5%	-5.7% <sup>r</sup>	2.5% <sup>P</sup>	9.1% <sup>P</sup>
Semiconductors <sup>2</sup>	-15.5%	-15.4%	-14.6% <sup>r</sup>	-12.7% <sup>P</sup>	-10.9% <sup>P</sup>
PCBs <sup>3</sup> (North America)	1.00	1.02	1.04	1.11	1.08
Computers/electronic products <sup>4</sup>	5.46	5.48	5.52 <sup>r</sup>	5.49 <sup>P</sup>	5.50 <sup>P</sup>

Sources: <sup>1</sup>SEMI, <sup>2</sup>SIA (3-month moving average growth), <sup>3</sup>PC, <sup>4</sup>Census Bureau, <sup>P</sup>preliminary, <sup>r</sup>revised

## Hot Takes

- The production value of Taiwanese fabricators across the China strait rose 1.7% year-over-year to NT\$185.7 billion (\$5.9 billion). (TPCA)
- The global market for IC packaging increased 3% in 2019, as the overall IC devices market declined 3.7%. (New Venture Research)
- Japan PCB fabricators reported October sales fell 7.4% year-over-year to ¥38.3 billion (\$1.27 billion). (JPCA)
- Taiwanese PCB makers' production in 2019 is expected to grow slightly from a year earlier to NT\$656 billion (\$21.74 billion), with strong shipments of rigid-flex boards.
- The HDI PCB market is expected to reach \$15.6 billion by 2024, with a CAGR of 8% from 2019 to 2024. (Report-Linker)
- The AR, VR and MR market will top \$30 billion by 2030. (IDTechEx)
- Worldwide spending on robotics systems and drones will be \$128.7 billion in 2020, up 17.1% over 2019, and will reach \$241 billion by 2023. (IDC)

## PCB/MCM Design Tool Sales Spike 20% in Q3

**MILPITAS, CA** – Sales of software for PCB and multichip module design rose 19.8% year-over-year to \$240.5 million in the September quarter, the Electronic System Design Alliance said in January.

The Americas led the way, with sales of \$83.3 million, followed by Asia-Pacific at \$59.2 million, Europe/Middle East at \$53.7 million, and Japan at \$44.3 million.

The four-quarters moving average, which compares the most recent four quarters to the prior four quarters, increased 10.3%.

Overall electronic design automation industry revenue increased 8.9% during the period to \$2.57 billion. The four-quarters moving average increased 6.8%.

# Which Tech Will Define the Roaring '20s?

The technologies that succeed will likely be variations on our current ones.

A NEW YEAR is always exciting. Thoughts of embarking on new initiatives provide opportunity and inspire everyone to dream big and make them happen. When the new year happens to coincide with a new decade – in this case, the '20s, or as some of my business colleagues are calling it, “the roaring '20s” – one can't help but dream extra big and forecast events that should or could impact our industry in the decade ahead.

Rather than focus on the geopolitical and global economics that clearly impact everyone, too often in an irrational or political way, I will focus on the area I am probably least qualified to opine on: technology.

In the rearview mirror of the past decade(s) have been notable technological disappointments. By “disappointments” I am not saying failures, but technologies, materials and processes that have, so far, not lived up to the hype garnered when first released. Organics, especially OSPs, showed great promise. After many years of refinement, however, the short shelf-life of these surface finishes still makes them too problematic for general use. Yes, they work great in a high-volume, rapid fab-to-assembly-to-OEM application, but for high-mix or ruggedized environments they aren't ready for prime time.

Ditto conductive inks. While still promising, widespread application of conductive inks to replace traditional plate-and-etch processes that have been the bedrock of the industry seems to have stalled. They may get there, but don't hold your breath for them to replace plating. And then there is printed electronics. Once touted as *the* disruptive technology that would replace printed circuit boards as we know them, it too has fallen short of the initial hype. Printed electronics is evolving but in areas and configurations that augment rather than replace traditional printed circuit boards.

If history offers any insight into the future, it appears technologies initially hyped as instant gamechangers or “the” disruptive technology or “must-have” processes usually do anything *but* live up to their hype. However, what appear to be incremental steps toward refining existing technologies, processes and materials more often “suddenly” become the difference-makers that propel the industry forward.

One such example of this is direct imaging. What started as tweaking and rethinking the tried-and-true laser photoplotter led to laser direct imaging (LDI). And the LED folks keep tweaking the brightness and focus of lighting, which ended up being a viable alternative to lasers for direct imaging. Slowly and (relatively) quietly refining existing technologies suddenly became a game-changing imaging tool for fabricators of all sizes and technology focus.

Looking forward, I see similar evolutionary refinements resulting in that wow! factor. Clearly sensor technology has evolved and is still evolving. I am not so sure the much-touted Industry 4.0 will be the result of the merging of sensors and software. I expect the goal of a connected factory will be the same at the end of this decade as it was at the end of the past one, not to mention the five before that. Improvements will be made, but various communication gaps will lead to a technological let-down for the connected factory.

On the other hand, I predict sensor technology will be harnessed like never before to manage discrete processes many feel are not suited for automation. Batch plating lines, for example, may be the biggest recipient of creative adoption of sensors and software. Applying sophisticated process management via sensors and software may result in long sought-after precision, speed and consistency of short-run plating processes, enabling the trifecta of lower cost, faster throughput *and* tighter tolerance (read, higher technology) in the competitive North American specialty fabrication segment.

Enhanced sensor capability yoked to more sophisticated software should enhance other aspects of manufacturing printed circuit boards. I expect that over this decade we will see these improved temperature sensors used to better control lamination presses, temperature rise and cycle temperature stability so that new, higher-temperature and enhanced laminates, prepregs and bond films can be deployed more easily and robustly, especially as extremely high Tg laminates become more common.

Similarly, I expect redeployment of sensor technology will radically change drilling equipment. Sensors should be able to displace x-ray technology as the tool of choice for registration control, enabling drills to make rapid adjustments more easily, accurately and consistently – regardless of material movement – to drill with tighter tolerances without the need for human oversight. Yes, such machines are currently available, but by the end of the decade such machines will cost less and maintain exponentially better tolerances.

And, progress will continue with ink technology. Printed electronics will evolve and nibble at the fringes of circuit board applications, and scientists will continue to work on environmentally friendly surface finishes.

None of this is either radical or rocket science, and that's just the point. Over the years ongoing, persistent evolution has enabled our industry to produce awe-

*continued on pg. 24*

## PETER BIGELOW

is president and CEO of IMI Inc.; pbigelow@imipcb.com. His column appears monthly.





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# Gazing in a Crystal Ball

Why the “rise of the robots” might be a good thing for workers.

**ONCE A YEAR**, I like to take a column to look at the trends I’m seeing for the coming year. I think 2020 is going to be fairly good for the electronics manufacturing services (EMS) industry.

The trade war finally appears to be cooling down. Both China and the US have been hurt by it, and I think both sides have reached the point where they realize that not reaching an agreement will cost both of them lucrative manufacturing sectors, since China is seeing production migrate to Southeast Asia, and the US is seeing production move to Mexico. As I write this, the phase 1 deal has yet to be signed. If it does get signed in early-2020 and tariffs begin to lift, that could remove the trade-war-driven drag on the US manufacturing economy. The signing of USMCA will also have some positive effects and hopefully improve the competitiveness of US manufacturing within North America.

That leads to a more interesting trend: unemployment, or lack thereof. Many readers don’t remember what 3.5% unemployment markets look like, because it has been nearly two decades since we were in that range. In the 1990s, what folks would say when we got to that level was everyone who was employable had a job. Manufacturing sector companies face a double whammy this time around – and EMS companies are even more disadvantaged. Why? For the past two decades we’ve been telling youth that manufacturing jobs are 20th century jobs, and their best career option is to get a college degree and work in the service

sector. Consequently, hiring labor in a job hunter’s market isn’t a matter of running an ad and watching people line up. It becomes an education effort, with a higher-than-average failure rate when applicants who don’t like the disciplined focus of manufacturing decide to look elsewhere after a few weeks on the job. The reason I say EMS companies are more disadvantaged is because the average American doesn’t know who they are. The products they manufacture carry the names of other companies. In a generation where folks aspire to work at companies like Google or Facebook, branding matters. Additionally, margins in EMS are tighter, so benefits and compensation are less, which means EMS companies must do more than a company with a recognizable brand to capture

the interest of potential entry-level employees.

Those dynamics lead to another trend I’m seeing in EMS: training and job enrichment. There is no question greater levels of automation are good from a quality standpoint because it reduces variation. Even smaller EMS operations are starting to invest in Industry 4.0 technologies that give machines more control over SMT line adjustments. And the labor shortages driven by a good employment market are driving a lot of value-stream mapping and continuous improvement efforts designed to reduce the headcount required to do assembly in general. These trends aren’t putting workers on the street. EMS companies are realizing experienced workers are valuable assets and are investing more in training to give them higher skill levels. In some cases, SMT operators are being trained to the level of a process engineer. Test operators are being encouraged to look at test technician career paths. Personnel in other production operations are seeing paths to advancement as well. In all the cases I’ve seen, it is a pay-for-skills arrangement where greater skills translate to better compensation. So, for employees willing to train and evolve into higher responsibility jobs, the rise of the robots may be a good thing.

Finally, I’m seeing a lot of shopping going on in 2020. Regional dynamics and cost structures have changed dramatically over the past two years. Now that materials constraints have eased a little, OEMs are reevaluating whether their current outsourcing strategy works. This is a good

time for EMS companies to exhibit at trade shows, advertise and promote in social media for that reason.

I also see a few clouds on the horizon. The trade war has been a drag on an otherwise healthy US economy, and when the brakes come off, I think we could get some surprises. While material constraints have eased significantly as supply and demand have aligned, some of that easing was due to manufacturing slowdowns. Additionally, the 5G rollout in 2020 may add some additional steep demand. So, keep a close eye on materials trends mid-2020. And if the economy really improves, expect jumps in energy and commodity prices, leading to price inflation. All that said, I do expect 2020 to be a year of growth and prosperity for the EMS industry. □



**SUSAN MUCHA** is president of Powell-Mucha Consulting Inc. (powell-muchaconsulting.com), a consulting firm providing strategic planning, training and market positioning support to EMS companies and author of *Find It. Book It. Grow It. A Robust Process for Account Acquisition in Electronics Manufacturing Services*; smucha@powell-muchaconsulting.com.



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# How Quickly Can You Move PCB Business?

Expand your manufacturing base at little or no cost.

**WHY ARE PCB** purchasing departments often hesitant to move business to a new vendor, even when it is clearly warranted? Perhaps it's the overly cumbersome process many buyers require before production can be moved.

Adding a new supplier to an approved vendor list (AVL) needs to be done with care, but I don't understand why many firms make it harder than it has to be.

It is important to keep PCB vendors on their toes. They should know that you, as a circuit board buyer, regularly review vendor pricing and performance and are willing to move business when necessary. And the truth is adding qualified suppliers may not be as difficult as you think.

Here's how to evaluate a potential vendor:

**Get a trial quote.** For the buyer, it's all about price. There's no need to get the quality or production departments involved if the only reason to move a board is for better pricing. Start with a trial quote from a potential vendor, *after* you have an NDA in place. Have the Gerber files available for a PCB that your company assembles often enough to use for price benchmarking purposes. Send those files, along with your corporate PCB fabrication specification (your company has fab specs, right?), to the vendor with a request for a trial quote.

If the prospective vendor's benchmark quote comes back at a higher price, and you are happy with your present vendor's performance, then move on to another potential vendor, if desired.

If the price comes back lower than your current supplier, that doesn't mean you should immediately jump ship, especially if it's a difference of only a few percentage points and you are happy with your current vendor's performance. But it does mean you should at least consider moving orders.

**Check references.** If the trial quote looks good enough to justify moving an order, proceed to the reference checks. Ask for at least three references, preferably in the same industry. And make sure you actually call those references. (You'd be surprised how many companies don't.)

Ask how long the reference has worked with the prospective supplier. Find out how much of their annual spend is invested with the vendor and why. Also important: Does that reference require the same product as you? The vendor may be great at two-layer and four-layer work, but what if you require

eight-layer and above? Get specific so you don't miss crucial information. Ask how the vendor handles scheduling changes or quality issues. Great pricing means nothing if it comes with poor customer service.

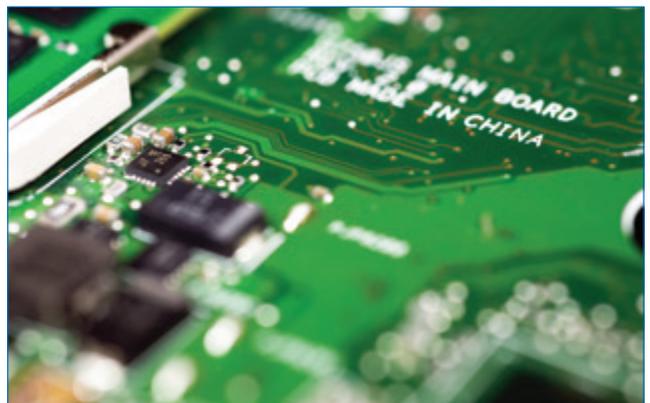
**Money matters.** If the references are good, it's time to check the vendor's financial stability. Run a D&B report. Call the vendor's bank and suppliers. Make sure the vendor pays its bills. A vendor that pays its own suppliers on time is more likely to be able to deliver *your* orders on time. Getting financials from an offshore vendor can be difficult, so in that case, double-up on references instead, and hit harder on questions concerning timely communication and customer service.

**Quality concerns.** If pricing, financials and references look right, it's time to get quality involved. Make sure your prospective vendor has all the required credentials, such as UL and ISO, as well as anything specific to your customer's needs. Send out a vendor survey (you have one of those, right?) and create a vendor file. Have your quality staff talk to their quality staff. Ensure the prospective vendor understands the quality paperwork (CofC, ET and material certifications) required to properly accept a shipment.

**Talk to production.** Production departments are usually and understandably averse to change. Don't cut your new vendor into the production schedule without involving production in the approval process. To help put production at ease, consider a contingency purchase order to the vendor (with tooling and test

*continued on pg. 24*

**GREG PAPANDREW** has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying; greg@boardbuying.com.



**FIGURE 1.** While China might not be the preferred build geography, relocating production is a methodical, intensive process.

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Here's how it works: Say a project requires a particular PCB every month. Order the next delivery from your present vendor and the following delivery requirement from your *prospective* vendor. Have both orders arrive on your dock at the same time. Have production assemble the boards from the present vendor as scheduled, along with a sampling of the boards from the prospective vendor. If your production and quality teams are happy with the sample assembly, you can be confident in the work of the new vendor.

If the boards do have a problem, according to IPC or your corporate specs, review the issue with quality and production. Don't give up quickly on that prospective vendor. Was the issue related to poor communication that could be easily fixed for the next run? Or was it a real quality issue, where the boards are useless?

If the sample build is done immediately, you should have plenty of time to determine whether to give the vendor another try or reject the order outright. You can then order the next requirement from your present vendor without missing a beat in your assembly schedule.

If the order is rejected, there is no invoice from the prospective vendor.

Every company needs to be held accountable. Your fabricators should know you are closely monitoring pricing and performance, even long after you've established a relationship with them. And your buyers should have the confidence to move business quickly and easily, whenever necessary.

A carefully thought-out vendor selection process will expand your manufacturing base and help your company maintain its competitive edge, with little cost in time or resources. □

*ROI, continued from pg. 18*

inspiring, cutting-edge technology. Everyone looking for the proverbial holy grail of new and disruptive, yet consistent tweaking and modifications has led to game-changing processes, equipment and materials that propel us forward. I predict just such evolutionary progress continuing during this new decade, the roaring '20s, as it has over so many of the past ones.

I look forward to seeing how it all transpires over the next 10 years. I expect it will be challenging times for all. However, I know it will be equally exciting to see what technologies emerge and thrive, and dare I say, it will be fun to be a part of. □



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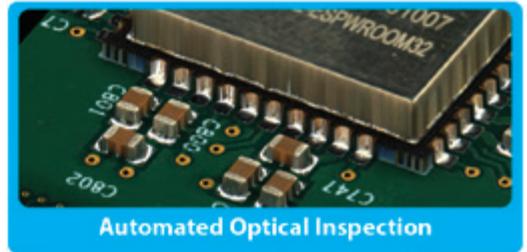


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# The Role of Heterogeneous Integration in the AI Hardware Ecosystem

Does Moore's law apply to the new HI frontier?

The IEEE International Electron Devices Meeting (IEDM) held a night panel discussion on Dec. 10 titled Rest in Peace Moore's Law, Long Live AI. As the title suggests, the discussion focused on the future of computing and the role of hardware. The moderator proposed questions like will CMOS technology become commoditized and differentiation occur mostly in circuit design, algorithm and architecture development? Will special purpose coprocessor adoption rates accelerate beyond CPUs and GPUs? What is the role of heterogeneous integration in the AI hardware ecosystem? Will the traditional memory hierarchy be upended by the arrival of non-volatile memory? Will analog accelerators using non-volatile memory elements drive the future semiconductor roadmap as scaling slows, enabling exponential improvements in compute efficiency and performance? Not all the questions were answered, but the discussion was lively.

The panel was moderated by Vijay Narayanan, IBM Research, with panel members from major OEMs, chip makers, packaging foundries and academia. The first section focused on the health of Moore's Law.

Wilfried Haensch of IBM Research quoted an Apr. 19, 2015, article in *The Economist* that explained the end of Moore's law. The article explained Gordon Moore's economic observation in 1965 that by shrinking transistors, it would be possible to double the number of transistors that fit onto an integrated circuit every year (revised to roughly every two years), providing a cost advantage to scaling. Haensch indicated economics is critical in artificial intelligence (AI) and the deep learning explosion. Showing a slide from IDC on worldwide growth in the AI market, he projected that AI machine learning is the next IT. Is heterogeneous integration (HI) Moore's law 2.0? According to Haensch, Moore's law is based on economics (observation) and represents a tradeoff between productivity and yield. The tradeoff will continue, but the cadence will not. HI adds complexity to the component. AI solutions are, generally speaking, accelerators for specific tasks. Accelerators will provide better utilization

and power/performance than simply using a CPU-based solution.

Mike Henry from Mythic, an AI accelerator startup, commented that cost improvements are on a flat line. Memory density, power, and bandwidth are concerns. Linear digital designs, no matter how integrated, won't help shrinking modules. What will help, he said, is technology that solves power density and bandwidth of the memory. Putting the compute as close to the memory as possible is essential.

Dimitri Stukov, a professor from University of California, Santa Barbara discussed use of in-memory computing to prolong Moore's law scaling. Ron Ho of Facebook also referred to Moore's landmark paper, while noting the minimum cost point vs. yield loss, stating, "It's all about economics." Cost is an important, self-fulfilling prophecy. Ho discussed five data

points, including the energy cost of monitoring data off-chip vs. on-chip. "Whether or not Moore's law is dead does not matter," Ho asserted. "What is important is yield for energy. Sustaining power solutions is the line now, not cost."



**FIGURE 1.** Members of the IEEE International Electron Devices Meeting IEDM panel.

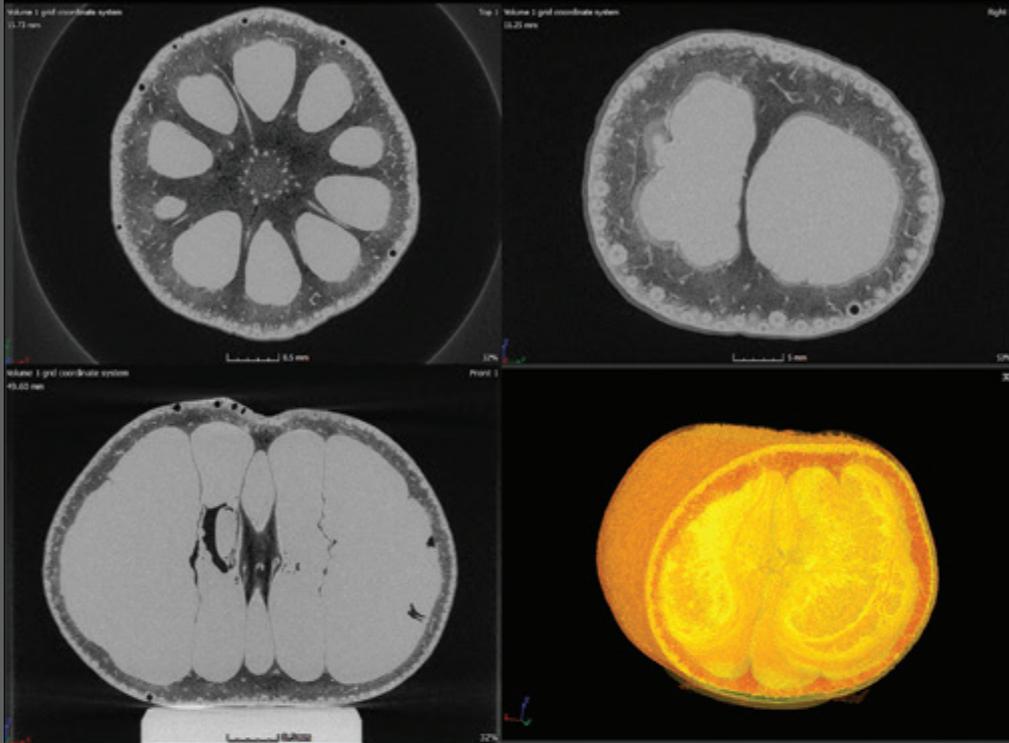
Douglas Yu from TSMC indicated HI helps the Moore's law concept for logic-to-logic integration and stated Moore's law is alive and well, enhanced by HI! He commented on the new era in packaging for microprocessor, CPU, FPGA and AI accelerators based on options such as Intel's embedded multi-die interconnect bridge (EMIB), and TSMC's chip-on-wafer-on-substrate (CoWoS) and integrated fan-out on substrate (InFOoS) or InFO\_MS (MS for memory stack), including transition to the use of high bandwidth memory (HBM) stacks and UMD. Yu discussed new 3-D interconnect options, such as TSMC's system on integrated chips (SoIC) + CoWoS and SoIC + InFO. Yu calls this a new era in frontend plus backend (FE+BE), holistic 3-D HI, and indicated there are tremendous advantages to best optimize system power, performance, area and cost (PPAC) for "More Moore" and "More-than-Moore." While Moore's law 1.0 is about SoC scaling, 2-D scaling and transistor scaling, Moore's law 2.0 is about system-

**E. JAN VARDAMAN**

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on-package (SoP) scaling and 3-D interconnect density (3DID) scaling. TSMC is also proposing a new metric to show 3-D interconnect density: number of line and traces/mm across chip boundaries on an interposer, or substrate multiplied by the number of vertical interconnects (min. pitch) between stacked chips/mm<sup>2</sup>.

Vivek De of Intel argued Moore's law and AI are better together, and no exponential is forever. It is not a one or the other discussion. AI today is because of Moore's Law. HI, 2-D/3-D, processing big data, AI deep learning, logic, DRAM, and NAND all are Moore's Law plays. Moore's law may have stopped moving as fast in 1975 and slowed down, but this does not mean there is demise.

A second discussion topic focused on digital vs. analog, with a perspective on custom accelerators vs. CPU and the role of HI. IBM Research's Haensch indicated hardware design takes advantage of AI algorithms. HI is needed to further decrease bandwidth constraints on data rate for memory access. Logic needs memory access without latency to function properly. Analog and digital will coexist and are best integrated. Analog has some advantages for custom accelerators. Stukov also indicated a focus on analog hardware is good for neuro inferencing. Ho of Facebook discussed the application of augmented reality glasses. Power is one of his critical concerns. A custom accelerator could help the latency problem.

The third topic looked in the crystal ball. IBM predicts

one of the major drivers in human-machine interaction will be "i-shopping," focused on targeted retail marketing, instant identification, and personalized advertising. Mystic discussed disruptions such as 5G and lack of understanding of the impact AI has on us. Intel discussed integrated ReRAM and logic technology beyond CMOS. Stukov described AI as a technology that will influence the future computer landscape.

Yu proposed the concept of immersion in memory compute for the future, where one would integrate multi-cores logic + memory with closest proximity logic-to-logic and logic-to-memory for AI. He also explained the concept of deep partitioning. InFO and CoWoS are backend 3-D solutions for heterogeneous integration. (They encompass DDR/GDDR and eDRAM, as well as HBM.) SoIC is frontend 3-D that enables deep partition, permitting logic that is not easily scaled to be partitioned. Deep partitioning focuses on scaling in the core for high-density and removing parts that can be pulled off but packaged together. Deep partitioning provides continuous improvement on total cost, time-to-market, performance, and power.

Intel's future look included neuromorphic computing, distributed autonomous learning, and neural networks. De indicated that while there has been a slowing of the transistor in the past 50 years, power is the ultimate limit of Moore's law. He indicated High K Metal Gate (HKMG) and FinFET developments are cost-effective developments. New switch devices can be expected as architecture innovates. □

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# The Case for Copper Pour on Routing Layers

Don't be afraid of the ground.

**DOING SPECIAL THINGS** with a circuit pattern is a hallmark of analog design. All the important signals on the board added together are equal in importance to one net; that net is the ground net. Every active component will have at least one of its pins tied to ground. An RF device could use any number of voltages and will likely want a dedicated power supply for each voltage required. Characteristic impedance relies on a ground plane or two.

Faster digital circuits start to behave like their analog counterparts. The typical routing rules involve fanning out the surface mount pins with short segments and doing the main course of the routing on an innerlayer. An elegant placement could make it possible for the bus of related traces to run entirely on the outer layers.

In that case, we don't get to sandwich the traces between ground planes to stifle electromagnetic radiation (EMI). The saving grace is we don't use vias to transition the signals to innerlayers. Printed circuit board design is always a balancing act. We use vias anyway, but in a different way. Wrapping the bus in a full metal jacket on the outer layer and staking the edges of the ground plane to the innerlayer ground is usually sufficient to meet the EMI specifications, where short digital traces are concerned.

**When to use caution.** Ground pour not accompa-

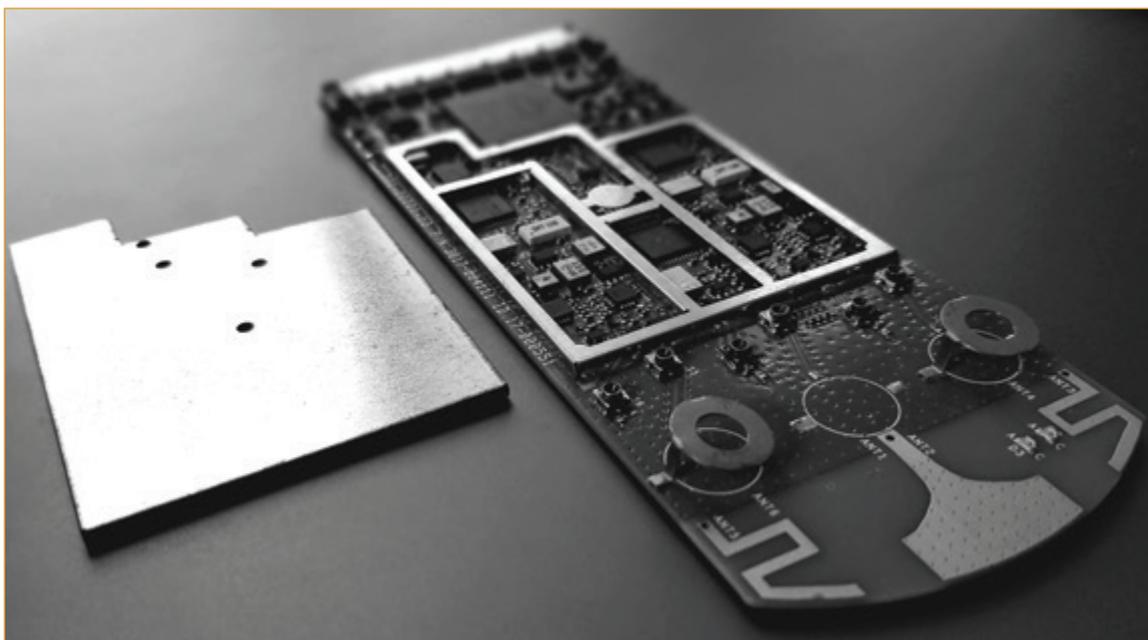
nied by ground vias can become a conduit for cross-talk between the traces on either side of the ground shape. Removing that copper, leaving the excess air gap, is better than an unsupported metal icicle to serve as an antenna between two lines, whether they are aggressors (noisy) or victims (sensitive to noise).

Count on clocks to be noisy. Receive chains on their way to the input pin are possibly the worst in terms of being a victim. It isn't always that obvious. Reset lines and other sundry circuits can generate noise. Pretty much any kind of sensor will be a victim, even when the aggressor is routed several layers below the sensing device. Consider the entire board around a sensor to be a no-man's land in terms of circuits not related to the sensor. As always, read the relevant datasheet application notes regarding layout.

**Outer layers.** We often label metal layers in a PCB categorically. The outer pair of layers are known as primary and secondary placement layers. The primary placement layer can be top or bottom; it depends on which has the greater number of components. It could also depend on a definition from the physical design team. If the busy side of the board faces downward in the enclosure, it will likely be labeled the bottom but would be considered the primary side.

No matter the context, the component placement layers offer the best possible location for using a

**JOHN BURKHERT JR.** is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally he was an RF specialist, but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.



**FIGURE 1.** Wifi to the rescue!



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### **Design Essentials for PCB Engineers, SUSY WEBB**

Engineers designing their own boards will need to understand and use the same science that seasoned PCB designers have built up over many years. For example, the way parts are built, or a board is designed can make a huge impact on the ease of fabrication and assembly, just by the practices put into place while working. Those practices can increase yields and lower the cost for all, and this two-day workshop starts with thoughts about that. There are many ways to place parts on a board, but some work much better than others for the physics, electrical and mechanical purposes. We will discuss the order of placing parts, setting up routing, and placement ideas that will lead to better flow.

On Day 2, fine-pitch BGAs will be examined. Their size and pitch make them increasingly challenging to work with, as do the signal integrity and EMI issues that come along with them. We will look at through-hole and HDI examples for fanout, grid and routing information, and their specific manufacturing needs. In the last section we will delve more into the science of how everything works together by discussing the electronics and physics, controlling impedance and high-frequency energy, and stack-up and power issues. There will be examples of how a signal's field energy actually flows through layers of the board, and steps to take when routing signals through the board. The workshop will conclude with a brief discussion of autorouting vs. hand routing.

copper flood as a passive heat sink. Through-hole or surface-mount pins can attach directly to a shape. For better solderability, the shape can be defined with a clearance, plus spokes that tie the pin or pad to the outer layer ground planes.

**Free reliability through thermal performance.** Almost every component on a PCB could generate heat as it does its work. The hottest location in the system is where the chip attaches to the substrate or interposer. The junction temperature at that point determines the lifespan of the component and thus the system. A strong layout provides the thermal path to success.

When the electromagnetic radiation is well shielded, the system's emissions go down. That effectively reduces power

consumption. All your good impedance practices contribute to the efficiency of the power domain. The component doesn't have to work as hard when there are fewer discontinuities. It's a little thing that adds up over time.

Uncontrolled thermal excursions can lead to early failure. Early failure leads to warranty work or product replacement on your dime. Fixing or replacing previously sold items cuts into whatever profit margin came from the initial sale. Lower profit leads to all kinds of bad things, ultimately going out of business. Don't go out of business. Get busy with the planes.

**On slots.** A technique taught to me at Qualcomm was to break the plane around an external oscillator with a gap that cuts the ground around the device and its posse of resistors.

The three sides not connected to the processor are framed by the void. This will help confine the oscillator's switching noise.

I always say put in some ground vias near any slots. In this case, this provides an escape path on the next ground plane for all those oscillations to propagate their heartbeat onto some unsuspecting transmission line. Back off on the ground vias a bit on the quiet side of the gap. Maybe even repeat the gap on the first inner (layer 2) ground plane if there are no traces running through there on layer 3. Reroute them if possible so you can trap the noise and corral it back to the device.

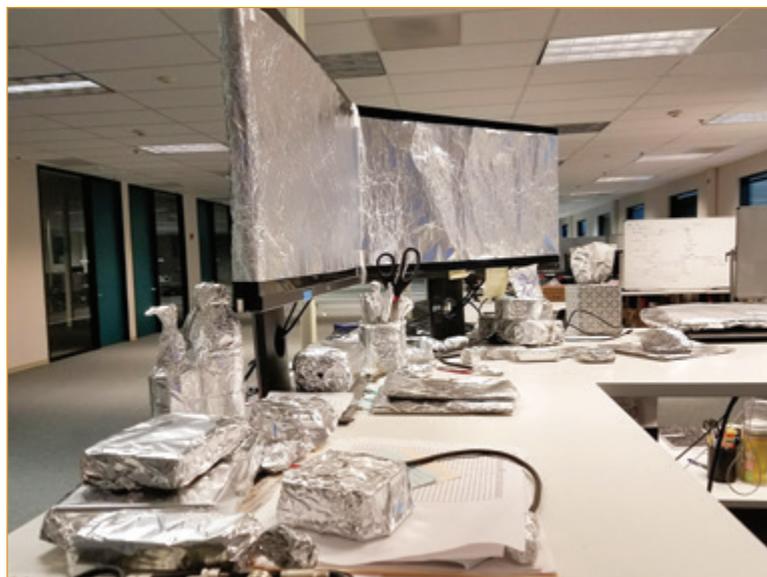
**Innerlayers.** When you flood a layer with significant routing on it, some areas are bound to wind up isolated. The way you group the traces will have a profound effect on the outcome of the ground flood. The first thing I do is set a wider gap rule between the copper flood and traces or shapes.

Backing off will keep the traces from becoming a coplanar line of unknown impedance. I use 0.50mm pull-back, about double what would be typical on the actual ground plane layers. Some busses get 1mm if they are long or have higher data rates. It also helps to set a larger aperture so the copper cannot even get between two traces that are close together.

Managing copper "islands" is a matter of setting a higher threshold for the minimum size. A blob of copper that has a single ground via in it isn't doing any good. When it comes to power plane layers, there is room for ground pour as well. Let's say you have a nice frame of ground vias around the perimeter of the board. Pull back the voltage plane and add a frame of ground that joins the stitching vias and completes the Faraday cage around the power planes. Your compliance team will see that and regard you as a saint. Manage it carefully, but don't be afraid of the ground. □



**FIGURE 2.** When you're hot, you're hot. When your board is hot, that's not so hot. (Source: BigStockPhoto)



**FIGURE 3.** You go on vacation, you come back to a well-shielded workstation.

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# CLEARSignals

## **RAIG: Reduction-assisted Immersion Gold Eliminates Corrosion, Allows Thicker Deposits on ENIG & ENEPIG**

**Industry Experts Share Their Views:**

- ▶ **Don Gudczauskas**, Vice President, CTO
- ▶ **George Milad**, National Accounts Manager for Technology and Chair of IPC's 4552 Committee
- ▶ **Rich DePoto**, Business Development Manager
- ▶ **Patrick Valentine**, Director of Technology
- ▶ **John Meyers**, Manager, Strategic Accounts
- ▶ **April Labonte**, Senior Applications Engineer

# “RAIG” answers demands for thicker immersion gold – without corrosion

**Moderator:** TWX-40 reduction-assisted immersion gold was introduced in 2018 as a nickel corrosion mitigation option; what has been the field experience to date?

**Meyers:** “From one large customer’s perspective, their Canadian facility has run ENIG for many years. They are installing the TWX-40 RAIG process because it will eliminate intermittent corrosion issues. With the continual demands on circuit boards fabrication – the way they’re built, new materials, increasing line density – the industry finally has a process that fully addresses nickel corrosion.

The fact is, this process is so unique, and has become so desirable, that it has created a strong pull into large PCB manufacturers who would not have considered changing ENIG and ENEPIG chemistries before.

A major OEM evaluated the process and created a market for this process among PCB shops. This type of ‘customer pull’ only happens a few times in a generation.

- ▶ **RAIG:** Reduction-Assisted Immersion Gold
- ▶ **ENIG:** Electroless Nickel / Immersion Gold
- ▶ **ENEPIG:** Electroless Nickel Electroless Palladium / Immersion Gold
- ▶ **EPIG:** Electroless Palladium / Immersion Gold
- ▶ **IGEPIG:** Immersion Gold / Electroless Palladium / Immersion Gold

We are now doing installs systematically at shops around the country. This speaks volumes about the advantages of UIC’s TWX-40 RAIG process.”

**Valentine:** “Dovetailing what John said, what I have been particularly impressed with is the distribution of TWX-40, especially at higher thicknesses. We have seen a small coefficient of variation for gold thicknesses. That is very advantageous for increasing circuit density and cost considerations. Also, being able to put a uniform coating of gold down on a very small wire-bond pad and a plated through-hole is a major performance advantage.”

**Labonte:** “Shops are definitely interested in TWX-40 for both ENIG and ENEPIG. Customers are continuing to push the bath’s MTOs without issue and gold plating rates have remained consistent throughout the life of the bath.”

**Moderator:** What changes are needed to run the process effectively?

**Labonte:** “The most critical requirement is a full working lab. TWX requires slightly more lab support than other immersion gold baths. Sometimes we need to assist customers in breaking bad habits, such as leaving immersion gold baths at temperature without work being processed.”

**Moderator:** What specific technical advantage does TWX-40’s RAIG provide compared with other options for corrosion-free ENIG and ENEPIG deposits?

Don Gudczauskas

George Milad

April Labonte

Patrick Valentine

John Meyers



**Milad:** "Very simply, TWX-40's reduction-assisted immersion gold gives the manufacturer the option to add more gold to the final finish layer without compromising the underlying nickel deposit. When we say 'more gold' we're looking for an increase to 3-4 microinches. These gold thickness deposits can be obtained on both ENIG and ENEPIG."

**Moderator: Why would a PCB manufacturer choose a RAIG process over high phos nickel immersion gold?**

**Milad:** "TWX-40's RAIG process provides the best protection and widest operating window against nickel corrosion. Although a correlation exists between higher phos nickel and lower corrosion, that strategy may not be totally effective."

Field performance indicates that a significant number of ENIG and ENEPIG plated layers with high phos nickel continue to have corrosion. It's Uyemura's position that, after evaluating all of the factors that affect nickel corrosion, including solution flow, pretreatment steps, plating rate, bath loading and chemical control variation, that the most reliable way to mitigate corrosion is to subordinate the immersion gold reaction and allow a reduction-assisted autocatalytic reaction to plate the majority of the deposit layer.

This strategy allows for a wider gold thickness target range. The fabricator can produce corrosion-free nickel final finish layers, consistently, with the operator skill levels that prevail in the industry."

**Gudeczauskas:** "In addition, the use of TWX-40 RAIG allows the nickel phos content to be kept in the middle of the range. The nickel-tin intermetallic solder joint grows faster with higher %P in the nickel. Thicker intermetallic lowers long-term reliability. Industry data suggests that longer-term solder joint reliability for high %P nickel will not be as good as for mid-phos nickel. Higher %P may well be a good option for shops that don't want to install a RAIG bath; we're looking at that for some facilities using a high phos nickel product such as our NPR-8."

**Valentine:** "There are several ways to mitigate hyper-corrosion. Options include modifying the electroless nickel bath stabilizer, electroless nickel bath operating parameters, rinsing parameters, or gold bath chemistry. Reduction-assisted immersion gold is where

UIC is differentiated. Relying only on increased phosphorous that is not necessarily uniformly distributed within the bulk nickel may not always produce the desired corrosion mitigation effect.

*Rich DePoto*

This factor, combined with the different metallurgical properties of high %P nickel layers (decreased hardness, increased compressive stress, higher resistivity, poorer heat dissipation, a narrower solderability window) is what drove the development of the RAIG process.

TWX-40 RAIG also allows thicker gold deposit layers with low nickel corrosion. This allows leeway for shops that are dealing with legacy ENIG specifications of 3+ microinches of gold deposit for medical, military and other applications.

In addition, the RAIG process allows for thicker gold for ENEPIG. Thicker gold opens up the process window for wire bonding at assembly."

**Moderator: Let's discuss the industry's increasing interest in ENEPIG. What makes TWX-40 an important component to successful ENEPIG processing?**

**Milad:** "Building gold thickness on palladium is much more difficult than on nickel, and TWX-40's reduction capabilities allow this to happen much more readily. People who use ENEPIG are looking for gold wire bonding as well as soldering, and they prefer a thicker immersion gold. We say the immersion gold on palladium is in the range of 1.2 to 1.5µin, and most designers feel that even a little more gold goes a long way toward improving gold wire bonding."

**Valentine:** "There are definitely some electrical designs that benefit from the higher reliability of thicker gold. Gold wire bonding on ENEPIG is a diffusion bond, not an intermetallic adhesion bond. Thicker gold improves wire bond reliability."

**Milad:** "With thicker gold deposit layers comes improved wire bonding yield. For the people doing the bonding, higher gold increases yield. For ENEPIG, 'thicker gold' is more than 1.5µin; between 2 and 4µin is ideal for wire bonding using ENEPIG."

**Valentine:** "For some end users, it comes down to wire bond pull strength. The IPC industry standard and the MIL spec require 1 mil gold wire at 2.5 or 3 gm. pull force. Some OEMs and end users want pull forces of 8 and 9 and 10 gm— 3 times over the spec. Thicker gold helps achieve that."

**Moderator: Rev B has not yet been issued, so why are manufacturers addressing nickel corrosion so aggressively?**

**Meyers:** "PCB manufacturers are trying to stay ahead of the specification. Many companies have done extensive testing and multiple corrosion studies, and when Rev A (IPC 4552) came out, they moved to get out in front of it. Quality departments were charged with



identifying where each facility ranked on corrosion and the options for addressing the issue. This is what brought the reduction-assisted alternative to the forefront. In one case, one of the divisions had already installed TWX-40 and its performance out-performed all of the other submissions. Since that evaluation, there has been no looking back in deciding which immersion gold to install."

**Moderator: How are companies protecting themselves from liability re: compliance with upcoming IPC specs?**

**Meyers:** "Liability is a major concern that PCB manufacturers know they will face. This is what drove the decision to aggressively eliminate the potential of corrosion on ENIG and ENEPIG. Consider this: the Canada facility was driven by corporate engineering, quality, and resident engineering to eliminate nickel corrosion. TWX-40 proved to be the best answer."

**Moderator: Are there any credible industry voices who challenge the TWX-40 'no-corrosion' claim?**

**Milad:** "The paper I delivered at SMTA, which will shortly be published by PCB007, outlines the TWX mitigation of corrosion in detail. As for our competitors, some have re-written history, and now claim that they 'invented' an ENIG which is corrosion-free. They have their own strategies to mitigate nickel corrosion with various nickel barriers or corrosion-resistant layers."

**Moderator: Do competitors have an equivalent alternative, perhaps with a high-phos nickel strategy?**

**Gudeczauskas:** "Increasing the phos content of the electroless nickel reduces nickel corrosion, but Uyemura does not see this as the preferred solution. The use of TWX-40 allows for NO corrosion on a variety of phos contents of deposited electroless nickel. While competitors advocate higher phos content electroless nickel to address corrosion, we view this as turning the knob on a single process parameter. The TWX-40 RAIG process provides maximum latitude on the percent phosphorous with a low-corrosion – or no corrosion – deposit."

**Valentine:** "I think the low coefficient of variation in gold thickness (uniformity) of TWX-40 will help process control dramatically, and is one of RAIG's most important features."

**Moderator: When IPC 4552 Rev B kicks in, what will be the most immediate effect on the industry?**

**Milad:** "Rev B will say PCB suppliers have to do a corrosion evaluation, and determine whether a sample has Level 1, 2 or 3 corrosion. It also sets forth the recommended methods for evaluation. Rev. A does not have this requirement. Unlike Rev. A, which

condemns any occurrence of level 3 corrosion, Rev. B examines multiple locations and offers a method of extrapolating an overall "product rating." An occasional level 3 may not alter the acceptable product rating. This change will require PCB manufacturers to rethink their ENIG and ENEPIG strategies."

**Moderator: What other capabilities does TWX-40 RAIG provide?**

**Meyers:** "EPIG has been getting a lot of interest, particularly for high frequency applications. OEMs are running high numbers of prototype parts to address high frequency signal loss. And today, we have a job shop that already has 22 customers. Additionally, I spoke to a customer's business unit president yesterday, and he said that last week alone, they had 3 large customers who were 'begging-slash-demanding' EPIG, asap."

Now, they are branching off with future rev numbers, where they're switching from ENEPIG to EPIG. What's driving this must be a frequency loss issue. It's beyond the bickering that often goes on in the shop; it's now customer and sales-driven. This would not be happening without TWX-40's reduction-assisted immersion gold deposition on electroless palladium."

**Gudeczauskas:** "One of the main advantages of EPIG that I see is that it is a less complex process. When you take the nickel out, you simplify the process and absolutely eliminate nickel corrosion as a concern."

**Valentine:** "One consideration that can surface under certain assembly conditions is the potential for Kirkendall voids at the interface of the palladium and copper. Customers who object to any voiding even on a microscopic level need to be aware of this. In those cases where the highest reliability is required, customers should move to Uyemura's IGEPIG. This process provides the most reliable layer deposit of all the combinations."

**Moderator: Are there any other major suppliers who are promoting the EPIG process?**

**DePoto:** "Other suppliers are attempting to make inroads, but Uyemura is driving this technology. One of the major issues we face is that it's difficult to get an OEM to say 'this is what made a particular high frequency circuit possible.'"

The future is clearly in high frequency designs; we just need to verify the data and the contribution of the final finish; specifically the contribution of nickel to high frequency signal loss."

# DES Supplies Modern-Day California Gold Rush

Quality gold processing powers growth for Santa Ana board plater



*Racking rigid panels for pattern plating*

Data Electronic Services (“DES”) processes ENIG, ENEPIG, immersion silver, immersion gold and hard gold, using Uyemura chemistries. In 2017, it added EPIG (also from Uyemura) to its capabilities.

Nickel, today, is what customers love to hate - and that’s particularly true of the elite medical and military customers that represent the majority of DES’ work. It is they who provided the impetus for the EPIG addition – a move, explains DES President Humberto Murillo, that stems from the negative effect nickel has on the signal integrity of boards used in high frequency applications.

In adding the new chemistry, DES put its quality team to work. That team, comprised of April LaBonte, Chris Carrillo, and Jeff Rand – all Uyemura tech support specialists – and DES Chemical Engineer Shailesh Vaghashia and Quality Manager Gabriela Murillo set up an in-house quality analysis system similar to what had been established for other processes. It involved XRF; atomic absorption spectrometry; solution and plated board testing,

cross sectioning and photography; daily SPC charting, and quarterly audits and audit validations.

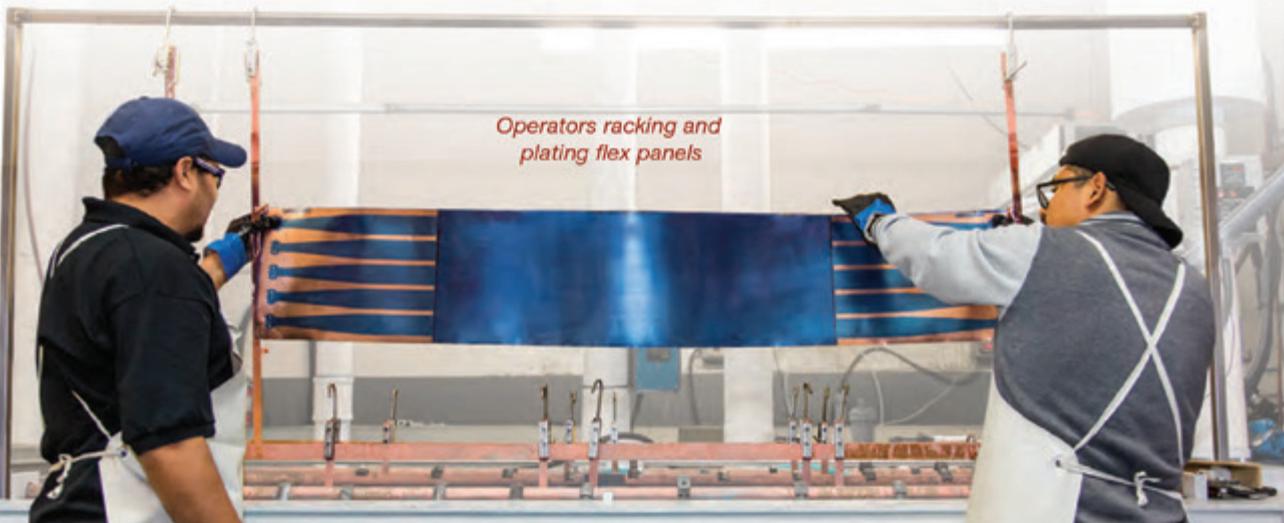
It also included several tracks of documentation: DES is ITAR compliant, holds AS9100 D and ISO 2015 certifications, and complies with IPC 4552 and 4556.

DES prides itself on its high acceptance rates, zero corrosion history relative to its gold chemistries, and compliance record. There are times when compliance takes on a different meaning, however, such as when a customer specs a gold thickness deposit that’s higher than standard ENIG can achieve.

Specific instances include a program requiring not 1-2  $\mu\text{in}$ , but 7 and 8  $\mu\text{in}$ , another for 25  $\mu\text{in}$  and yet another for 30  $\mu\text{in}$ .

“These were boards spec’d instead for electroless gold,” explains Murillo. “In close consultation with Uyemura’s lab, they were manufactured to specification, using Uyemura’s AuBEL 2.” AuBEL Electroless Gold is an alkaline autocatalytic process with excellent gold wire bond properties, and a deposition rate of 80  $\mu\text{in}$  per hour.

For heavy gold ENEPIG / EPIG applications under 8  $\mu\text{in}$ , DES uses TWX-40, a reduction-assisted bath that is unique in its two distinct modes of deposition, and its “zero corrosion” performance.



*Operators racking and plating flex panels*

## Gold Rush, continued

Where traditional immersion gold exchanges with the substrate in a displacement reaction, TWX-40 deposits gold using both immersion and autocatalytic (electroless) reactions.

The autocatalytic aspect means it does not displace the substrate; it has its own driving force, and deposits gold without contribution from the base metal. TWX-40 is well documented in its ability to deposit up to 8µin of gold over palladium without compromising the underlying nickel. TWX-40 is the only immersion gold that assures compliance with IPC 4552," says Murillo.

DES worked with 3 other gold vendors in the past, changing to UIC chemistries as a solution to problems with skip plating, and to overcome objections from customers about products with a hydrochloric base, which can contaminate final finishes.

For EPIG and ENEPIG programs, TWX-40 is used with Talon 3 electroless palladium, a ground-breaking board chemistry that allows plating directly onto copper.



*Inspection of surface finish board*

Talon 3 deposits an electroless / autocatalytic palladium that is solderable and gold wire bondable. The bath has a low palladium metal content and is highly stable; the rate of deposition and quality of the deposit are consistent throughout the product's bath life. The EPIG finish produced with Talon 3 electroless palladium solders perfectly after eight hours of steam aging – a notable benchmark.

This nickel-free alternative process is widely predicted to become more consequential as lines become tighter, space more critical, and high frequency applications more common.

DES has major plans for 2020, including a return to electrolytic soft gold, a process that had been offered previously, then discontinued. DES's first priority, though, is the start-up of a plasma system to augment its desmear cleaning operation. Plasma is the most effective means to enhance interface adhesion, remove oxides and prevent micro-voids between layers during electroplating. "Also," explains Murillo, "our boards often have via holes, rather than through-holes, and the former can only use plasma. This will allow us to process vias, and holes less than 8 mil."



*Copper plating tank for via fill*

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# A New Beginning

Introducing the Printed Circuit Engineering Association.

**IN THIS COLUMN,** I share a letter from the legacy officers and board members of the IPC Designers Council, introduce the formation of the Printed Circuit Engineering Association (PCEA), and invite readers to consider future professional development and event opportunities.

## *Gratitude, Acceptance, and Future Efforts*

*To: The PCB Industry*

*From: Legacy Officers and Board Members of the IPC Designers Council*

All,

*It is with appreciation we are writing this letter to express our gratitude to have had the opportunity to serve the designers in the electronics industry through our affiliation with the IPC Designers Council. Many of us have contributed a significant amount of our careers to the betterment of our industry with this involvement. We have done so with the attitude of an educator with a servant's heart. Through all the decades of this effort, we have encountered success and challenges. We have no regrets in looking back at our efforts.*

*We are also writing to convey our acceptance that we have been summarily dissolved effective immediately, at the request of senior management at IPC. We have respectfully ceased all actions in relation to our efforts as an IPC Board. We will make all efforts to continue to represent IPC in a professional and positive manner, as professionals serving in our industry. Many of us continue to serve the IPC community in other capacities and plan to do so with excellence.*

*With our determination to continue to be involved in the electronics industry, we are informing IPC of the intentions of the Legacy Board Members, along with many others in the engineering/design community, to continue to serve the design professional. We have determined to form a new entity called the Printed Circuit Engineering Association (PCEA). In this new organization, we seek to be strong advocates of IPC and all their efforts to better the electronics industry. We will encourage all we encounter to embrace the IPC standards, along with other organizations and standards bodies in the electronics community.*

*It is our goal and hope to have a professional, cooperative relationship. We truly wish IPC continued success and seek to be professional advocates.*

*Respectfully (alphabetic order),*

*Stephen Chavez*

*Michael Creeden*

*Kelly Dack*

*Gary Ferrari*

*Richard Hartley*

*Luke Hausherr*

*Cherie Liston*

*Bob McCreight*

*Scott McCurdy*

*Susy Webb*

**STEPHEN CHAVEZ, MIT, CID+**, is a master instructor of PCB design for EPTAC, an SME in PCB design for a major aerospace corporation, and is a member of the Printed Circuit Engineering Association (PCEA); [stephen.chavez@collins.com](mailto:stephen.chavez@collins.com).



## Professional Development and Events

As we start the new year with excitement and anticipation for coming industry events regarding professional development opportunities, this section of the column will continue to list details of opportunities that will be available, such as IPC Apex Expo, the Del Mar Electronics Show, DesignCon, PCB West, PCB Carolina, Realize LIVE, AltiumLive, etc., and CID and CID+ certification courses. If you have any local or regional industry events coming up in your area and would like to announce them, please submit the details to be listed in an upcoming column. For 2020 CID and CID+ certification schedules and locations, contact EPTAC to check current dates and availability. (Dates and locations are subject to change.)

The Printed Circuit Engineering Association (PCEA) is an international network of engineers, designers, and anyone related to printed circuit development. Its mission is to promote printed circuit engineering as a profession and to encourage, facilitate, and promote the exchange of information and integration of new design concepts through communications, seminars, workshops, and professional certification through a network of local and regional PCEA association groups. □

# Preparing for Next-Gen Loss Requirements, Part 2

Can signal-integrity test vehicle results be accurately simulated?

Ed.: This is Part 2 of a three-part series on preparing for next-generation loss requirements.

HERE IN PART 2 of the series, I'll outline the means by which insertion-loss requirements are determined. In Part 3, I'll suggest a better method for obtaining more accurate Df numbers without having to go to the trouble of building test boards.

As I stated in last month's column, if you want to stay on top of the parameters that contribute to loss, there are a lot of factors to juggle. Frequency, copper weight, resin system, glass characteristics, dielectric thickness, trace width, copper roughness, and fabricator processing all contribute to the discussion if you're savvy, driving fast, with both eyes open.

Component manufacturers will typically specify a loss budget for a chipset. There are multiple server platforms, of course, but Intel's PCI Express (PCIe) trends provide a good example of the performance jumps seen across today's interconnect standards. TABLE 1 shows how PCIe speeds have changed in recent years, from PCIe 3.0 to PCIe 5.0.

TABLE 1. Intel PCI Express Speed Trends and Min. Voltage Requirements at the Receiver (V<sub>RX, min</sub>)

	Bit Rate (Gbps)	Frequency (GHz)	V <sub>RX, min</sub>
PCIe 3.0	8	4	0.013
PCIe 4.0	16	8	0.007
PCIe 5.0	32	16	0.004

It is also possible to derive the budget. The relationship for estimating an interconnect loss budget is:

$$\text{Attenuation budget (dB)} = 20 \times \log(V_{RX, \text{min}} / V_{TX, \text{min}})$$

This loss figure reveals attenuation requirements before employing pre-emphasis or equalization.

Some signal integrity software solutions include these guidelines, represented as eye masks, defining minimum and maximum "keep-out regions" for received signals. At a glance, an eye mask will show if an interconnect is acceptable from a signal-quality standpoint across many bit transitions. FIGURE 1 shows a PCI Express Gen 5.0 eye mask from Mentor's HyperLynx software. It's important to observe the inner keep-out region, represented by Top Min in the figure, correlates to the V<sub>RX, min</sub> column in Table 1. From PCIe 3.0 to 5.0, these requirements have narrowed significantly.

FIGURE 2 shows simulation results for an 8 Gbps signal over a 24" transmission line using a material that was successful on platforms that used PCIe 3.0. The loss tangent or Df for this material is 0.012. The blue keep-out region doesn't have any bits encroaching on it, which is what we want. Obviously vias, connectors and copper roughness come into play as well. This is simply intended as a high-level example of the interplay between frequency, the eye mask, and the eye diagram. Increase Df above 0.012 and bits begin encroaching on the eye mask's inner keep-out region.

Keeping with this theme, let's consider a more expensive, lower-loss material for the next-generation requirement. We'll use 16 Gbps and the PCIe 4.0 eye mask, both corresponding to Table 1. To make this work, I used a material with a Df of 0.008, and I had to change the transmission-line length to 15", which was right on the edge of what would work. The additional factors noted above must also be considered, but we've learned a few things that get us in the ballpark from a dielectric-selection standpoint. FIGURE 3 shows the result. Note the vertical scale was changed, adapting to the tighter keep-out requirements with PCIe 4.0 versus those of 3.0. The same

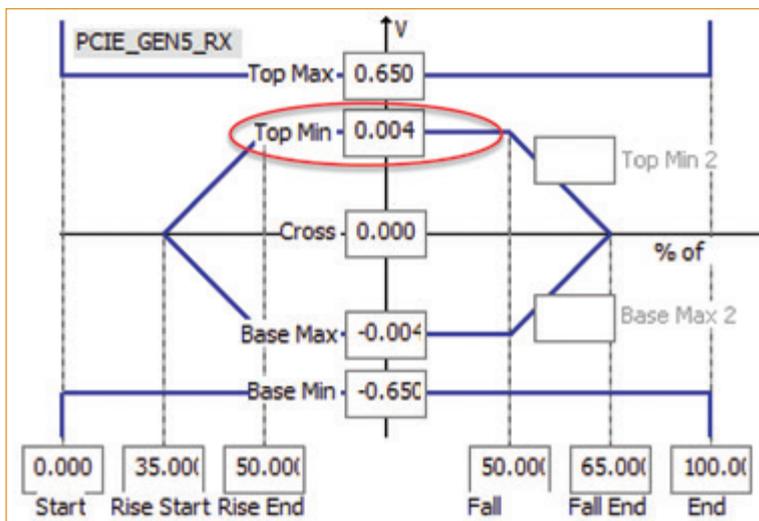
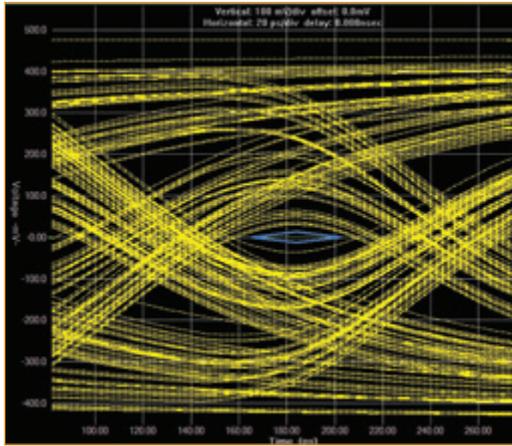


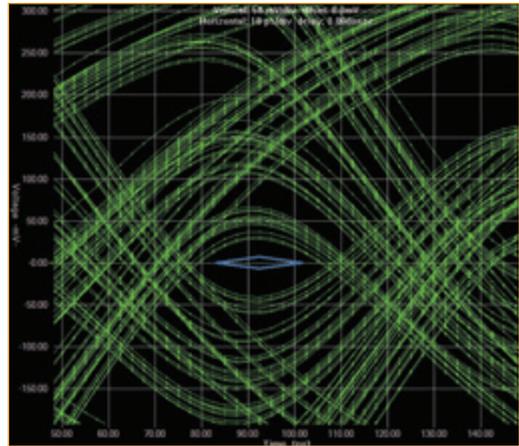
FIGURE 1. Intel PCI Express 5.0 eye mask from Mentor's HyperLynx software.

**BILL HARGIN** has more than 25 years' experience with signal-integrity software and PCB materials. He is director of everything at Z-zero (z-zero.com); billh@z-zero.com.





**FIGURE 2.** Intel PCI Express 3.0 simulation and eye mask from Mentor’s HyperLynx software.



**FIGURE 3.** Intel PCI Express 4.0 simulation and eye mask from Mentor’s HyperLynx software.

simulation exercise could be performed for PCIe 5.0 and higher frequencies, although the task of producing acceptable eye patterns at the receiver gets much tougher.

In Part 3 of this series, I’ll suggest a better method for obtaining more accurate Df numbers without having to go to the trouble of building test boards. □

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# How Does Combining Various Via Structures Affect Circuit Design?

In some cases, the designer might forego PTHs.

**AS COMPONENTS CONTINUE** to shrink, designers are challenged to find strategies to route the supporting circuit to handle all the I/O from those components while using less real estate.

The high I/O count on these devices can cause major heartburn when trying to route out from under the BGA. There is not enough room for pad traces and spaces. And at pitches under 0.8mm, in some cases you cannot route signals between the pads.

This usually drives the designer to use a combination of blind or buried vias and microvias, along with through-holes. All these are fair game in flex and rigid-flex designs. The key is to implement them in a manner that permits the various structures to coexist.

The biggest concern on parts with multiple via structures relates to how to align the different vias with the various etched layers within the circuit. Different via structures are drilled at different times with different equipment and may use different fiducials for alignment. For example, while top layer laser microvias will use layer 2 as an alignment, full layer count mechanically drilled through-holes are aligned to an average of all the internal layers in the laminated board. What if these two datums are not perfectly aligned to each other? Here is a secret: While they are perfectly aligned in the CAD data, they are not in the real-life board.

The challenge, then, is that when it comes time to image and etch the outer layers, the manufacturer must make a choice on how to align the outer image. They can align either to the microvias or the through-holes, but not both. Typically, the manufacturer will align the image to the microvias because the hole-to-pad size relationship is tighter. The assumption is that the delta between the microvias and through-holes is not so much as to cause loss of annular ring on the through-holes.

Strategies to consider:

**Provide extra allowance on plated through-hole pads.** Allowing extra pad size on the through-holes will mitigate the via to through-hole misregistration impact.

Multiple lamination cycles may drive the need for additional annular ring allowance as well. Each extra lamination cycle may in turn require an extra 0.002" of pad diameter to account for potential misregistration. The through-hole may need larger pads than a buried via in the same board.

Another consideration is the minimum hole size the supplier will drill if via fill is required. This is usually limited by aspect ratio, as well as their confidence in getting the fill material to flow through and fill a small via. Imagine when drilling at 0.008" with copper plating, the finished hole diameter may

be 0.005" or smaller, depending on plating thickness. Some suppliers may say this is too small to get the via fill epoxy to flow through the hole. This may drive them to a larger drill size (say 0.010") and may result in the need to increase pad size accordingly. Thicker boards (e.g., >0.093") may also cause the manufacturer to drill larger in order to fill a deep hole.

**Use no plated through-holes.** In designs where there are no leaded components or connectors, there is no need for plated through-holes from the top to bottom layer. Eliminating through-holes reduces concern of misalignment. These designs use buried vias, with microvias added to provide connection from top to bottom. There are no through-holes. The advantage here is alignment concerns are reduced. Designers use this strategy on "true" HDI designs.

Reconsider annular ring requirements. If a combination of different via structures is needed, including through-holes, that is fine. Ask what type of annular ring is really needed to meet reliability needs.

Do the buried vias need anything more than Class 2 (90° breakout)? There is nothing soldered in or on these holes. Class 2 annular ring may allow reduced pad size and increased routing room.

For through-holes that are just vias, ask the same thing. You may allow Class 2 annular ring on these holes, while maintaining Class 3 on holes for components like connectors.

One caution as you do this: Ensure sufficient clearance from the drilled hole wall to any adjacent copper feature. A trace too close to the drilled hole wall can create a path for a high-resistance short.

**Via-in-pad strategies.** At 0.8mm pitch and below, via-in-pad is likely necessary. There are still decisions to make, however. A combination of microvias and through vias can be used for via-in-pad. However, the through vias will have larger pads, which might not fit on smaller devices. Another option is to use only microvias for via-in-pad. This has the potential to eliminate via fill and cap plating on any of the through-hole vias. This can save money. It can also influence the minimum spacing the manufacturer can achieve due to the reduction of total plating on the external layers. Keep in mind that once you decide to use microvias on a layer, the number used is not really a cost driver.

There are ways to navigate these perplexing BGA waters. Account for the manufacturing realities of your strategy choices, and confidently route your way to a successful design. □

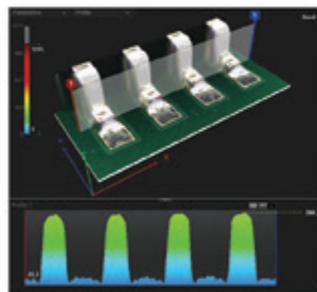
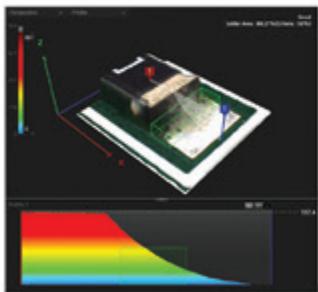
## NICK KOOP

is senior field applications engineer at TTM Technologies (ttm.com), vice chairman of the IPC Flexible Circuits Committee and co-chair of the IPC-6013 Qualification and Performance Specification for Flexible Printed Boards Subcommittee; nick.koop@ttmtech.com. He and co-"Flexpert" MARK FINSTAD (mark.finstad@flexiblecircuit.com) welcome your suggestions.





"Spectra-Tech continuously invests in the latest technology to provide the highest level of accuracy and quality of assembled products. As part of our commitment to continuous quality improvement, Spectra-Tech recently acquired a total of five (5) new MIRTEC MV-6 OMNI 3D AOI systems. After evaluating several leading 3D AOI vendors, we selected MIRTEC as the best solution to meet our ongoing quality initiatives. Our MIRTEC MV-6 OMNI AOI machines have performed extremely well! The defect detection capability has proven to be outstanding for both SMT and Through-Hole inspection. We are equally pleased with the level of customer service and after sales support." - Craig Wilson, Vice President of Spectra-Tech



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# Can PCB FABRICATION PROCESSES Keep Up with Design Demands?

New hole formation technologies and low-cost low-loss materials are needed. by STEVE PAYNE

Ed.: This is the fourth of an occasional series by the authors of the 2019 *iNEMI Roadmap*. This information is excerpted from the roadmap, available from iNEMI ([inemi.org/2019-roadmap-overview](http://inemi.org/2019-roadmap-overview)).

iNEMI's Organic PCB Roadmap summarizes the technology needs for rigid PCB, flexible circuits and optical circuits, and it includes the gaps and challenges that need to be addressed to meet the expectations of the key product groups that are driving industry demands. Successfully meeting these challenges will provide significant business opportunities for PCB fabricators.

Technology needs are divided into two major segments: research needs and development needs. Each has their challenges and opportunities.

A summary of the development needs in PCB technology include:

- Microvia technology improvement.
- Improved or new via hole formation (drilling or ablation or additive).
- Improved plating for additive fabrication and high aspect ratio blind vias.
- Continuing development of design and modeling tools for embedded actives, passives and optoelectronic PCBs.
- Improved layer alignment accuracy (improved registration).
- Finer line and space development in imaging and fabrication techniques.
- High-speed alternatives to back-drilling (e.g., additive buildup techniques).
- Continuous cycle-time reduction for rigid and flexible circuits.
- Adoption of Industry 4.0/smart manufacturing for improving traceability and enabling continuous processing lines.

**Rigid circuits.** Multiple challenges face PCB fabricators and those in the supply chain. For example, new or previously rare failure modes, such as pad cratering, are becoming more common and surface treatment of coppers to aid innerlayer adhesion in multilayer circuits can affect high-speed signal properties. These and many other challenges need to be

investigated and understood to eliminate or at least mitigate the issues. Often, collaborative research will be the most expedient way forward for the successful adoption of future technology requirements.

Use of embedded technology is predicted to increase in the next 10 years. Standard process methodology, testing methods and acceptance standards must be developed for embedding discrete and active components.

Solder mask is now used as a structural material with the adoption of underfill under the BGA. Its adhesion to the board and the need for reduced moisture absorption and permeability are critical factors, as electrical characteristics are affected. There is also a need for sub 25µm solder mask registration of features and tolerances. Ink-jetting solutions may be developed to respond to these challenges.

Measurement capability, terminology and associated specifications are needed for finer/smooth copper foils below today's low-profile copper. Copper-foil tooth reduction with increased adhesion of foil to resin is a definite need, as this will improve signal integrity. The trend for lower-loss laminates is growing, driven by high-frequency applications (e.g., 5G) and is a concern in the cost-sensitive consumer category.

**Flexible circuits.** Growing demand for "portability" fuels demand in notebook PCs, cellphones, wearables, etc. Technology considerations for flexible circuits include the following:

- Narrower spacing between conductors and thinner dielectric layers require dielectrics with higher breakdown voltage.
- High-frequency, controlled-impedance circuits, utilizing low-cost, low-Dk, process-friendly dielectric.
- Wearable and medical technologies will continue to drive adoption of stretchable flexible circuits.
- A lower-cost polyimide flex substrate or equivalent may be necessary to expand into the domain of lower-cost rigid boards.

**Optical circuits.** Laminated and embedded polymer waveguides are likely to be enablers for high-speed optical

backplane applications. Laminated optical technologies are critical to enable next-generation high-speed architectures, solving issues for high-speed and high-bandwidth signals, while preserving the cost and enabling full system integration. Optical electronics technologies are emerging continually, and we need to watch for important developments and keep an open mind.

**Research needs.** Long-term research is being undertaken by academia, research institutes and several companies in the PCB supply chain. A major challenge affecting the interconnect industry is the decline in PCB/substrate R&D investment, which does not bode well for meeting the ambitious density and cost targets defined in the roadmap chapter. Collaborative R&D must be considered as a way forward to successfully meet the challenges.

Some of these challenges include:

- Electrical test (higher throughput and more complex, physically inaccessible circuit elements).
- Dimensional consistency/stability of materials at higher assembly and use temperatures.
- Understanding the true cost/performance relationship and

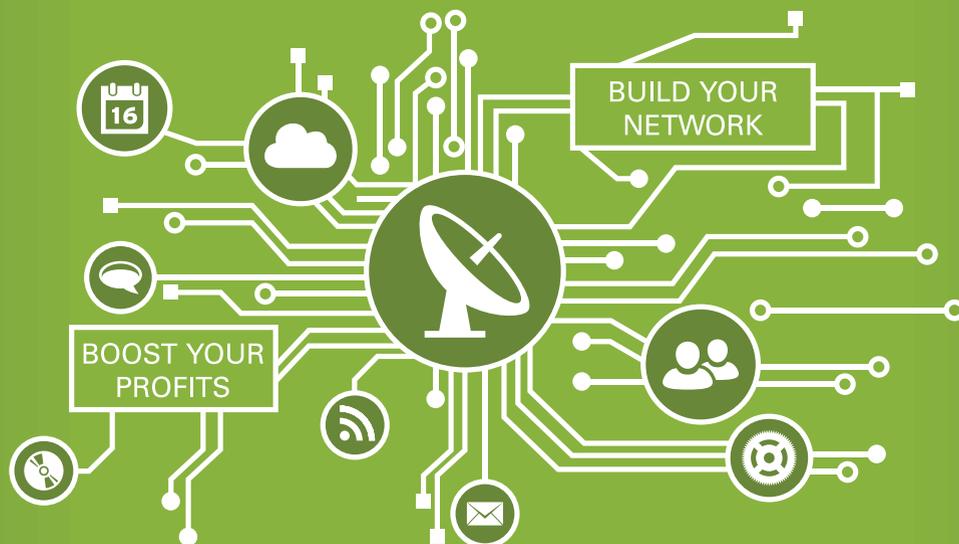
its effect on design and material choices.

- Reconciling the price inelasticity of the major product applications with sharply increasing electrical and thermal performance expectations.

The chapter concludes by describing how advanced technologies used for organic semiconductor packaging substrates are now being adapted for advanced high-density interconnect (HDI) PCBs (e.g., SLPCB). PCB fabricators must prepare for these demands driven by miniaturization and increased product functionality. Specific future product demands will drive and accelerate the development of new materials and manufacturing methods. In 10 years, we will likely be at 6G, or whatever it will be called, and artificial intelligence (AI) may be the next boundary to cross. □

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# Designing a Robust INDUSTRIAL AUGMENTED REALITY Solution

A review of tracking methodology choices to address challenges of environmental factors such as light and the prerequisite of fixed visual features. by JAY GORAJIA, NIR SAGI, ERAN NADEL and SHAI NEWMAN

The future of manufacturing will include elements of augmented reality (AR). As Pokémon GO and Ikea Place apps continue to drive awareness for AR, technology companies continue to develop solutions to solve key productivity, quality and efficiency challenges using AR. Manufacturers are looking for innovative ways to solve problems, and AR may be the key. According to an article by Cognizant, innovative companies such as Ikea, Mitsubishi, Toyota, Lego, and 10% of Fortune 500 companies have begun exploring augmented reality applications.<sup>1</sup> In addition, Gartner predicts that by 2020, 20% of large enterprises will evaluate and adopt augmented reality, virtual reality and mixed reality solutions as part of their digital transformation strategy.<sup>2,3</sup>

Augmented reality has been around for some time. However, the crossroads of visual processing power, data processing capabilities and compute power have suddenly made any mixed reality solution viable.

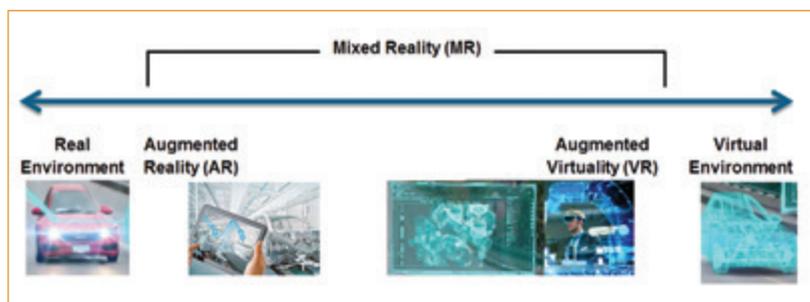
**The reality-virtuality continuum.** The notion of a reality-virtuality continuum was introduced by Paul Milgram, a professor of engineering at the University of Toronto, more than two decades ago. In a paper published in 1994,<sup>3</sup> Milgram describes the mixed reality environment as the space between the real environment and the virtual environment, as described in **FIGURE 1**.

In the manufacturing context, the far right of the spec-

trum describes what is often referred to as the digital twin of a factory, product and production, whereas the far left describes the actual factory floor with workers operating machines based on information on screens or other instruments.

Several use cases show the high impact augmented reality has on manufacturing. These use cases include assembly instructions and validation of complex assembly, asset maintenance instructions, expert remote instructions and support, programming and commissioning validation, and real-time quality processing and visualization.

Most use cases in manufacturing today seem to focus on integrating AR at the actual production line, where it's most feasible to link actual machinery, robots, parts, and 3-D graphic models. Some of these use cases include helping a shop floor worker identify the next part to assemble in the assembly sequence (**FIGURE 2**), validating a robotic program using an AR-generated part, instead of an actual part, and overlaying the 3-D model on top of the actual part for quality inspection purposes (as-planned vs. as-built scenario). When reviewing use-cases throughout the product lifecycle (**FIGURE 3**), it is clear the use cases relevant for AR technology are the



**FIGURE 1.** The reality-virtuality (RV) continuum.



**FIGURE 2.** Demo on an airplane nose (One Aviation) from the Hannover Messe trade show in 2018.

ones further down the cycle, where the digital twin – the virtual model of the product – can interact with the real production line and related products.

Model-based work instructions, leveraging the design and assembly process data within managed data structures, could easily clarify an assembly process for the shop-floor worker by overlaying the actual design data 3-D model on top of the actual, current assembly structure, thus shortening process cycle time and reducing human error. Such an AR model-based work instruction solution has another significant benefit: It resides within the automation which comes with model-based work instructions, as the CAD model and the process sequence are all byproducts of work done in earlier stages of the product lifecycle and can be leveraged. Such a solution should obviate the need to manually create and update documents as part of the work instruction authoring process. It also speeds up onboarding processes, as it makes the work instruction product more intuitive.

Another relevant use case that addresses production assembly planning validation includes an AR part precisely

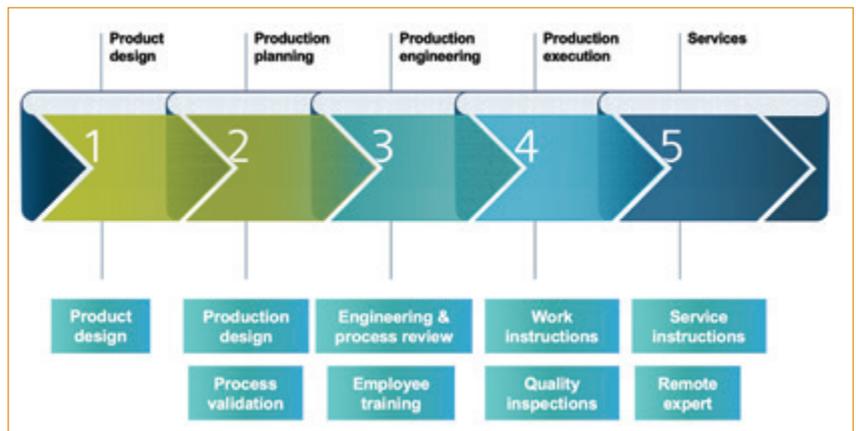


FIGURE 3. Siemens' holistic product design-through-manufacturing value chain.

mounted on a fixture at the real production line to validate a welding operation program written directly to the robot controller, hence saving time and money on manufacturing a real prototype, which, in addition to its costs and manufacturing time, might not comply with common standards.

Training shop floor workers on assembly procedures is an AR use case that could accelerate new employees' learning curves and save valuable time for experienced employees who currently must mentor the new ones. For quality issues and validation, AR can be used to validate part manufactur-

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ing and assembly structures in an as-planned vs. as-built scenario, where an employee compares the physical product and digital twin which overlays it for quality purposes.

To address the use cases described above, a scalable, robust solution must be designed that includes accurate and reliable tracking. Tracking is how the augmented reality algorithm recognizes real-world objects, so it can accurately place virtual objects onto it. Most common commercial solutions that perform tracking today, such as ARCore by Google, ARKit by Apple and Vuforia’s eponymous system, utilize vision algorithms that inspect visual features in the incoming image stream of the actual object to determine the exact position to place the 3-D model. These solutions allow flexibility and simplicity during setup but are sensitive to environmental factors such as light variances and line of sight, and require clear, high-detailed features to the scanned object to gain high accuracy.

This article describes the design and implementation of a robust industrial augmented reality assembly instruction and validation solution in which various choices of AR and tracking methodology are reviewed to address challenges of environmental factors and the prerequisite for visual features in the environment. In addition, the solution “validates” that a manual operation was performed, which is key to ensuring a robust solution. Simply providing instructions is not enough for critical manufacturing needs. This solution is being tested in an actual production line for gas-insulated switchgear at the Siemens gas and power factory in Berlin, Germany.

**Technology Overview**

**Key technologies.** Current AR solutions are based on two main factors: the type of camera used and the analysis of visual features within the camera feed. The main demand of such AR solutions is they require an environment with sufficient differentiating visual features, defined as “trackers.” These visual features are identified by computer vision-based algorithms which calculate the camera’s location relative to the physical environment and enable augmenting virtual objects over the camera feed of the target physical object to generate the AR effect.

As clear visual features are not always available in the physical environment, use of visual stickers, also known as “markers,” enrich the environment for optimal detection if placed accurately onsite next to the target object to track.

Other popular solutions in use today by the AR market include embedded 3-D cameras, which indicate depth

between the camera and target object (for instance, as integrated in Microsoft’s HoloLens head-mounted wearable), which improves the tracking mechanism by adding a 3-D mapping layer. Another possible solution for accurate AR involves an array of cameras that track physical objects by means of attached visual trackers (usually IR reflective spheres), and then locate the position of these objects via computer vision algorithms that process these images as generated by the array of accurately calibrated cameras, in real time.

An important differentiation regarding AR implementations is the user interface perspective, as current AR developments are divided into two major categories: wearable, head-mounted devices and mobile devices. Some major OEMs (Microsoft, Magic Leap) are developing and customizing hardware devices that aspire to achieve transparency on the user’s mixed-reality experience. Others (Google, Apple) focus on their own software development kits, intended for developers creating the AR applications, and focus on the experience on mobile devices.

**Challenges.** One of the key challenges to developing an augmented reality solution for industrial applications is a majority of industrial environments (e.g., a fuselage of an airplane) lack clear visual features on all surfaces, limiting the use of AR to the regions where the visual features are clear and visible. Further, such solutions create a prerequisite for good lighting conditions in industrial environments, and many times are sensitive to variation between the actual part(s) and the 3-D representation in scale, color, etc.

Use of visual stickers as markers to enhance the visual features in an industrial environment requires excessive preparation work, is prone to user errors and inaccuracy, and is only a partial solution, as it is not always possible to get full coverage utilizing this technique. One of the key benefits to an integrated solution is to overcome data revision issues. Using visual stickers would not solve that problem.

Use of 3-D cameras to attempt to map an area and provide a better feed to an AR solution is also a partial solution, as there are use cases where the target environment is covered with uniform surfaces where it’s impossible to differentiate between surfaces based on depth information.

Using an array of cameras is also limited, as it is expensive, requires complicated calibration between devices, adds substantial infrastructure and hardware to the setup, and can create security and layout issues.

**TABLE 1.** AR Software Technology Comparison

	Marker/3-D Model-Based	Trackerless	2-D+3-D Cameras	PointAR (Patented)
Main vendors	Vuforia	ARCore/ARKit	Hololens	Compedia
Positioning method	Computer vision	Computer vision	Computer vision and 3-D data	Computer vision and laser sensors
Accuracy	Low to high (depends on visuals)	Low	Medium	High
Robustness	Low to medium	Low	Medium	High

The reasons provided above are currently preventing commercial AR solutions based on visual features, markers, and high-end cameras from instantly becoming widely used by manufacturers around the world.

When referring to industrial shop-floor use cases, it's also important to address the most-suitable hardware devices to use. Wearable devices that give the user an intuitive, hands-free experience also have their limitations. The most significant limitation is the reluctance of workers on the shop floor to put these devices on their heads for long periods of time, as required in production line use cases. They tend to also limit field-of-view, and the related orientation issues that have been identified by many tests further add health concerns.

There are many challenges to existing AR solutions, and a new approach is needed.

## Solution Design

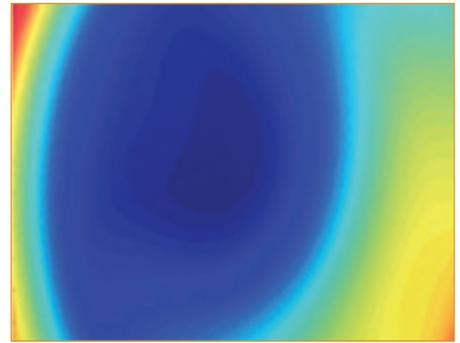
**Analysis and technology decisions.** After performing an in-depth feasibility study focusing on specific production, shop floor use cases, and AR implementations in manufacturing environments, it was concluded the limitations of existing AR solutions as described earlier have dictated the need for a new technology.

All those efforts eventually led to development of a new technology we call "PointAR." We have identified a new generation of low-cost, low-energy laser lighthouses and related sensors developed in the virtual reality (VR) industry. However, we found no complementing off-the-shelf software. The reason is tracking on VR headsets does not require absolute accuracy but rather consistency and continuity. (Namely, it is not important if the absolute position is not accurate, provided the change in movement is consistent). On the contrary, a robust AR solution for manufacturing requires absolute accuracy as it relates with real objects in the physical environment. Further calculations and experiments demonstrated fusing computer vision algorithms for absolute accuracy-oriented algorithms can use the same VR Lighthouse hardware, while generating good results 7m from the lighthouse and 4m from the target object. This new technology enables an AR solution based on computer vision algorithms fused with laser lighthouses and inertia sensors that are reliable and cheap.

**Solution architecture.** As a prerequisite for a robust AR solution for manufacturing, the data source must consist of precise CAD data, 3-D models and metadata, which describe additional information on the given process. An enterprise data management solution to manage electronic CAD (ECAD), mechanical CAD (MCAD), process information, and metadata related to dependencies to process is recom-



**FIGURE 4.** A PointAR unit equipped with IR-based sensors for tracking and a standard Logitech 4k web camera.



**FIGURE 5.** AR accuracy mapping. The image represents the system accuracy in different positions of the camera feed. Blue colors indicate the accuracy is better than 1mm (from distance of 2m of tracked object). Green and bright yellow colors indicate accuracies of 1 to 2mm (from 2m).

mended. This is typically performed at many manufacturers and technology companies by implementing a strong connection to the product lifecycle management (PLM) system. The PLM system may act as a tool to create, store, author, and configure the data that are later loaded in the AR solution.

The 3-D models materialize via CAD software and dedicated CAD libraries stored in the PLM database in the early product design and production planning phases. Additional metadata related to the production process are added in the




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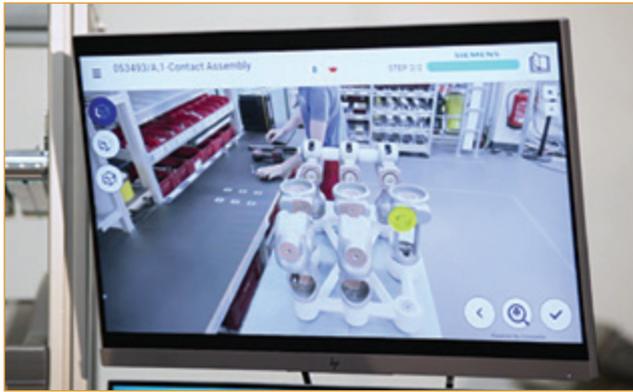



production planning and engineering phases, before dedicated plugins output the data from the PLM to the AR solution. The PLM software acts as a configuration management system that ensures transparency between the latest datasets and the AR visualization software.

When designing an AR solution for manufacturing, consider the following components:

- A hardware component that reports the exact location of the camera (mandatory) and optionally other components



**FIGURE 6.** Precise AR image placement (CAD model emphasized in yellow) on complex assembly procedures.



**FIGURE 7.** An AR-enhanced work instruction solution for an assembly station at the Siemens Gas and Power factory, gas-insulated switchgear manufacturing line in Berlin.



**FIGURE 8.** The AssistAR AR-enhanced work instructions solution, shown at Realize Live in June 2019 in Detroit.

in the environment;

- An interface mechanism that translates and transmits the hardware output to the software layer;
- A software layer that utilizes the location information to apply the AR layer on top of the camera feed, reads and parses the data package exported from the PLM, and loads the application layer with according user interface for the user.

The AR system described should be agnostic to the hardware component used to retrieve the location of the camera and other components in the environment. This provides flexibility for the manufacturer to acquire hardware that may be more relevant, cost-efficient and optimally performing for their manufacturing environment. Tracking is performed by connecting a tracker to the camera via dedicated mounting device so the camera's movement is aligned with the tracker as one complete unit (**FIGURE 4**). Additional trackers can be connected to other physical objects in the environment to track their movement; for instance, a tracker can be placed on a fixture in the assembly station to track its movement and maintain the AR experience.

A unique calibration process is performed per each Point AR unit to precisely output the offset among the tracker, the camera and the connecting unit's tip. This calibration process is essential to accurately overlay the 3-D model on top of the actual part, as part of an initial positioning method. On initial launch of the AR application, a simple positioning process needs to be performed where predefined points selected on the 3-D model are matched with a recording of points generated by the user who physically identified these points on the actual object via the PointAR unit's end tip. This process aligns the coordinate system of the real world with the coordinate system of the 3-D model and permits free movement of the camera along with other, tracked objects in the environment, without damaging the AR tracking experience.

**Test methodology.** The challenge during development and fortifying the AR solution was defining how to implement accurate AR in real time with low latency. For this, we developed proprietary GPU-based algorithms to ensure the required accuracy and performance can be achieved.

Accuracy was tested by supporting zoom and enabling the user to "move" the 3-D overlay image on the projection plan to reach full accuracy. The physical length in the real world of this "correction" movement can be calculated and then used to define the AR accuracy. In many use cases, we have achieved 1 to 2mm of AR accuracy in real time, while using low-priced sensors and a standard PC.

## Results

A proof-of-concept pilot of the Siemens PointAR solution has been launched at Siemens Gas and Power division. The project consisted of equipping three manual assembly stations with a full hardware and software solution for work instructions in the shop floor (**FIGURE 7**). The main motivation for such a solution came from the need of this newly built manufacturing line to quickly ramp up in production and

accelerate the learning curve of the precise assembly process to new employees, without using experienced employees for supervision and guidance.

As the AR solution is agnostic to the specific sensors, we are now evaluating different sensors for different use cases and requirements. We are also looking for new use cases and identify new ones almost every week.

Future planned software updates will include a more fitted user experience, enabling alignment with suitable wearable devices as they evolve, connectivity with IoT devices on the shop floor such as Atlas Copco's smart tools, and improved algorithms for supporting tracking accuracy.

From a business perspective, as the AR-enhanced work instructions solution is now officially part of the Siemens Industry Software portfolio (FIGURE 8), it is most important to validate other AR use-cases and leverage our developed infrastructure to provide accurate AR technology throughout various scenarios with good ROI within the shop floor.

"The AR solution's data source must consist of precise CAD data, 3-D models and metadata."

### Summary

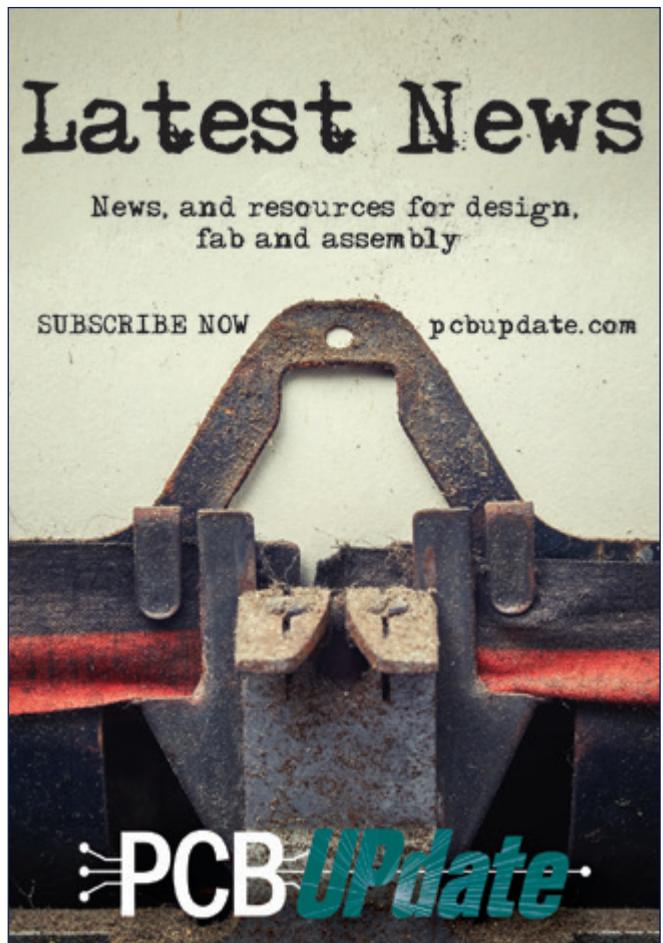
The article described AR for manufacturing use cases, challenges with current popular technologies and how we had to develop a new approach in order to implement a robust industrial augmented reality assembly instruction and validation solution. We reviewed various choices of tracking methodology and developed a unique hybrid computer vision and sensor-based solution to achieve an accurate image overlay. This new AR for manufacturing, PointAR, yielded a robust solution with 0.5 to 2mm absolute position accuracy and 0.05° to 0.2° of angular accuracy (depending on sensors, setting and range). The solution also overcame challenges of environmental factors, the prerequisite to have scanned objects in the environment, and is not affected by lighting or background. In addition, the solution is sufficiently accurate to "validate" a manual operation was performed, which is key to ensuring a robust solution. Simply providing instructions is not enough for critical manufacturing needs. We completed successful initial tests, and the AR solution continues to be tested in an actual production line, including at the Siemens Gas and Power factory in Berlin, with others to join. □

### REFERENCES

1. Cognizant, "Building the Business Case for Augmented Reality," Jun. 19, 2018, [cognizant.com/perspectives/building-the-business-case-for-augmented-reality](https://www.cognizant.com/perspectives/building-the-business-case-for-augmented-reality).
2. Bryan Griffen, "Augmented Reality and the Smart Factory," Augmented Reality and the Smart Factory, Apr. 12, 2019, [manufacturing.net/article/2019/04/augmented-reality-and-smart-factory](https://www.manufacturing.net/article/2019/04/augmented-reality-and-smart-factory).
3. Shanhong Liu, "Global Augmented Reality Market Size 2025," Statista, Aug. 17, 2018, [statista.com/statistics/897587/world-augmented-reality-market-value](https://www.statista.com/statistics/897587/world-augmented-reality-market-value).
4. P. Milgram, H. Takemura, A. Utsumi and F. Kishino, "Augmented Reality: A class of Displays on the Reality-Virtuality Continuum," *Telemanipulator and Telepresence Technologies*, SPIE, 1995.

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# An Automated TIN WHISKER RISK ASSESSMENT Process Resulting in Significant Cost Savings

How a modified design tool automated and standardized TWRA measurement. by KAREN EBNER, ROBERT DEMEO, JANET VILLIERS, ANDREW GOOSSENS, DANIEL MANTONI and LENNA MCCARTHY

The European RoHS Directive mandated that by July 2006, lead would be removed from electronics assemblies. In response, the electronics industry introduced more lead-free components into the supply chain. US military and medical device companies were exempt from this legislation. This exemption is rapidly changing.

Tin-lead parts obsolescence has become an acquisition issue for the military. The risk is alternative RoHS-compliant parts typically substitute pure tin for traditional tin-lead finishes. Pure tin can grow electrically conductive whiskers that may dislodge or short, causing failure (FIGURE 1). To mitigate the risk, the company developed a tin whisker risk mitigation policy that requires hardware programs to develop and implement a tin whisker mitigation plan.

Performing tin whisker risk assessments has become a schedule-driving, labor-intensive process. The engineering team's vision was to develop and implement an automated tin whisker risk assessment (TWRA) process that would reduce manual work and save program cost and schedule.

Engineering worked with the printed wiring board design group to automate the TWRA process using a new approach and evaluated 12 new printed circuit board assemblies using the new process. The average measurement time was reduced approximately 97% per PCB. Furthermore, engineering archived each PCB analysis in a common data management system, allowing easy access for future leveraged designs.

Over a 12-month period, Raytheon business units released

a large number of new PCB designs. If this new automated measurement system is employed throughout the company, the potential savings is significant.

## Conventional Approach

In the past only a few components were manufactured with only a pure tin finish option and no option for tin-lead plating. Tin-lead component finishes were readily available. Therefore, only a few components required tin whisker risk mitigation. As the RoHS legislation went into effect in July 2006, more component manufacturers transitioned to a RoHS finish (e.g., nickel palladium gold, pure tin, or gold finish), tin being the prevalent option. Companies that had high reliability requirements (aerospace, military, medical) had to spend more time evaluating tin whisker risk in their designs, resulting in increased cost.

Engineering must evaluate each component in the bill of materials for contact finish type. Each component type can be seated in multiple locations on a PCB. If the component is a pure tin finish, a tin whisker risk evaluation is required for every component instance. A key risk factor in the tin whisker risk evaluation is the conductor gap spacing between adjacent components and the component lead spacing itself. The smallest gap spacing measurement identified at each component instance is used as a risk factor dimension in the TWRA to determine the component instance's risk score. Multiple measurements might be necessary for each component location to determine the smallest gap spacing.



FIGURE 1. Tin whiskers growing from a transistor assembly (images courtesy of NASA).

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Note the TWRA is not just evaluating component lead spacing. It is also critical to measure the spacing of the adjacent components to determine the complete tin whisker risk. Based on historical data, it can take significant engineering labor resources to complete this task on a densely populated PCB, and to produce new artifacts. This analysis is time-intensive, and it is imperative the data generated from the evaluation be archived in a central repository for access and reuse in future analysis.

### TWRA Algorithm

The engineering team proposed an innovative solution of automating the conductor gap spacing measurement process to reduce costs and reduce schedule impact. The TWRA algorithm requires a conductor gap spacing. A key part of this conductor spacing risk factor is the minimum line of sight gap between a tin-coated surface and the nearest conductor (FIGURE 2). Each tin-coated component instance can have multiple components next to it, which must be measured. The smaller the gap, the higher the risk. Manually gathering these measurements is an enormous task to complete on a PCB assembly, where the average number of component instances may be greater than 1,000, each requiring measurement to an adjacent conductor.

The engineering team already utilized design tools that automate inspection, producibility and tolerance validation for the physical PCB. Engineers use these tools to ensure the assembly of the PCB, and physical layout rules meet specific standards prior to prototype. This process improves assembly yield and reduces labor content. This process capability is critical to assess component gap spacing between a tin-coated surface and any other nearby conductor surface.

The value of these tools' performance capability and potential cost reduction was recognized, if these tools could be modified to assess component lead spacing to adjacent conductive components, as needed for the TWRA. The team considered use of one of the design tools that could be automated specifically to measure component gap spacing from lead-to-lead of adjacent components (FIGURE 3). Engineering establishes rules in the design tool. Then the tool checks components, pad stack-ups, pin-to-pad, test points and solder point analysis against product requirements. These design rules are configured against product requirements and guidelines established by manufacturing capabilities and component requirements. Engineering previously had not utilized the process/tool to measure adjacent component lead spacing needed in TWRA.

Understanding required process requirements, the engineers modified the design tool software and process. Design rules were developed to identify lead spacing on

PCBs, from lead to adjacent lead where a TWRA failure will occur under worst-case conditions for Level 2B, in accordance with the Tin Whisker Guidelines and GEIA-STD-0005-2.

Engineering created an output report from the new process (FIGURE 4) that shows any component spacing measurements that failed the design rule. The output report lists:

- ID number
- Component type
- Out-of-specification dimension
- Image of location of a failure
- Reference designators of the two adjacent components.

Engineering can review the data and assess the need for additional TWRA. Engineering can determine if plating materials and self-mitigation considerations are valid and can remove the component risk. Hardware engineering now had a possible solution to automate the TWRA at a reduced labor effort.

### Results

Hardware engineering used this tool with the newly configured rules to evaluate nine PCBs for a program. In addition, three other program PCB designs were evaluated using the new TWRA process. A total of 12 PCB assemblies were evaluated using this automated method for TWRA measurement.

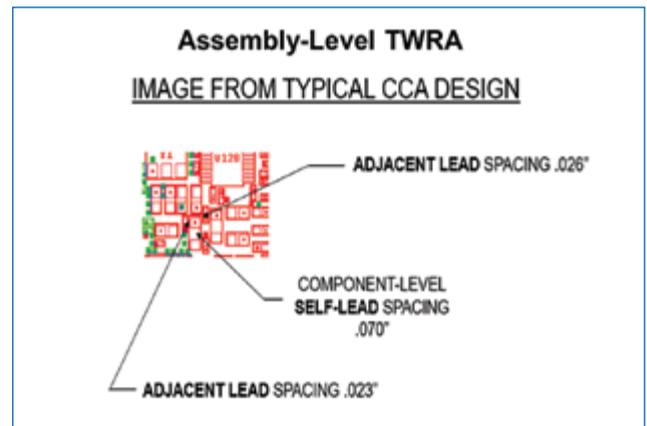


FIGURE 2. Assembly-level TWRA.

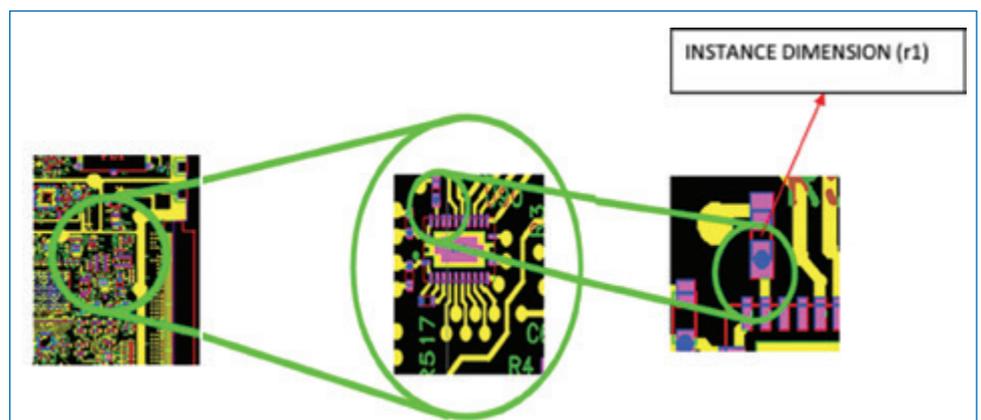


FIGURE 3. PCB CAD software was modified to measure component gap spacing from lead-to-lead of adjacent components.

Sharelist report of job pwb0550643-tin-whisker				
ID	Chk-Category	Value-Found(*)	Image	Refdes
1	Comp_Spacing_Accrete201_Accrete201_an	0.04660		C656,C657
2	Comp_Spacing_Accrete201_Accrete201_an	0.08810		C673,C674

FIGURE 4. Example of chosen headers from Sharelist report.

Based on a historical average, a large fraction of the component instances on the assembly is tin-coated and requires analysis. Some components are known to be dimensionally self-mitigating; i.e., based on dimensions and locations of leads and pad terminations, they are found to be sufficiently small enough to become completely coated with lead-bearing solder during standard PCB reflow soldering.

The tool automated the measurement process between each tin-finished component instance and its adjacent components. This new process is a major time-saver for the component measurement part of the TWRA at the assembly level.

Engineering's estimate of time and schedule to perform TWRAs using the manual process was unacceptable to meet program cost and schedule goals. Therefore, the new automated measurement process was implemented. Using the reconfigured engineering design tool, spacing data for the 12 assemblies were assessed with significant rapidity. The average time reduction per PCB assembly for the measurement task was reduced 97%. The measurement process eliminated full analysis on most of the components, resulting in only a few components requiring a full factor analysis in the TWRA algorithm. This process change significantly benefited the time for this measurement effort.

An additional benefit is the TWRA output for the entire PCB assembly can be archived by part number as a general document in the data management repository. This repository meets company and customer record management standards. A centralized repository permits easy retrieval for assessment data and work product traceability that support best practices and future rework abilities.

Engineering estimated a significant labor savings of an average 97% measurement time reduction per PCB across businesses, and schedule impact is far reduced. Because the analysis can be performed real-time during the design phase of the board, multiple TWRA preliminary runs can be made in time to give useful feedback to optimize PCB layout, without affecting program cost and schedule.

## Tool Implementation

Internal company training on this TWRA tool was held across the businesses in July 2019. This training was held in collaboration with the Lead-Free Tin Whisker Technical Interest Group. Individuals who attended the training became the trainers at each of the businesses. Hardware engineering created a TWRA Automated Measurement Job Aid that was used for TWRA enterprise training. The vision is to supplement training with an easily accessible job aid that documents the process for use across all internal businesses. The TWRA Job Aid has been loaded and approved in the data

management system for the whole business to utilize to support their TWRA.

The job aid explains to the user how to generate a TWRA report that identifies components requiring additional analysis after failing the rule for TWRA Level 2B or the rule for TWRA Level 2C, in accordance with GEIA-STD-0005-2. The report highlights the failed component's location and reference designator. Any self-mitigating components in the report are noted per Tin Whisker Mitigation Guidelines.

Once TWRA is completed, the tool generates a report listing all potential failure sites. The report allows an analyst to focus on components that require additional evaluation and provides critical information such as their locations. Engineering can ignore small components that satisfy the self-mitigation run rules, leaving only a few components to manually evaluate.

All artifacts from the resulting TWRA are collected in a zipped folder. These artifacts include:

- A list of all components on the assembly with information from parts list and vendor part number
- A copy of each required tin whisker algorithm
- A copy of each required gold/palladium embrittlement algorithm
- The TWRA output report
- A summary page, including recommended corrective actions.

Once all artifacts are collected, a general document will be created in the data management tool, and the zipped folder will be attached. The method for archiving the TWRA report includes adopting a naming convention to facilitate retrieval of existing reports. Instead of searching and recording the generated formal document number, a search can be done using the relevant assembly number for easy retrieval.

## Next Steps

After training on use of the new tool, scheduling more frequent preliminary TWRA assessments upfront during the design would mitigate the need for redesign after PCBs are manufactured. Engineering could identify these risks early on and modify the design to mitigate any manufacturing issues. This upfront analysis will increase profit by eliminating excess engineering rework, minimize costs of any mistakes and improve reliability. Programs will need this process automation even more when the industry loses its tin-lead exemption.

The next phase of this project will be to merge the output from these assessments with a component database where company part data currently reside. The tool also contains information related to key factors needed for the TWRA. Merging these data will build a system that all engineers can use and share information across all the businesses. Engineering in collaboration with other businesses is looking to assess the work involved

in joining the two processes. This merger will reduce time seeking information for the other risk mitigation factors that are specific to the component and can be reused in other designs.

## Conclusions

An automated TWRA measurement process was developed using an engineering design tool. This tool use resulted in a 97% measurement time reduction per PCB and a potential significant cost savings across the enterprise in a one-year period.

Using the tool in this manner was an innovative solution that can permit TWRA during PCB layout and manufacturing pre-build review. Using Six Sigma practices, engineering can estimate annualized cost avoidance and assign to prioritize design change decisions. This will address tin whisker risk concerns early in the design process and address any potential reliability issues.

This new process not only saves cost and schedule but provides a document that is ready to archive in an approved repository that is easily accessible for future revision changes.

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## REFERENCES

1. D. Pinsky, "Tin Whisker Application Specific Risk Assessment Algorithm," Proceedings of the 2003 Military & Aerospace/Avionics COTS Conference, August 2003.
2. D. Pinsky and E. Lambert, "Tin Whisker Risk Mitigation for High-Reliability Systems Integrators and Designers," Proceedings of the IPC/JEDEC 5th International Conference on Lead Free Electronic Components and Assemblies, March 2004.
3. D. Pinsky, "Enhancements to Current Tin Whisker Risk Assessment Methods," Proceedings of the IPC/JEDEC 11th International Conference on Lead Free Electronic Components and Assemblies, December 2005.
4. D. Pinsky, "An Updated Application-Specific Tin Whisker Risk Assessment Algorithm, and Its Use within a Process Compliant to GEIA-STD-0005-2," raytheon.com.
5. Tin whisker photo examples, digital photos, courtesy of NASA.

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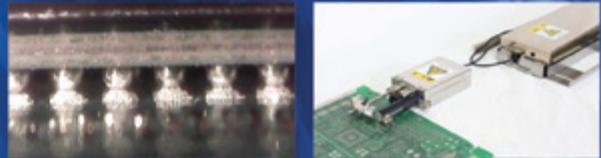


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# Sn-Bi LOW-TEMPERATURE HOMOGENEOUS SOLDER Joint Microstructure, Reliability and Failure Mechanism

How do LTS solders perform under thermal cycling and drop-shock testing? by NILESH BADWE, KEVIN BYRD, OU JIN and PUBUDU GOONETILLEKE

Several environmental, technology and reliability factors have recently combined to renew interest in the use of tin-bismuth-based solder alloys for motherboard manufacturing. Corporate and government initiatives to reduce greenhouse gas emissions benefit from reduced electricity usage afforded by use of low-temperature solders. Thin electronic components and motherboards experience less warpage at the lower peak reflow temperatures, enabling pitch and form factor scaling, driving technology innovation. A new generation of tin-bismuth solder alloys engineered for increased ductility is enabling SAC BGA-LTS SMT solder joints to meet board-level reliability requirements.

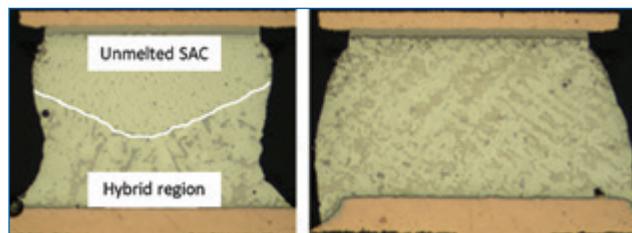
Tin-bismuth (SnBi)-based low-temperature solders (LTS) can be used to create solder joints both when used in conjunction with an electronic package using tin-silver-copper (SAC) solder spheres or a SnBi-based solder sphere. In the case of a SAC-LTS solder joint, the resulting structure is referred to as “hybrid.” For an LTS-LTS solder joint, the structure is referred to as homogenous. **FIGURE 1** illustrates the structure of each case.

When working with hybrid solder joints, it is necessary to consider the ratio of theoretical solder paste volume being printed to the volume of the unmounted BGA sphere used on the component. This is referred to as the paste:ball volume ratio. **TABLE 1** illustrates the calculation of the paste:ball volume ratio.

**FIGURE 2** illustrates the change in solder joint fatigue performance as the paste:ball volume ratio is modulated. **FIGURE 3** shows the typical crack locations and crack types (T1 to T4). A ratio of 0.5 has been repeatedly demonstrated to optimize the solder joint reliability performance.<sup>1</sup> If the ratio is significantly below 0.5, solder joint quality may degrade, leading to all PCB side cracks (T3). A ratio significantly greater than 0.5 may result in small concentrations of bismuth reaching the ball-to-package interface. In the SnBi system, Bi weight percent of 5 to 12% results in significant reductions of elongation<sup>2</sup>, and this behavior is believed to result in low-cycle, brittle package side failures (T2 cracks) for components built with the excessive paste:ball volume ratio.

For a homogenous solder joint, the Bi is uniformly distributed throughout the joint and the need to control paste:ball volume ratio when designing the SMT process eliminated. By considering the Bi content of the solder sphere and the solder paste, final metallurgy can be achieved that optimizes the elongation performance (**FIGURE 4**). The paste:ball volume ratio provides an additional process window to modify solder volumes to address warpage or other component requirements necessary to achieve maximum process yields.

Previous investigations have shown hybrid SAC-LTS solder joints formed with eutectic SnBi solders can show reduced



**FIGURE 1.** Cross-sectional image of a SAC-LTS hybrid joint (left) and a homogenous LTS joint (right).

**TABLE 1.** Solder Paste Volume to BGA Ball Volume Ratio Calculation

	mil	mm
BGA sphere diameter	10	0.254
BGA sphere volume (unit <sup>3</sup> )	524	0.0086
Desired Paste:BGA sphere volume ratio	0.5	0.5
Required solder paste volume (unit <sup>3</sup> )	262	0.0043
Stencil thickness	4	0.102
Round aperture = $2 \cdot \sqrt{\text{paste volume} / (\text{stencil thickness} \cdot \pi)}$	9.1	0.232
Square aperture = $\sqrt{\text{paste volume} / \text{stencil thickness}}$	8	0.205

mechanical drop capability compared with homogenous SAC solder joints.<sup>3</sup> Sn-Bi solders modified with additional doping elements that increase the material ductility demonstrate improved mechanical characteristics.<sup>4</sup> It is postulated some portion of the reduced performance of the hybrid SAC-LTS solder joint results from poor control of Bi mixing in the solder joint and small concentrations of Bi at the package side interface, significantly reducing elongation of the solder joint. Tighter control of Bi mixing during solder joint formation or a homogenous LTS solder joint optimized for elongation is expected to show improved mechanical drop capability.

A homogenous LTS solder joint can effectively eliminate a solder joint quality defect referred to as “hot tearing.” In a non-eutectic solder system, during cooling the solder will solidify over a range of temperatures. As the package returns to the room temperature shape, the dynamic warpage creates stress on the solder joints. If the solder joints are not fully solidified during this period, the joint can tear, which creates a crack-like signature post-SMT and may pose a risk to solder joint reliability. For a hybrid joint, this risk is increased by the lack of solder joint collapse during reflow. As the SAC solder ball does not fully melt, the unmelted portion of the joint acts

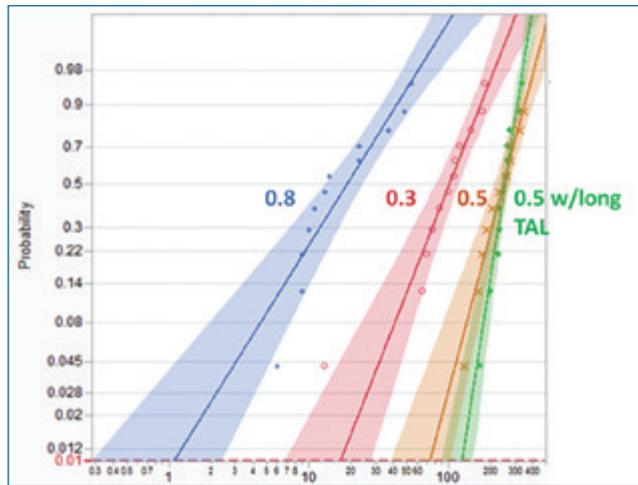


FIGURE 2. Thermal cycle reliability Weibull for different solder paste to BGA ball volume ratios (0.3 to 0.8).<sup>1</sup>

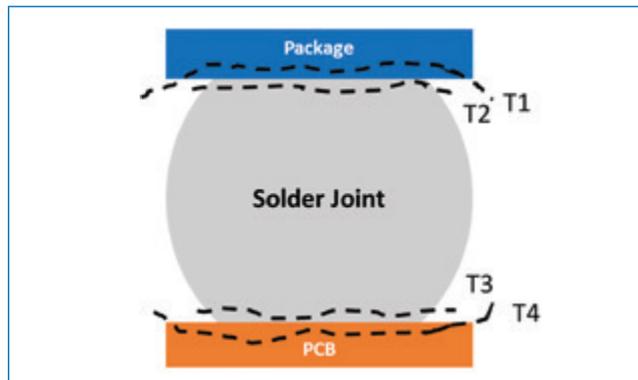


FIGURE 3. Crack types at different interfaces for a solder joint (T1 – T4) annotated.

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as a standoff and prevents full collapse. Figure 4 shows the difference in post-reflow standoff height of a hybrid solder joint compared with a homogenous solder joint.

Details about hot tearing defects and process knobs to mitigate those in hybrid joints are discussed in a companion proceeding.<sup>5</sup> The homogenous solder joint melts completely and creates a full collapse, which has been shown to help eliminate the occurrence of hot tearing (FIGURE 5) and provides a much wider process window.

Given the advantages of homogeneous LTS joints for SMT processing, we examine differences in solder joint morphology between hybrid SAC-LTS solder joints and full LTS solder joints. Post-reflow compositions for different combinations of ball-and-paste metallurgy will be detailed. Finally, component-level reliability performance and failure mechanisms will be compared between SAC-LTS hybrid and full LTS second-level interconnects using different package form-factors.

**Experimental Methods**

**Materials.** Two different solder paste materials (referred to as paste A and paste B here) were used for the study. These materials used different flux formulations, as well as different SnBi-based LTS alloys. The Bi compositions of the alloys in paste A and paste B are 50% and 58% by weight, respectively, along with supplier proprietary dopant elements to enhance reliability of the materials. Melting behavior of the alloys was studied through differential scanning calorimetry (DSC) using TA modu-

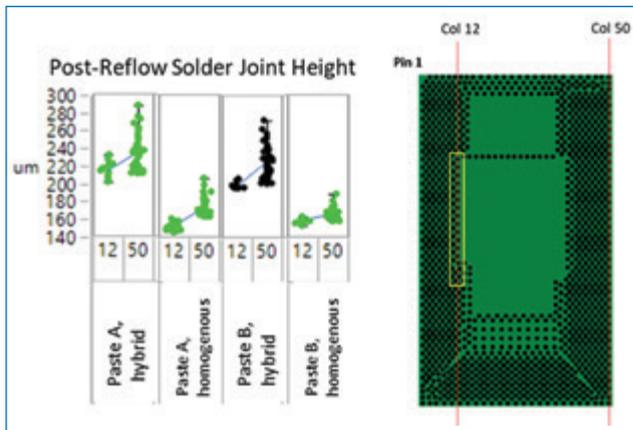
lated DSC model Q1000. DSC testing used ~10g of paste, which was heated from 25° to 240°C at a ramp rate of 10°C/min. Melting onset, peak and end-of-melting temperatures were recorded.

**Thermal cycle reliability: BGA assembly and testing details.**

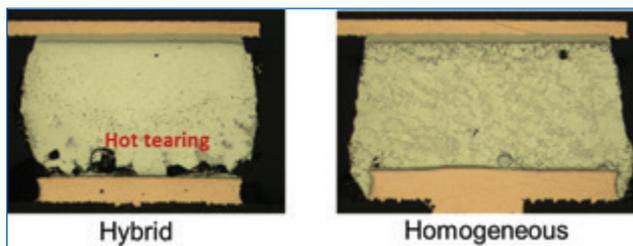
To evaluate the thermal cycle fatigue performance of a hybrid joint vs. a homogenous joint, a 16.5mm x 28mm, 0.43mm pitch ball grid array (BGA) component was chosen as the test vehicle. The package used an electroless nickel-electroless palladium-immersion gold (ENEPIG) surface finish and a 250µm solder sphere. Half of the packages were built with a SAC 405 solder sphere, and the other half were built with a SnBi solder sphere with 40% Bi and supplier proprietary dopants. The packages were assembled on a 700µm thick, 15cm x 15cm printed circuit board with copper organic solderability preservative (Cu OSP) surface finish. Each test board had a single package placed at the center of the board. The test board was designed with a daisy chain to allow *in-situ* continuity monitoring during temperature cycle (TC) testing.

Boards were assembled using two different Sn-Bi LTS solder pastes. To accelerate fatigue failures and reduce testing time, a stencil was designed that did not print paste in certain known high-stress locations (FIGURE 6). Due to the depopulated stencil apertures, no solder joints were formed at those locations. The stress on the remaining joints were increased, thus reducing mean time to failure. A 100µm-thick nano-coated stencil was used with a 237.5µm round aperture for each pad. This resulted in a theoretical solder volume of 0.0046mm<sup>3</sup>. Compared to the 0.0086mm<sup>3</sup> volume of the 254µm solder sphere, the resulting paste:ball volume ratio for the hybrid joints was 0.535, very close to the target 0.5 ratio (Table 1).

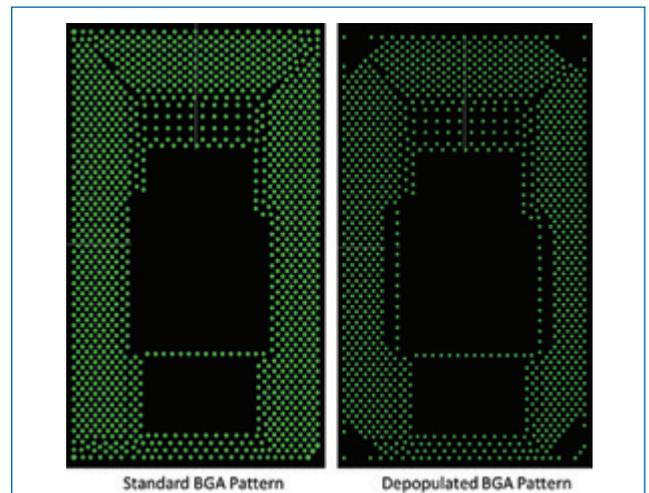
After paste print on a DEK Galaxy printer, 100% paste volume data were collected using a Koh Young solder paste inspection machine. BGA components with both hybrid and homogeneous LTS joints were assembled using peak reflow temperature of 190°C for paste A. Assembly for paste B involved hybrid joint BGA reflow at 175°C peak and homo-



**FIGURE 4.** Post-reflow solder joint height difference: hybrid vs. homogenous joints.



**FIGURE 5.** Hot tear defect in a hybrid joint (left) vs. complete collapse under the same SMT process conditions eliminates hot tearing for a homogeneous LTS joint (right).



**FIGURE 6.** Rows two and three on both right and left long sides of the die shadow region were depopulated in stencil design for thermal cycle testing.

geneous LTS BGA reflow at both 175°C and 190°C peak. For both pastes, a soak of 60-90 sec. between 100° to 120°C and a total time above liquidus (set as 151°C) of 100 to 120 sec. was used. The same reflow conditions were used for hybrid and homogenous joints. All samples were reflowed in ambient air. Post reflow, each board was tested for electrical continuity using a flying probe and then inspected in a Vitrox automated x-ray tool to ensure no solder bridging was present. A corner adhesive was used to provide extra mechanical support at the corners of the package. Prior to initiating thermal cycle testing, one package from each leg was cross-sectioned (XS) to verify solder joint quality.

Test boards were thermal-cycled in an unloaded configuration using a -40° to 85°C, 30 min. cycle. Electrical continuity was measured continuously *in-situ*. The sample size was nine boards per leg. Testing was continued until at least 80% of the boards had recorded a failure to permit a Weibull plot to be completed. Eight of nine packages were dyed and pulled post thermal cycling to identify crack type based on the failure interface as shown in Figure 3. The number of cracks larger than 80% of the solder joint area was measured for each crack type. One package from each leg was cross-sectioned to study the microstructure post thermal cycling.

**Drop shock reliability: BGA assembly and testing details.** A study was completed comparing the mechanical shock capa-

bility of a homogenous SAC interconnect, a hybrid SAC-LTS interconnect formed using paste volumes to result in optimum and extended Bi mixing, and a homogenous LTS interconnect. The daisy chain test vehicle was a 16.5mm x 28mm, 0.43mm pitch BGA. The package used an ENIG surface finish and a 250µm solder sphere. Half of the packages were built with a SAC 405 solder sphere, and the other half were built with a Sn-Bi solder sphere with 40% Bi and supplier proprietary dopants. For the hybrid and homogenous LTS solder joints, paste A was utilized. The homogenous SAC solder joints were formed using a SAC 305 solder paste. The BGA packages were soldered to a 700µm-thick, 30.5cm x 30.5cm test board. No corner adhesive was used. For this testing, the BGA joints were fully populated, as no-time-to-fail acceleration was required. The test board was designed with a daisy chain to permit solder joint electrical continuity to be continuously monitored *in-situ* during drop testing.

Mechanical drop testing was completed using a drop table and a variable acceleration (G) level, 2 ms pulse, ½ sine. The sample size was 10 boards per leg. For each sample, five drops were completed at a starting G level of 80G. If no electrical fails were recorded, the G level would be increased by 5G and five drops repeated. Testing continued until all samples had recorded an electrical fail. Capability is reported as <1% fail at 90% lower confidence limit (LCL).

## Results and Discussion

**DSC Results.** Both LTS paste materials showed comparable melting behavior (**TABLE 2**) despite different Bi composition.

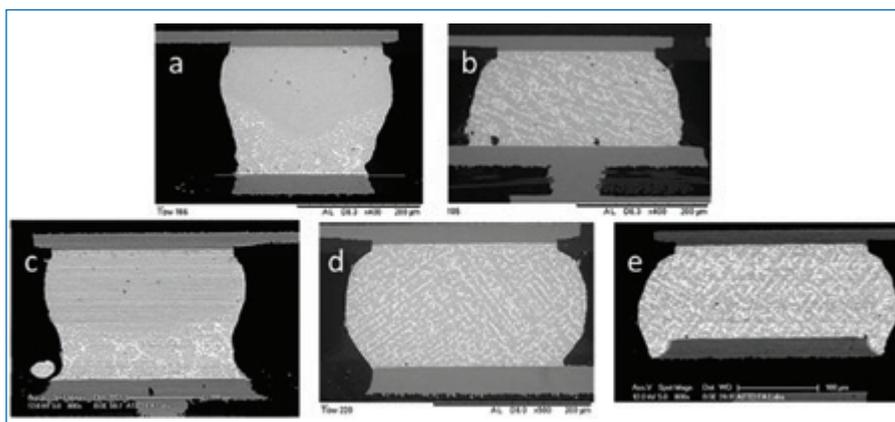
**Post-SMT/pre-reliability characterization.** One board from each SMT leg was cross-sectioned post-SMT (Figure 4) along column 12 of the package. This column typically exhibited the highest stress solder joints in historical thermal cycle testing on the package. Representative scanning electron microscope (SEM) images are shown in **FIGURE 7**. Overall, hybrid joint microstructures were comparable for both paste A and paste B.

### Temperature cycle testing results.

All thermal cycle testing failures occurred in the die shadow region around the central cavity of the package. Thermal cycle Weibull plots (**FIGURES 8** and **9**) showed a significant improvement in the failure predictability ( $\beta$  parameter) for homogeneous LTS joints over SAC-LTS hybrid joints. The characteristic life ( $\alpha$ ), however, was lower for homogeneous LTS joint with paste A, whereas it was higher for homogeneous LTS joint with paste B for both 175°C and 190°C peak reflow temperature (**TABLE 3**). These trends for paste A and paste B are consistent with earlier lab level mechanical

**TABLE 2.** Melting Behavior Comparison for Paste A, Paste B, and LTS BGA Spheres

Material	Paste A	Paste B	LTS Spheres (supplier data)
Bi weight in alloy	50%	58%	40%
Dopants	Supplier proprietary		
Melting onset	139.0°C	132.6°C	139°C
Melting peak	139.7°C	137.7°C	140°C
Melting end (Liquidus)	152.8°C	151.4°C	174°C



**FIGURE 7.** Post-SMT microstructure for (a) paste A hybrid 190°C peak, (b) paste A homogeneous 190°C peak, (c) paste B hybrid 175°C peak, (d) paste B homogeneous 175°C peak, (e) paste B homogeneous 190°C peak.

testing, where paste B showed better performance than paste A in mixed mode fatigue testing.<sup>6</sup>

Homogeneous joints also help reduce the microstructure variation typically observed in the hybrid joints. For the hybrid joints, the natural variation in the extent of Bi exposure at the package side as cycling progresses is hypothesized to account for the larger variation in cycles to fail. Previous research<sup>4</sup> shows SnBi solder joint performance reveals less capability when paired with NiAu-based surface finishes. For the test vehicle in this study, a homogenous LTS solder joint is expect-

ed to fail preferentially at the ENEPIG interface (package side). Literature<sup>4</sup> also shows historically that a homogenous SAC solder joint should be more capable than a hybrid SAC-LTS joint, unless the homogenous SAC + ENEPIG has low concentrations of Bi. For the test vehicle in this study, assuming no Bi exposure at the package side, failure location is expected to be at the PCB side.

For both pastes, the majority of failures for the homogenous solder joints was at the package (ENEPIG) interface, which is consistent with the expectation. Only paste B reflowed at 190°C, with LTS BGA showing a few failures at the PCB interface, as shown in Table 3. These cracks are fatigue-driven in the bulk solder (FIGURE 10). In the case of the hybrid solder joints, most of the failures were located at the PCB (OSP) interface, consistent with expectations. A smaller number of failures were noted at the package (ENEPIG) interface, however. As evident from the crack location variation, an inconsistent failure location results in a lower  $\beta$  parameter. To help with the argument, we define a crack location variability parameter (CLVP) as:

$$CLVP = \text{minimum (No. of T2 cracks/No. of T3 cracks, No. of T3 cracks/No. of T2 cracks)}$$

For hybrid joints in this study, no. of T3 cracks > no. of T2 cracks. Hence CLVP is T2/T3, whereas, for homogeneous LTS joints with predominant T2 failures, CLVP is T3/T2. This parameter captures the consistency of cracking locations for solder joints. As observed in Figure 9, it has an excellent correlation with Weibull  $\beta$  parameter. This further asserts variable cracking in a solder joint can impact thermal cycle life predictability.

A microstructure study using SEM showed the best performing homogeneous LTS leg, paste B with 190°C reflow, had more refined Bi-phase post thermal cycling compared to the rest of the two homogeneous LTS legs. The higher Bi-phase refinement can help pin a crack at the Bi/Sn interface, whereas larger Bi particles will lead to a crack along the Sn/Bi interface or through the bulk of the brittle Bi-phase.

**Drop-shock testing results.** All failures in the drop-shock reliability testing were at the package corner, unlike the thermal cycle testing. Failed samples from the drop-shock testing were submitted to a dye-and-pull process, and then crack type was documented. For the homogenous SAC samples, the primary failure location was cracking under the PCB pad into the board laminate (pad crater). Both hybrid sample legs cracked preferentially at the solder joint-PCB pad interface, indicating the hybrid SAC-LTS metallurgy is weaker than the ENEPIG-SAC interface. In the homogeneous LTS samples, cracking occurred preferentially (>70% cracks) at the package side interface (T2 crack). SEM microstructure study confirmed the findings (FIGURE 11).

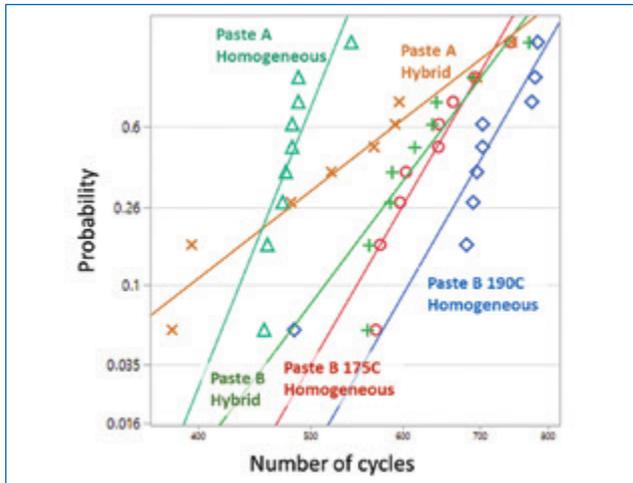


FIGURE 8. Thermal cycle failure Weibull plot for hybrid vs homogeneous LTS joints.

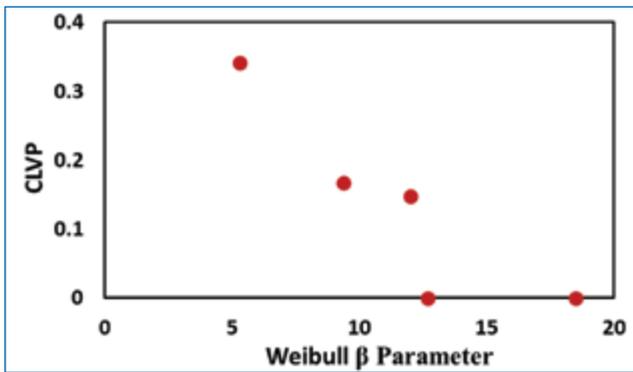


FIGURE 9. Crack location variability parameter (CLVP) vs. Weibull  $\beta$  parameter.

TABLE 3. Thermal Cycle Reliability Results with Crack Type Statistics

Solder Joint Type	Paste	Peak Reflow	TC Weibull Parameters		No. of Cracks	
			$\alpha$	$\beta$	T2	T3
Hybrid	A	190°C	601	5.3	15	44
Homogeneous	A	190°C	494	18.5	71	0
Hybrid	B	175°C	659	9.4	9	54
Homogeneous	B	175°C	668	12.7	70	0
Homogeneous	B	190°C	732	12	61	9

**TABLE 4** summarizes the mechanical drop capability for each experimental leg. The homogenous SAC samples recorded the highest capability value. As was expected, the hybrid SAC-LTS samples built to create excessive Bi mixing showed reduced performance compared to the hybrid samples built to optimize Bi mixing. The homogenous LTS samples showed greater capability than the hybrid samples and performed almost as well as the homogenous SAC units for the critical-to-function (CTF) pin locations.

**Conclusions**

Homogeneous LTS joints are expected to reduce SMT process complications, leading to higher predictability in the solder joint microstructure, reliability performance, and elimination of hot tearing defects. The current study shows that with the right material choices and correct process parameters, homogeneous LTS joints perform significantly better than hybrid joints in both thermal cycle and drop-shock reliability. In addition, a correlation needs to be established between a solder joint life in actual use conditions and thermal cycle life, as a Bi diffusion-driven mechanism may play a role in failure, along with conventional intermetallic compound growth-driven failure in SAC solder joints. This study is applicable for both SAC-LTS hybrid and homogeneous LTS BGA solder joints, which are expected to be highly relevant with increased adoption of SMT LTS technology in the industry.

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**REFERENCE**

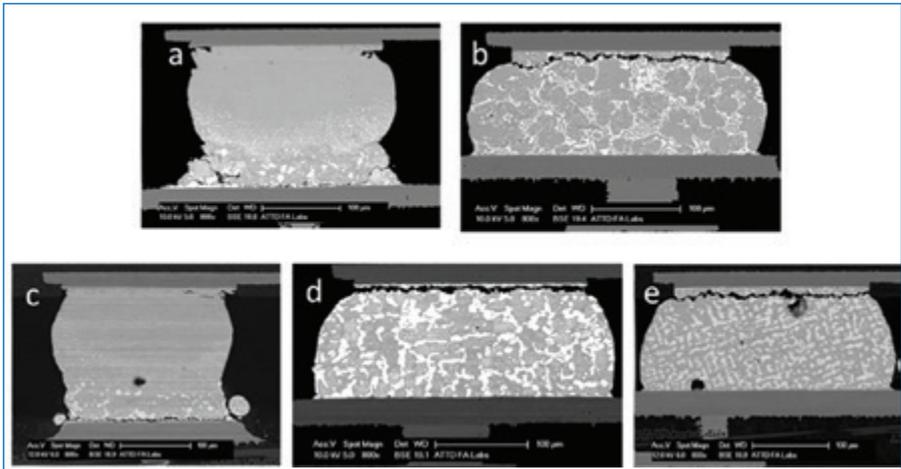
- Shubhada Sahasrabudhe, Scott Mokler, Mukul Renavikar, Sandeep Sane, Kevin Byrd, Eric Brigham, Owen Jin, Pubudu Goonetilleke, Nilesh Badwe and Satish Parupalli, "Low Temperature Solder – A Breakthrough Technology for Surface Mounted Devices," IEEE 68th Electronic Components and Technology Conference (ECTC), May 2018.
- Hisaaki Takao, Akira Yamada and Hideo Hasegawa, "Mechanical Properties and Solder Joint Reliability of Low-Melting Sn-Bi-Cu Lead-Free Solder Alloy," R&D Review of Toyota CRDL 39, no. 2, 2004.
- Scott Mokler, Raiyo Aspandiar, Kevin Byrd, Olivia Chen, Satyajit Walwadkar, Kok Kwan Tang, Mukul Renavikar and Sandeep Sane, "The Application of Bi-based Solders for Low Temperature Reflow to Reduce Cost while Improving SMT Yields in Client Computing Systems," SMTA International, September 2016.
- Seiki Sakuyama, Toshiya Akamatsu, Keisuke Uenishi and Takehiko Sato, "Effects of a Third Element on Microstructure and Mechanical

Properties of Eutectic Sn-Bi Solder," *Transactions of the Japan Institute of Electronics Packaging*, vol. 2, no. 1, 2009.

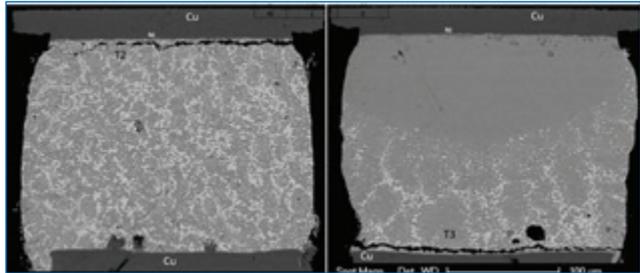
- Todd Harris, Kevin Byrd and Nilesh Badwe, "Root Cause and Solution to Mitigate the Hot Tear Defect Mode in Hybrid SAC-Low Temperature Solder Joints," SMTA International, September 2019.
- Satyajit Walwadkar, Suresh Guthikonda, Raiyo Aspandiar and George Hsieh, "A Novel Approach to Determine Mechanical Fatigue Performance of Solder Material using Single Solder Joint Test," SMTA International, October 2018.

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**FIGURE 10.** Post-TC microstructure for (a) paste A hybrid 190°C peak, (b) paste A homogeneous 190°C peak, (c) paste B hybrid 175°C peak, (d) paste B homogeneous 175°C peak, (e) paste B homogeneous 190°C peak.



**FIGURE 11.** Homogeneous LTS (left) vs. SAC-LTS hybrid (right) joints showing failure post-shock test.

**TABLE 4.** Mechanical Drop Capability Results Versus Solder Joint Construction

Solder Joint	First-Fail Capability	CTF Capability	Major Crack Type
Homogeneous SAC	99.6G	135.7G	T4
Hybrid (extended Bi mixing)	63.7G	109.9G	T3
Hybrid (optimized Bi mixing)	70.5G	120.8G	T3
Homogeneous LTS	78.4G	129.6G	T2

The logo for PCB WEST 2020 features the letters 'PCB' in a bold, white, sans-serif font inside a teal square. To the right, the words 'WEST 2020' are written in a larger, dark grey, sans-serif font. Below this, the words 'Conference & Exhibition' are written in a smaller, dark grey, sans-serif font. The background of the entire page is a gradient from teal to yellow, overlaid with a complex, glowing circuit board pattern.

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VYCOM Global Sources Ltd.  
Xiamen Bolion Tech. Co., Ltd.  
Zuken USA Inc.

# Screen Printing Hacks: Alignment

Not sure how to tackle an alignment issue?  
These tips might help set you straight.

**IN TODAY'S SLANG**, a “life hack” is any trick, shortcut, or proven workaround for a given task that increases productivity and efficiency. And, as regular readers will be acutely aware, this column's focus is all about improving printing productivity and efficiency. So, I thought a series of “screen-printing hacks” might be helpful to engineers, no matter the level of experience. Throughout 2020, this space will periodically delve into various screen-printing hacks; an issue central to a good print outcome will be identified, and I'll cover some ways to get the process back on track if something goes awry. The first installment of our screen-printing hack series is alignment.

The goal for the printing process is 100% alignment; the solder paste must align with the feature (the pad) on the substrate. When the solder paste inspection (SPI) system indicates this is not the case and offsets (paste not centered on the pad) are present, an alignment issue is most likely the culprit. Where do you start? Here's a list of the most common causes and potential fixes; i.e., hacks:

**Machine calibration.** First things first. When was the last time the printer was calibrated? The truth is most operators and line engineers can't answer this question, which is a bit scary. Nevertheless, when alignment is off, the first thing to do is run SPC for an alignment check on the system. It's literally a 10-minute exercise that could save countless hours and lost yield. If it doesn't pass, do a machine calibration – *stat!* (An annual maintenance program wouldn't hurt, but I digress.)

**Fiducial issues.** Potential issues and fixes here are many. In short, make sure fiducials are well-defined, and use as many as possible given the allowable cycle time. To get a read on fiducial readiness, interrogate the fiducial and look at the score (out of 1,000 on our company's system). A score less than 70% indicates something's not right, so go down the list.

- **Correct size and shape:** The machine is looking for something 1.0mm, but if the board fabricator has made it a bit smaller, then the alignment might not be centered. Or, if the fiducial mark isn't round (most are, although there are the occasional diamonds and squares) and ends up a bit egg-shaped, it can also affect solder paste deposit location. Again, the fiducial score is a great tool for identifying any fiducial shape issues.

- **Color:** If the fiducial is gold flash, ensure there is a dark background so the camera can see it and accurately find the edge. If the fiducial color is too close to that of the background/substrate color, the camera may struggle to locate it.
- **Quantity:** A minimum of two fiducials are needed to get triangulation, but some systems accept three or four fiducials. In my book, and especially in the age of high-density designs and miniaturization, the more the better for accurate alignment. The cycle time tradeoff to using more is negligible, so I say go for it, especially with complex boards.

**Rotation.** So, the machine is in calibration, fiducials check out and offsets are still present. Now what? I suggest rotation. Theta offset is historically an adjustment many operators/technicians tend to shy away from. However, it is often a necessary evil. Dialing in offsets is paramount for good alignment. Estimating x and y offsets is relatively straightforward. Rotation, however, takes a little more reasoning. If you chose to do this manually, my advice is to start by dialing out the theta and then move to the x and y. Full disclosure: I use our company's automated printing process control technology that, when enabled, makes the rotation adjustments for you. That's the ultimate hack!

**PCB fabrication issues.** If, after all these checks, solder paste is still not on the pad, start investigating the PCB fabrication. Our company recently saw an issue with some mobile phone substrates. The solder-mask-defined pads were not, shall we say, very well defined, and the pad openings were not exactly where the Gerber file said they should be. If that's the case, then you have a good game because the problem could be anywhere. In this situation, I'd use a tool on our machines called “video model.” Instead of relying on fiducial alignment, choose a unique pad defined by the solder mask (i.e., not one in the middle of a CSP!), and use the video model as the alignment point instead of the fiducial. To be fair, this is a heck of a hack and a last resort. But, if the issue is a solder mask definition problem, this is the way to go.

While a whole host of potential mechanical interactions can impact alignment, the above are my top contenders. Next up on the hacking front: bridging. □

**CLIVE ASHMORE**  
is global applied  
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manager at ASM  
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ashmore@asmpt.  
com. His column  
appears bimonthly.



# Solder Surface Deformation

When solder isn't shaped correctly, the condition is known as head-in-pillow.

**THIS MONTH WE** show the ball surface on area array packages where no solder joint was formed. The joints were intermittent, but one of the surfaces – either the ball or the surface of the solder on the pad – was deformed. This is better known as head-in-pillow (HiP) or head-on-pillow (HoP), depending

on the shape formed on the solder adjacent surface.

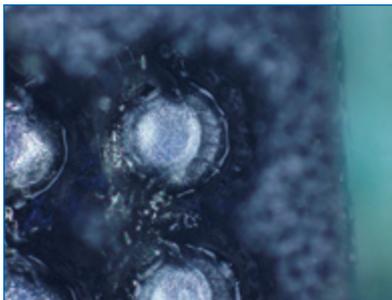
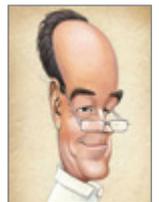
**FIGURES 1** and **2** show examples of HiP/HoP. In Figure 1, the surface of the ball is shown after mechanically separating the device from the board. The indent of the solder from the pad on the board is visible.

Figure 2, on the other hand, shows a ball with some residue but with no indentation. Compared with the corresponding PCB pad, it may show the reflowed solder being deformed.

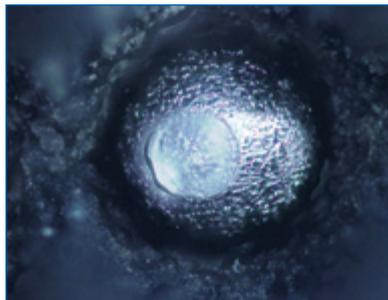
We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at [youtube.com/user/mrbobwillis](https://www.youtube.com/user/mrbobwillis). □

## BOB WILLIS

is a process engineering consultant; bob@bobwillis.co.uk. His column appears monthly.



**FIGURE 1.** The surface of the ball after mechanically separating the device from the board.



**FIGURE 2.** A ball with some residue but with no indentation.

## How Efficient is Your Company's Account Acquisition Process?

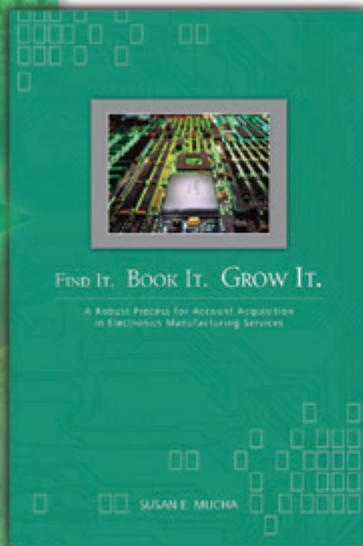
In the electronics manufacturing services (EMS) industry, differentiation is key to winning and growing accounts. Differentiation isn't simply the best slogan or ad, it's also the approach taken in developing value propositions, setting expectations and delivering value after the sale.

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EMS Account  
Acquisition.

Find it at [amazon.com](https://www.amazon.com),  
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IPC and SMTA.



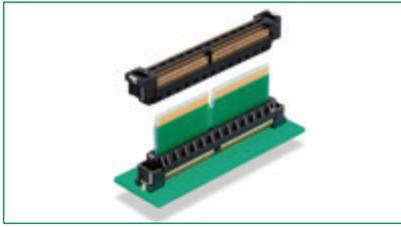
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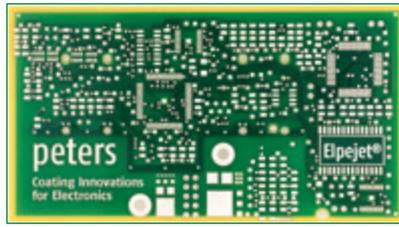


### HIGH-SPEED B2B CONNECTOR

FX27 0.8mm pitch card edge board-to-board connector allows flexible stacking heights. Allows varying board stack heights by changing length of PCB interposer. Supports floating range of  $\pm 1.2$ mm in x and y; absorbs stress from misalignment while tightening screws and PCB shrinkage caused by high temperatures. Self-alignment range of  $\pm 0.7$ mm.

Hirose Electric Co.

hirose.com

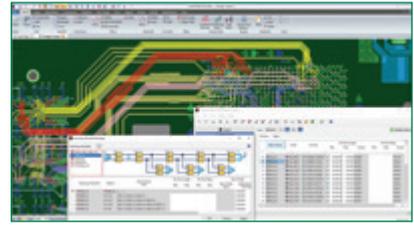


### INKJET SOLDER RESISTS

With print head adjusted, Elpejet reportedly provides print image and edge coverage precise to specification, along with high resolution. Among typical application parameters, there is pinning with UV LEDs immediately after printing, an additional UV bump if necessary, or thermal curing to achieve relevant final properties such as no bleeding, adhesion, scratch/crack resistance, etc.

Lackwerke Peters

peters.de



### HIGH-SPEED ROUTING

eCADStar Advanced HS extends 3-D PCB design capabilities with high-speed routing tools, such as length, delay-based impedance, skew control and comprehensive constraint management capabilities. Constraints can be specified in schematic and physical design tools or as design rule stacks.

Zuken

us.zuken.com

## OTHERS OF NOTE

### HIGH-VOLTAGE CONNECTOR

PQ50 series rugged high-power connector comes in lightweight plated plastic resin or zinc die cast shell. Is rated up to 600V. Two-point contact design is for industrial machinery and wafer/LCD carrier machines. Comes in water-resistant version.

Hirose Electric

hirose.com

### PPS FILM FOR 5G PCBs

Polyphenylene sulfide (PPS) film reportedly maintains dielectric characteristics, flame retardancy and chemical robustness of polymer, while remaining thermally resistant at 40°C higher than conventional counterparts. Resists deformation up to 250°C and is dimensionally stable near 280°C melting point. Offers electrical insulation. Has CTE in thickness direction of 98 ppm/°C.

Toray Industries

toray.com

### NANO SIM CARD CONNECTOR

KP13B Nano SIM card connector reportedly reduces required PCB mounting space up to 26%. Simplifies designs in digital cameras, digital video cameras, laptops, printers, smartphones and TVs. Card detection feature prevents incorrect card insertion; ensures proper mating and protects contacts from damage. Offers 5,000 mating cycles.

Hirose Electric

hirose.com

### FREE CLOSED-SOURCE SIMULATOR

Micro-Cap 12 includes multipage schematic editor, native digital simulation, Monte Carlo analysis, 33,000 parts in library, worst-case and smoke analysis and Smith charts. Incorporates spreadsheets. Supports active device models, including recent MOSFET models. Reads almost any regular Spice or IBIS model.

Spectrum Software

spectrum-soft.com

### HARSH ENVIRONMENT INDUCTOR

IHDF-1300AE-10 through-hole inductor features a low-loss edge-wound coil with a ferrite core. Operates over a temperature range of -55° to +125°C with low AC and DC power losses and excellent heat dissipation. Is reportedly ideal for mechanical shock and vibration.

Vishay Intertechnology

vishay.com

### SOLDERLESS PCB CONNECTORS

Micro-Mini (SMP/SMPM) extreme frequency subminiature RF/coaxial push-on solderless PCB compression mount connectors are for high-frequency printed PCBs. Solderless application makes assembly fast and easy, without damaging PCB. RF performance DC to 65GHz.

Amphenol SV Microwave

svmicrowave.com



### LOW OUTGASSING EPOXY

Supreme 121AO is suitable for bonding, sealing and potting. Features a Tg of 200°-210°C; resists temperatures up to 550°F. Less stiff than conventional epoxies that withstand extreme temperatures. Tensile modulus is 750,000 to 850,000psi at room temp., and compressive strength is 26,000 to 28,000psi. NASA approved for low outgassing.

Master Bond  
masterbond.com



### X-RAY COMPONENT COUNTER

Assure is for live component inventory management. Is plug-and-play; uses advanced algorithms to identify new components and does not rely on libraries or cloud-only support. One-button operation and intuitive touchscreen UI. Counts components quickly regardless of how full or empty the reel is. Validates results immediately.

Nordson Dage  
nordson.com/en/divisions/dage



### TINY PARTS REWORK

JNASE is for rework of 0402, 0201, 01005 and 008004 components. Is designed for HDI boards. Enables flow regulation of temperatures and air at very low levels to avoid expulsion/movement of adjoining components. Pedal-activated pick-and-place.

JBC Tools  
jbc tools.com

## OTHERS OF NOTE

### SOLDER PASTE VISCOMETER

PCU-285 spiral viscometer creates, executes and stores measurement programs with or without a PC. Touch panel display. Features compact and enhanced heating unit, making it easier to put inside or take out sample; simplifies cleaning. Temperature control and viscosity measurement have been improved in stability and speed.

Malcom  
malcom.co.jp/en

Seika Machinery  
seikausa.com

### 'EASY-RINSE' STENCIL CLEANER

Kyzen E5631 is formulated to clean flux and uncured adhesives from stencils and misprints. Is diluted and used in all stencil cleaning processes, including spray-in-air and ultrasonic processes, as well as in printer as under-stencil wipe solution. Cleans all widely used assembly materials. Reportedly rinses easily and completely. Formulated to operate at low concentrations (<25%).

Kyzen  
kyzen.com

### SINGLE-HEAD SOLDERING ROBOT

TMT-R8000S soldering robot is designed for simplified soldering applications. Includes vision/mapping and dynamic laser height control. Incorporates same IP software used on benchtop system.

Thermaltronics  
thermaltronics.com

### 'ANY CURE' GAP FILLER

GF400 is a two-part, liquid silicone-based gap filler that can be cured at room temperature or with heat. Following cure, forms a low modulus elastomer said to prevent "pump-out phenomenon," for minimal degradation of effective heat dissipation. Operating temp. range of -50° to +200°C. Low viscosity.

Electrolube  
electrolube.com

### FAST-SETUP PROGRAMMING SOFTWARE

NexTeach Pro software for PSV7000 automated programming system reportedly reduces job setup time up to 4x and increases production throughput up to 24%. Delivers one-touch teaching with up to 10x better accuracy and increases overall handler performance. Automates XYZR measurements and coordinates with single button. Optimizes handler settings by package type.

Data I/O  
dataio.com

### 3-D INLINE AOI

ALD8720S delivers shadow-free 3-D height measurement of solder joints and components, fast inspection, 100% board coverage, high detectability, low false call rate, auto-programming, debug-free powerful OCR, IPC-based defect judgement criteria and other features. Standard configuration includes reading barcodes with camera, SPC and verification software installed on system, support for central server and library, and support for offline programming and rework stations.

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Santa Clara, CA	June 10 & 11

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## In Case You Missed It

### Additive Technologies

“Process Capability of Aerosol-Jet Additive Processes for Long-Runs up to 10-Hours”

*Authors:* Pradeep Lall, Ph.D, Amrit Abrol, Nakul Kothari, Ben Leever and Scott Miller; lall@auburn.edu.

*Abstract:* Aerosol Jet supports a variety of materials, including nanoparticle inks and screen-printing pastes, conductive polymers, insulators, adhesives, and even biological matter. Adoption of additive manufacturing for high-volume commercial fabrication requires an understanding of the print consistency and electrical and mechanical properties. Little literature exists that addresses the effect of varying sintering time and temperature on the shear strength and resistivity of the printed lines. In this study, the effect of process parameters on the resultant line-consistency, mechanical and electrical properties is studied. Print process parameters studied include the sheath rate, mass flow rate, nozzle size, substrate temperature and chiller temperature. Properties include resistance and shear load to failure of the printed electrical line as a function of varying sintering time and varying sintering temperature. Aerosol Jet was used to print interconnects. Printed samples were exposed to different sintering times and temperatures. The resistance and shear load to failure of the printed lines was measured. The underlying physics of the resultant trend was then investigated using elemental analysis and SEM. The effect of line-consistency drift over prolonged runtimes has been measured for up to 10hr. of runtime. Printing process efficiency has been gauged a function of process capability index (Cpk) and process capability ratio (Cp). Printed samples were studied offline using optical profilometry to analyze the consistency within the line width, line height, line resistance and shear load to study the variance in electrical and mechanical properties over time. (ASME International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems, October 2019)

### Materials Science

“Radiophysicists Study the Properties of Composites for 5G devices”

*Authors:* Tomsk State University

*Abstract:* TSU radiophysicists are forming a database of properties of composite materials, which can be used to create devices with 5G and space communication devices operating in the terahertz range. The scientists are creating composite materials from ABS plastic and nanotubes and measuring their properties in a frequency range from 10MHz to 1THz. To create the source material, the radiophysicists are using polymers and, aided by chemical treatment, filling them with carbon nanotubes, which the Boreskov Institute

of Catalysis of the Siberian Branch of the Russian Academy of Sciences produces for the Terahertz Laboratory of the Faculty of Radiophysics. By adding nanotubes of different concentrations, the electrophysical properties of the material are changed; for example, the dielectric constant is increased. Then, using 3-D technology, a printed circuit board with elements (conductors, resistors, and others) can be created. From the material obtained on a 3-D printer, a control sample is printed – plates or rings, depending on the standard of the measuring installation, and the properties of the composite in the terahertz range are examined. Properties of 50 samples in the radioactive range up to 1THz have been studied. (Tomsk State University website, Dec. 9, 2019, [en.tsu.ru/news/radiophysicists-study-the-properties-of-composites-for-5g-devices/](http://en.tsu.ru/news/radiophysicists-study-the-properties-of-composites-for-5g-devices/))

### RF Antennas

“Two-Dimensional Metallic Niobium Diselenide for Sub-Micrometer-Thin Antennas in Wireless Communication Systems”

*Authors:* Girish Sambhaji Gund, Min Gyu Jung, Keun-Young Shin and Ho Seok Park.

*Abstract:* State-of-the-art Internet of things (IoT) and smart electronics demand advances in thin and flexible radio frequency (RF) antennas for wireless communication systems. So far, nanostructured materials such as metals, carbon nanotubes, graphene, MXene, and conducting polymers have been investigated due to their noteworthy electrical conductivity. However, most antennas based on metallic materials are thick, which limits their application in miniaturized and portable electronic devices. Herein, the authors report 2-D metallic niobium diselenide (NbSe<sub>2</sub>) for a monopole patch RF antenna, which functions effectively despite its sub-micrometer thickness, which is less than the skin depths of other metals. The as-fabricated antenna has an 855nm thickness and a 1.2Ωsq<sup>-1</sup> sheet resistance and achieves a reflection coefficient of -46.5dB, a radiation efficiency of 70.6%, and omnidirectional RF propagation. Additionally, the resonance frequency of this antenna at the same thickness is reconfigured from 2.01 to 2.80GHz, while decreasing its length and preserving its reflection coefficient of less than -10dB. This approach offers a facile process to synthesize 2-D metallic transition metal dichalcogenides for the rational design of flexible, miniaturized, frequency-tunable, and omnidirectional monopole patch RF antennas for body-centric wearable communication systems. (ACS Nano, November 2019, [pubs.acs.org/doi/10.1021/acsnano.9b06732](https://pubs.acs.org/doi/10.1021/acsnano.9b06732))

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

# 5G: Higher Frequencies!

## Do you have the **right** circuit materials?

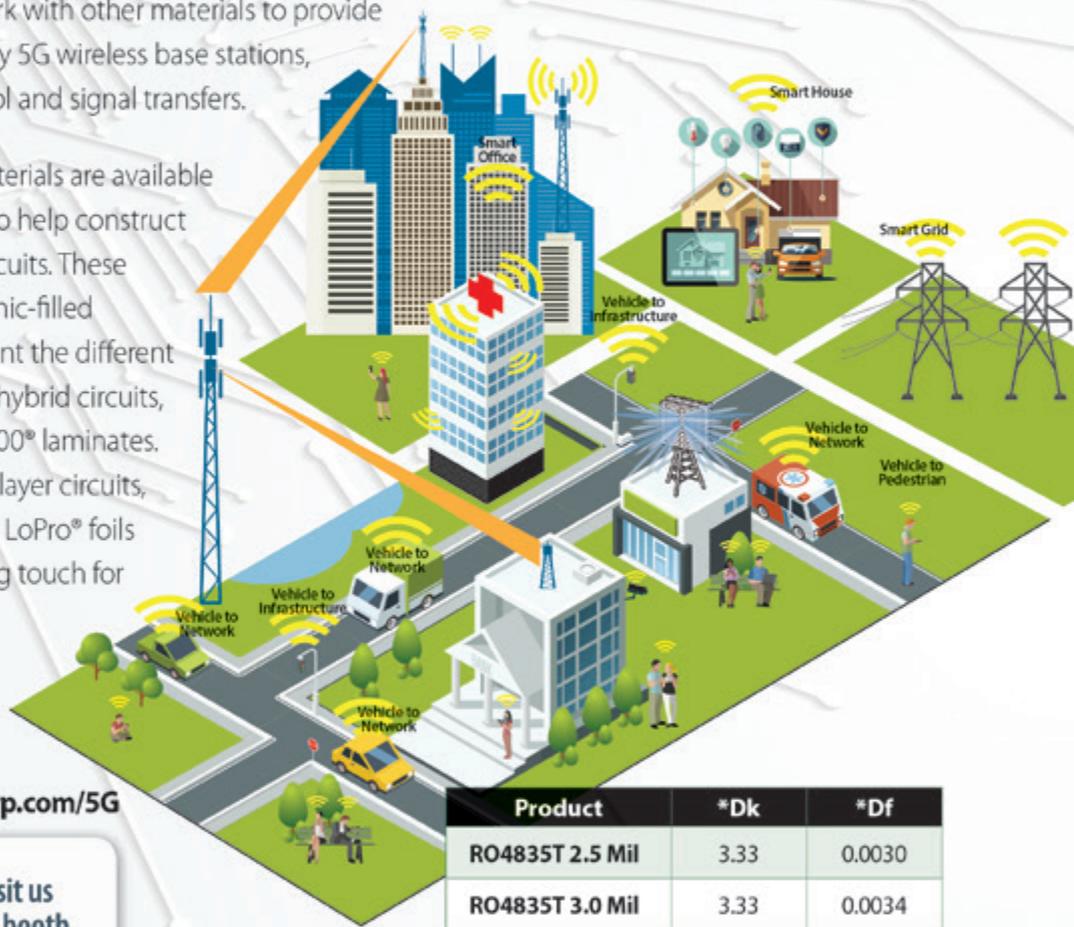
Frequencies at 28 GHz and higher are being used in Fifth Generation (5G) wireless communications networks. 5G infrastructure depends on low-loss circuit materials engineered for high frequencies, materials such as RO4835T™ laminates and RO4450T™ bonding materials from Rogers Corporation!

Rogers RO4835T spread-glass-reinforced, ceramic-filled laminates are low-loss materials in 2.5, 3.0, and 4.0 mil thicknesses. They are well suited for millimeter-wave frequencies as part of the inner cores of 5G hybrid multilayer PCBs. They can work with other materials to provide the many functions needed by 5G wireless base stations, including power, signal control and signal transfers.

Rogers RO4450T bonding materials are available in 3, 4, and 5 mil thicknesses to help construct those 5G hybrid multilayer circuits. These spread-glass-reinforced, ceramic-filled bonding materials complement the different materials that will form these hybrid circuits, including RO4835T and RO4000® laminates. And for many 5G hybrid multilayer circuits, Rogers CU4000™ and CU4000 LoPro® foils will provide a suitable finishing touch for many hybrid multilayer circuit foil lamination designs.

**5G is here! Do you have the right circuit materials?**

Learn more at [www.rogerscorp.com/5G](http://www.rogerscorp.com/5G)



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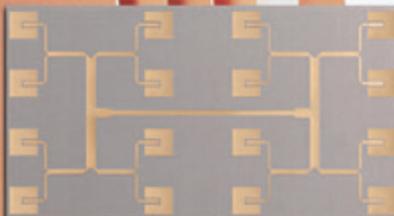


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Product	*Dk	*Df
RO4835T 2.5 Mil	3.33	0.0030
RO4835T 3.0 Mil	3.33	0.0034
RO4835T 4.0 Mil	3.32	0.0036
RO4450T 3.0 Mil	3.23	0.0039
RO4450T 4.0 Mil	3.35	0.0040
RO4450T 5.0 Mil	3.28	0.0038

\* IPC TM-650 2.5.5.5 Clamped Stripline at 10 GHz - 23°C



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