UP Media Group

5 Ideas for Ensuring Supply Chain Stability

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CIRCUITS ASSEMBLY

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AUGUST 2020

Are 2 better than 1?

(Lee Ritchey Says No!)

Embedding Magnetics

Understanding BGA Anomalies

Low-Temperature Soldering

AUGUST 2020 • VOL. 37 • NO. 8

PRINTED CIRCUIT DESIGN & FAB CIRCUITS ASSEMBLY

FIRST PERSON

MONEY MATTERS

TECH TALK

DEPARTMENTS

FEATURES

IN THE DIGITAL EDITION

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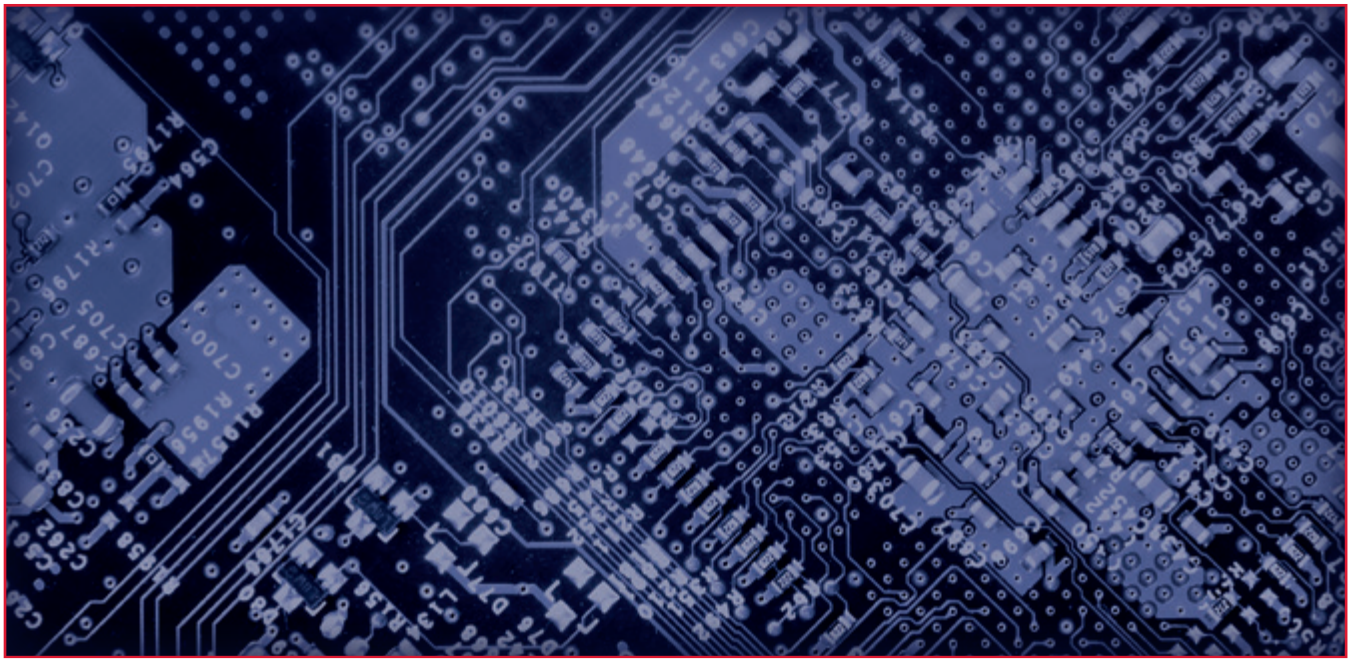

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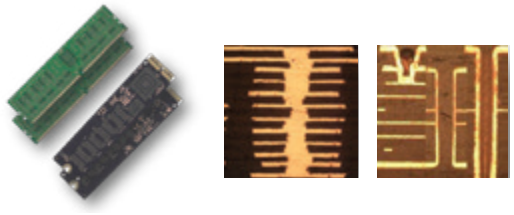
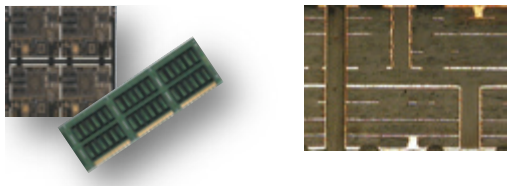
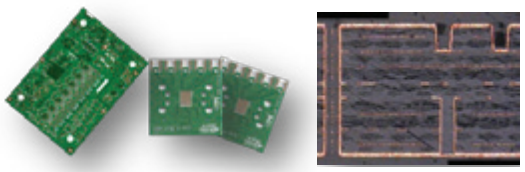


IOT / Build-up Board



Semiconductor TEST B'd & 5G Network System



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MIKE BUETOW
EDITOR-IN-CHIEF

Living in the Virtual World

SOME 13 YEARS ago, UP Media Group launched the first virtual trade show for the electronics industry. In some ways – most, probably – we were ahead of the times. People liked it because it was simple to attend, but the platform wasn't ready for prime time.

That's not to say it was technically subpar. You could pop in and out of booths and talk to the personnel waiting for you, and I still feel for those folks who, driven by caffeine and excitement (or just an affinity for self-abuse), kept vigil around the clock as attendees in different time zones came on line and into the show. And we held webinars and chats with high-profile experts like Dr. Eric Bogatin. But in the end, attendees seemed to prefer meeting with peers face to face.

Covid-19 is injecting itself into almost every facet of our work and home lives, however, and we have to make some concessions to the times. As such, we have made the difficult but necessary decision to make PCB West a virtual event this year. The call was made following a survey of past attendees and talks with our more than 100 exhibitors.

We are pleased to announce, however, that almost all the technical sessions originally slated for the live PCB West will now be available on demand, starting Sept. 7. That's more than 125 hours' worth of high-end technical training. For the full list, see the conference catalog at pcbwest.com.

On the plus side, even those with severe travel restrictions will be able to participate in this year's show. Each year, we receive feedback from conference-goers that there's more presentations to hear than they can get to in four days. Since PCB West Virtual 2020 is all on-demand, attendees won't have to pick and choose this year. Some of the speakers will be available for live question/answer sessions following their presentations. And like the physical show, attendees will receive certificates indicating the number of hours of training received at PCB West.

The exhibitors will be there of course, too. We are grateful to the many companies using this event as a chance to reach new customers. We also welcome the Printed Circuit Engineering Association, the trade group launched earlier this year (and in the interest of disclosure, I'm a director), which will be on hand to talk about its plans for promoting the printed circuit engineering profession.

While I'm on the subject, two of the contributors to this month's issue are also speaking at PCB West Virtual 2020. Mark Finstad will join co-Flexperts columnist Nick Koop in covering the gamut of flexible and rigid-flex circuits, from material selection and cost drivers to design tips for better physical and electrical performance. And Lee Ritchey will give a pair of five-plus-hour tutorials on power delivery system design and stackup design.

I firmly believe that when the threat of Covid-19 has been mitigated, we will go back to populating offices and factories, and will do so gladly. Same goes for making sales calls and plant visits, and yes, going to industry events like conferences and trade shows. It may not occur immediately, but over time it will happen.

We aren't there yet, unfortunately, at least not in the United States. Yet training and education must go on. Companies must get to know potential vendors, and designers and engineers must continue to expand their networks. Trade shows remain a highly effective way to do that.

So, with apologies for the promotion, I hope readers from around the world take advantage of this one-of-a-kind opportunity to hear and learn from the best our industry has to offer at PCB West Virtual 2020 in September.

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PCDF People

Bowman promoted **Jeffrey Korpus** to manager of the company's Standards business Unit. He formerly was project manager and support engineer with responsibility for new standards design and team management, and managed Bowman's quality system.

Charles Pfeil has released the second version of his e-book on *High-Speed Constraint Values and PCB Layout Methods,* available at pcdandf.com.

MacDermid Alpha appointed **Fabio Taiana** vice president Assembly Solutions – Europe.

Sierra Circuits named **Roy Alcus** director of manufacturing.

PCDF Briefs

The Air Force Research Laboratory will allocate $154 million to **NextFlex** to fund flexible hybrid electronics research for 3-D printing.

Bold Laser Automation shipped a LPW2424 laser precision welding system.

Dongguan Tanjin Electronic Technology will invest $28 million to build an Al-based Cu-clad foil production project in the Chongqing Western Electronic Circuit Industrial Park in China. Annual output value is expected to reach $85 million.

Huangshi Guanghe Circuit has begun construction on a new PCB fabrication plant in Hubei Province.

IPC membership has voted to accept a new addition covering medical devices to the industry standard for bare board qualification and acceptability following industry review. IPC-6012 Medical Device Addendum should be ready by the end of this summer, says the task group chairman, Jan Pedersen of **Elmatica**.

IPC and the **HDP Users Group** signed a memorandum of understanding enabling a partnership, increased technical collaboration between groups, and a mutual path toward emerging and disruptive high-density interconnect technologies.

Isola has officially opened an expanded R&D and analytical services laboratory at the company's new global headquarters in Chandler, AZ.

Matrix USA received a trademark registration for its Europads PCB lamination press pads.

MFS Technology has completed the first phase of a major expansion of its flex circuit plant in Yiyang, Hunan, and will launch volume production this month.

Rogers named **Krayden** distributer in the US.

UPMG Announces Technical Sessions for PCB West Virtual 2020

ATLANTA – UP Media Group announced more than 40 technical sessions – totaling more than 125 hours – have been selected for PCB West Virtual 2020 this fall. The conference, which is moving to an online platform because of the novel coronavirus, takes place Sept. 7-10.

This year's conference features a pair of extended talks from Lee Ritchey on power delivery system design and stackup design, two talks from Dr. Eric Bogatin, and three full days of classes from Rick Hartley. The conference covers everything from RF/microwave and mixed-signal design, circuit grounding, understanding material choices, flex circuits, signal and power integrity, to fabrication and assembly processes. Talks are aimed at the spectrum of backgrounds, from novice to advanced.

"Like most conferences, we are putting the safety of our speakers and registrants ahead of any other priority. That said, we are elated to bring the best of the industry together for this unique technical conference," said Mike Buetow, PCB West conference director and editorial director, UPMG. "Even those with severe travel restrictions will be able to participate in this year's show. We will have more than 125 hours of training available – and the best part is, since it's all on-demand, attendees won't have to pick and choose which presentations to see."

"As an added bonus, some of the speakers will be available for live question/answer sessions following their presentations," Buetow added.

New presentations will be made available throughout the week and will be available on-demand for 30 days. Attendees will receive certificates indicating the number of hours of training received at PCB West.

PCB West annually provides a conference and exhibition focused on the design and manufacture of PCBs, HDI, electronics assembly and circuit board test. For more information about PCB West, visit pcbwest.com. (MB)

IPC, IAEG Encourage Use of IPC-1754 in Aerospace, Defense Industry

BANNOCKBURN, IL – IPC and International Aerospace Environmental Group issued a joint statement encouraging use of IPC-1754, *Materials and Substances Declaration for Aerospace and Defense and Other Industries,* in the aerospace and defense industry and its global supply chain.

Obtaining data from the supply chain to support chemical content reporting for article (hardware) products remains challenging and resource-intensive for industries such as aerospace and defense, the trade groups said. Increasing use of materials and substances declaration standards promotes efficiency in obtaining such data, however.

The standard, which is voluntary, supports data acquisition for various substance reporting requirements for article products, including data required by the EU's Waste Framework Directive for reporting to the SCIP database. Under the WFD, European article suppliers subject to SVHC reporting under REACH Article 33 will also be required to report SVHC data to the SCIP database. However, SCIP reporting will also require additional data elements such as material and product identifiers.

IPC-1754 supports all data elements needed for reporting to SCIP. In support of SCIP reporting, IPC is developing guidance for using IPC declaration standards when acquiring the necessary data. IAEG is also developing supporting general information for the use of IPC-1754 and related IAEG-developed tools in the AD industry supply chain, available on the IAEG website. (CD)

SEMI AMERICAS EVENTS

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The **Technology Leadership Series of the Americas** is a collection of seven major events representing the various technology communities in our industry. These programs connect the 2,300+ member companies and over 1.3 million global professionals to advance the technology and business of electronics manufacturing and the design-supply chain.

There are numerous ways for you to participate in these events to connect with the industry and grow your business.

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SAVE THE DATES

FOR THESE 2020-2021 EVENTS

Explore these upcoming programs and fill out the Interest Form on each website to get connected for the latest event updates.

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semi.org/connect/events

Panasonic will ramp up its production of 5G circuit board material in China.

PCD&F opened its 2021 New Product Introduction Awards for printed circuit board fabrication.

Z-zero signed an agreement for **Mentor** to distribute its Z-planner Enterprise padstack design software worldwide starting in July.

CA People

Escatec named **Patrick Macdonald** chief executive.

Intelligent Manufacturing Solutions (IMS) named **Jim Barry** director of business development. His experience includes 14 years as president of Eltek USA and seven years in executive positions at Strataflex.

Kimball Electronics promoted **Steve Korn** to president of Global Electronics Manufacturing Services Operations, and **Lee Kemper** to vice president of Diversified Contract Manufacturing Services.

Libra Industries appointed **Trever Winters** VP of operations at its Dayton, OH, facility. He has experience as master scheduler, supply chain analyst, and most recently site manager.

Moog named **John Hengst** SMT manufacturing engineer.

Mostafa Aghazadeh of Intel has been elected chairman of the iNEMI board of directors.

National Circuit Assembly named **Wade Owens** CFO. Owens brings more than 20 years of management experience in the financial and banking sectors.

Ning-Cheng Lee, Ph.D., VP of technology at Indium, and **John Lau, Ph.D.**, CTO of Unimicron, have coauthored *Assembly and Reliability of Lead-Free Solder Joints.* The book covers Pb-free solder joints for advanced reliability across the food chain of electronics products.

SMTA announced **Martin Anselm** has been elected president for the term 2020-2022.

TestEquity named **Dan Stewart** chief marketing officer and **Nick Hawtrey** CFO.

VJ Electronix appointed **David Hamel** director of global sales and marketing. He joins VJ from Boston Semi Equipment, where he served as vice president of sales.

Benchmark Adds Fab Shop in Phoenix

PHOENIX – Benchmark Electronics has joined the ranks of vertically integrated manufacturers with its new 122,000 sq. ft. state-of-the-art factory in Phoenix. The end-to-end process encompasses a dedicated design center, board fabrication, assembly and test, highlighted by a state-of-the-art factory 4.0 lights-out SMT line.

The plant, which houses a Benchmark Lark Technology team, as well as other Benchmark operations, celebrated its grand opening in June.

It is the fourth greenfield fabrication plant built in the US in the past 20 years, the others being Whelen Engineering's captive shop, which opened in 2015; GreenSource Fabrication, which launched in 2018; and TTM's new plant in Chippewa Falls, built in a converted 20-year-old, 40,000-sq. ft. warehouse and officially opened last winter.

Benchmark is the fifth-largest EMS company in the US and 18th in the world, according to the CIRCUITS ASSEMBLY Top 50.

The fab shop features automated plating for copper and final finish, laser-direct imaging (LDI) and an automated MSAP line capable of producing 1 mil (25 micron) lines and spaces. The company has two laser drills and two mechanical drills, with the lasers capable of microvias to 2 mils, while the mechanical drill capability is currently 6 mils, with the expectation it will reach 4 mils later this year. Sequential lamination processing is standard. Final finishes include ENIG, ENEPIG and EPIG. Benchmark can process a variety of laminates, including rigid, polyimide, BT, high-performance blends, LCP, PTFE, and mixed-material hybrid constructions. Legends are screened, with inkjet planned for later this year.

A big part of the site investment was the ISO 7 and 8 cleanrooms, adds Kevin Walker, product line director, RF & High Speed Circuits at Benchmark Lark. Inventory is kept in the cleanroom.

While the company had manual plating as part of its partnership with HSIO that started in 2018, the Phoenix plant upgraded to automated copper for direct plate and final finish for precision deposition control.

The MSAP process will enable size, weight, performance and cost (SWPC) improvements for many end-markets, with a focus on aerospace and defense customers, who are "enthusiastic supporters of what we are doing," said Walker.

The SMT area includes a volume production line, with an NPI line to be installed by the end of the year. Benchmark installed 3-D x-ray, Sonoscan micro-acoustic imaging, a laser confocal microscope for surface analysis, and performs microwave test up to 110GHz.

Daniel Everitt, vice president, Benchmark Lark, says the fab shop gives Benchmark "the opportunity to eliminate superfluous packaging, achieve high-reliability designs and performance for our customers, as well as mixed technologies where we mix an SMT and microelectronics assembly to create a hybrid module, which is commonly used in space, military and defense applications for the most highly demanding scenarios, as well as the highest reliability scenarios."

While Arizona is not a water-rich state, the shop has closed-loop treatment systems for air and water.

The site will build bare boards for both OEMs and other EMS companies. (MB)

IPC Releases New Press-Fit Connector Standard

BANNOCKBURN, IL – IPC announced the release of a new standard for the qualification and acceptance of press-fit technology. IPC-9797, *Press-fit Standard for Automotive Requirements and Other High-Reliability Applications* also includes high-reliability needs for automotive and other industries such as aerospace.

Press-fit technology is relatively new to the automotive industry and high-reliability needs but not to electronics, IPC said. Used primarily in the telecommunications industry, the dependability and efficiency of press-fit makes it stable for use in high-reliability electronics.

The technology has been found to be critical to the manufacturing of electronic and electro-mechanical components. (CD)

PCB Chat

Recent Chats:

Kevin Walker on Benchmark Lark Technology's new fabrication/assembly plant

InspectAR on electronics debugging tools

Wally Rhines on the latest PCB design tools market trends

Christopher Tang, Ph.D. on supply chain changes in the Covid era

upmg.podbean.com

The PCB Podcast

CA Briefs

A bipartisan pair of US senators have introduced a bill to restore semiconductor manufacturing to American soil by increasing federal incentives to stimulate advanced chip manufacturing, enable cutting-edge research and development, secure the supply chain and bring greater transparency to the microelectronics ecosystem.

ASE Technology, Powertech, SPIL and Amkor plan to take advantage of incentive schemes recently announced by the Indian government to set up semiconductor packaging and test services in the country.

Acer is seeing shortages of components, including passive components, ICs and panels by around 30% due to surging orders from the end-market, according to co-COO Tiffany Huang.

Adco Circuits has developed a free instant costing tool for circuit board assemblies that takes a bill of material and outputs a price with complete unit costs.

AIM Solder opened a stocking facility in Manaus, Brazil.

Benchmark Electronics will close its plant in Angleton, TX, in the first half of next year.

Capital Partners completed a control investment in **MicroCare** in partnership with the company's cofounder and senior management on May 28.

Cascade Systems is moving its EMS supply chains from China.

Charles Edward Industries plans to invest $1.5 million in a new EMS plant in Asheville, NC, over the next three years.

CheckSum named **Horizon Sales** representative in Michigan, Ohio, Indiana, Kentucky, Western Pennsylvania, Illinois, Eastern Iowa, Wisconsin and Florida.

CIRCUITS ASSEMBLY is now accepting entries for the 29th annual Service Excellence Awards (SEAs) – the premier awards program in electronics manufacturing.

Cobham Advanced Electronic Solutions sold its radiation testing unit to **Radiation Test Solutions.**

Critical Manufacturing appointed **SDG** manufacturers' representative in Italy, Malta and Albania.

DataED and **Bestronics** announced a merger to form **Emerald Electronics Manufacturing Services (Emerald EMS).**

Datest is acquiring a second **Spea** 4060 flying probe tester.

Dichaba Consumer Electronics opened an electronics assembly facility at the Botswana Innovation Hub.

East/West Manufacturing purchased a **Nordson Select** Cerno 103IL selective soldering system.

ECD has developed a five-module course that provides electronic assembly specialists with an overview of thermal profiling basics (ecd.com/electronics/courses/thermal-profiling-course/thermal-profiling-m0.aspx.).

Enics will open a 10,000 sq. m. high-volume electronics manufacturing facility in Senai, Malaysia, in early 2021.

Foxconn aims to improve its gross margin from a current 6% to 10% in 2025. It also set up its own research center to work on new technology, including 5G telecommunications, artificial intelligence and cybersecurity.

Foxconn is planning further investment in India and may announce details in the next few months. **Foxconn, Wistron, Flex, Samsung, Oppo and Vivo** are likely to apply for a production-linked incentive scheme (PLI) worth Rs 41,000 crore as part of India's massive push to wean away companies from China and emerge as the world's hub for electronics production.

Gentec purchased a **MIRTEC** MV-3 Omni 3-D AOI.

A smart manufacturing trial base in central Taiwan will progress from experimental production for components to technological verification of smart manufacturing solutions, according to the **Intelligent Machinery Technology Center.**

Johnson Outdoors installed a **Nordson Dage** Assure x-ray component counter.

KIC is integrating its profiling technology into **SMT Thermal Discoveries'** vacuum reflow oven and standard reflow machines. It also appointed **Technical Marketing Company** manufacturers' representative in Colorado, Utah and Idaho.

Lockheed Martin purchased an **Austin American Technology** X30-A vertical cleaning system.

The Manufacturing Technology Centre (pictured) has developed the first stage of Europe's first smart factory demonstration for the manufacture of electronics assemblies.

Nokia became the first major telecom equipment maker to commit to adding open interfaces in its products that will allow mobile operators to build networks that are not tied to a vendor.

Nordson Select named **Fuji Do Brasil** sales representative for the Select product line throughout South America.

One Equity Partners will acquire the **Sparton** EMS business for an undisclosed amount from **Cerebus Capital Management.** The transaction is expected to close during the third quarter, subject to regulatory and customary closing conditions.

Out of the Box Manufacturing purchased a **MIRTEC** MV-6 Omni SPI.

Pegatron is renting a plant in Vietnam that will go online in early 2021, and **Qisda's** chief executive said the firm is constructing a new factory there as well. Pegatron will gradually boost its non-China production ratio to 10 to 20% by 2021.

Scanfil EMS is selling its subsidiary **Scanfil (Hangzhou) Co.** for €18.4 million to **Hangzhou** Cabinet Technology, a mechanics manufacturer.

SMT Northwest purchased a **MIRTEC** MV-3 Omni desktop 3-D AOI.

TT Electronics' Global Manufacturing Solutions division is opening operations in Kuantan, Malaysia, in response to customer demand for an additional manufacturing center in Asia.

Yamaha Motor Europe Factory Automation appointed **Routeco** distributor of industrial robots and associated controllers and accessories in the UK.

Z-Axis installed an **ITW** Speedline MPM/SPM stencil printer and two updated **Mycronic** MY9E pick-and-place machines.

The MTC in Coventry, England.

IPC CLASS 3 DESIGN GUIDE

SIERRA CIRCUITS

- Introduction
- What is IPC?
- Class 1, Class 2, and Class 3 PCBs
- IPC Guidelines for Manufacturing Defects
  - IPC Standards for Annular Ring
  - Design Rules for Annular Rings
- IPC Standards for Assembly Process
  - IPC Standards for Solder Joints
- Common Differences Between IPC Classes
- PCB Cross-Section Verification
- IPC Documents to Set the Level of Acceptance Criteria

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METALS INDEX

CALM BEFORE THE STORM?

Trends in the U.S. electronics equipment market (shipments only).	% CHANGE MAR.	APR.	MAY	YTD%
Computers and electronics products	-0.7	0.5	0.5	0.9
Computers	-4.1	-0.2	0.7	-12.6
Storage devices	0.2	-2.8	-0.2	57.4
Other peripheral equipment	-3.2	2.8	9.4	5.2
Nondefense communications equipment	2.9	-0.2	0.9	5.8
Defense communications equipment	0.4	3.5	3.4	-3.7
A/V equipment	-8.4	5.3	1.4	-19.0
Components[1]	-0.9	1.9	0.8	8.8
Nondefense search and navigation equipment	-1.3	-1.3	-0.9	-6.5
Defense search and navigation equipment	0.0	0.3	0.2	3.5
Medical, measurement and control	-0.9	-1.1	0.0	-4.1

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, July 2, 2020

US MANUFACTURING INDICES

	FEB.	MAR.	APR.	MAY	JUN.
PMI	50.1	49.1	41.5	43.1	52.6
New orders	49.8	42.2	27.1	31.8	56.4
Production	50.3	47.7	27.5	33.2	57.3
Inventories	46.5	46.9	49.7	50.4	50.5
Customer inventories	41.8	43.4	48.8	46.2	44.6
Backlogs	50.3	45.9	37.8	38.2	45.3

Source: Institute for Supply Management, July 1, 2020

KEY COMPONENTS

	JAN.	FEB.	MAR.	APR.	MAY
Semiconductor equipment billings[1]	22.7%	26.6%	20.1%	18.2%[r]	13.1%[p]
Semiconductors[2]	-0.35%	5%	6.85%	6.13%[r]	5.84%[p]
PCBs[3] (North America)	1.05	1.15	1.15	1.19	1.10
Computers/electronic products[4]	5.42	5.41	5.43	5.44[r]	5.43[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

Hot Takes

- The **worldwide contract manufacturing services market** increased 2.5% year-over-year in total revenue to $555 billion. The EMS/ODM market expanded $13 billion from 2018. For the 10th year in a row, the CM industry was profitable, at $6.8 billion (for 34 EMS public companies and 17 ODM public companies), decreasing by $900 million from 2018. Foxconn accounted for more than half of all the earnings of the EMS industry in 2019, at $4.3 billion. (New Venture Research)
- **PCB sales among German, Austrian and Swiss fabricators** rose 16% sequentially in the first quarter but fell 7.5% year-over-year. (ZVEI)
- The Covid-19 pandemic effect on numerous end-products slowed **the growth rate for HDI** in the first quarter. Taiwanese high-end HDI makers suffered relatively minor impact, however, as the HDI sector grew 7.5%. (TPCA)
- **Worldwide spending on the Internet of Things (IoT)** has been significantly impacted by the economic effects of the Covid pandemic, although a back to double-digit growth rebound is expected both in the mid- and long-term. (IDC)
- **Memory spot prices,** particularly for DRAM, have started to rise, reflecting a pickup in buying momentum prior to China's 618 shopping festival.
- **The AR/VR/MR industry** is predicted to top $30 billion by 2030, in part from an uptake of devices for use in everyday life. (IDTechEx)
- **Vendor revenue in the worldwide server market** declined 6% year-over-year to $19 billion during the first quarter. (IDC)
- **2021 is poised to mark a banner year** for global fab equipment spending with 24% growth to a record $68 billion, 10% higher than the previously forecast $66 billion. (SEMI)
- **Exports by the German electronics industry** in April plummeted 20% compared to the previous year to 13.5 billion euros. (ZVEI)

Covid-19 has Forced Us to Change. Will It Stick?

We must retain our new agility even after the pandemic ends.

NOTHING MAKES YOU flexible like a crisis. Yet, as rough as it can be for a person to quickly shift gears, it is significantly more daunting for a corporation to do so.

The entirety of my working career, the mantra of any good business consultant or culture guru has been be flexible and embrace change. Whether an organization is implementing a TQM (total quality management) plan or struggling with financial survival because "plan A" no longer works, embracing flexibility and rapid change is never easy – and often unsuccessful. The larger the organization, the harder it can be. Embracing change and becoming flexible often only occurs when no other option remains, or in short, extinction awaits.

In these most unusual times of Covid-19, however, most people and virtually every company have been forced to embrace radical change overnight. Some change is cultural. To wit: Where employees work and how they communicate has stretched some companies much further than they could have imagined a few short months ago. For instance, large, centrally located staffs have reconstituted in home offices. Restaurants now are embracing outdoor seating and simplified, modified menus. And everyone, in one form or another, has become more open to wearing masks, shopping following in-store traffic patterns, and greeting friends with elbows rather than handshakes. All this change has been rapid, requiring flexibility of thought and action.

As extraordinary as these cultural changes are, some large corporations have demonstrated they can make an elephant dance. Indeed, the ability of some companies so rigid they have the flexibility of a steel I-beam, in industries that traditionally take years to "change," has radically changed what they produce to support the common good of fighting Covid-19 virtually overnight.

The auto industry has a deserved reputation for moving relatively slowly. It typically takes years for an automaker to develop new technology, tool it and produce it. However, Ford and GM, companies not known for producing medical equipment, rapidly converted manufacturing facilities, bringing them up to medical standards (read: cleanroom environment), tooled, and are successfully producing ventilators. Fiat-Chrysler was not left out; they produced many of the parts that go into ventilators made by Ford, GM and others. If these industrial behemoths can show the flexibility and the appetite for such radical change, imagine if they harness those traits when rolling out the next generation of automobiles.

They are not alone. Bacardi, Brown & Forman, and LVMH – companies known for their spirits and wines – have entered the hand sanitizer business. These companies, as well as cosmetic companies such as L'Oréal, have shifted gears to new, very different product lines and rapidly scaled to volume production.

S.C. Johnson and Dow, two major chemical companies with a good number of overlapping/competitive products, started to work together to produce hand sanitizers and wipes in volume to stock medical facilities and home consumers. Competitors working together with employees who have the flexibility to shift production and share technical data again demonstrates how rapid change can be.

Face mask production has been the catalyst for virtually every clothing company of late. A corporate neighbor of mine is a supplier to Brooks Brothers, the high-end clothing store. It converted a factory for making shirts into one for masks over a weekend. Other clothing suppliers, which served everyone from high-end boutiques to Walmart, rapidly and successfully converted manufacturing to masks and medical garments. Whether homemade over a kitchen table or produced in mass by a large clothing manufacturer, countless people and businesses embraced change and demonstrated flexibility.

Our electronics industry always needs to be nimble and flexible, as the technologies we are involved with constantly change. Our usual rate of change is nothing compared with what's required to fight a pandemic, however. With scores of electronics firms now producing medical equipment and ventilators, and so many in their supply base providing the chemicals and raw materials necessary to get the job done, ours is among the markets embracing real change.

A vast majority of people and companies across the globe have had to react to the realities of this pandemic. Flexibility is the common trait we have all embraced. Change, painful as it is at times, is the desired result of exercising flexibility. When our lives finally return to a semblance of normal, however, which companies or industries will leverage the lessons learned and adapt them into their corporate culture – their business approach – for competitive advantage?

We have all been witness to sudden and rapid change, and our flexibility has been exercised and stretched. Those who take to heart the advantages that can be realized by staying nimble, being flexible, and embracing – rather than avoiding – change, personally as well as throughout the organization, have the best chance of long-term success. ▫

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The Covid-19 Sales Challenge

With travel frozen, rethink and repurpose those marketing dollars.

BY MAKING FACE-TO-FACE sales calls impossible, Covid-19 is challenging electronics manufacturing services (EMS) salespeople to work in new ways. Sadly, that challenge isn't likely to go away soon. On the bright side, it opens the door to a more productive, less costly sales and OEM relationship, provided salespeople modify their approach.

In the normal flow of EMS selling, there is typically a lead follow-up phase that results in a face-to-face sales call. There may be an additional meeting to present a quotation, depending on the distance between the salesperson and decision-maker. There is also usually a plant tour. When all these activities are local, costs drop to the amount of time the individuals spend on the activity. However, the cost of a sales call that involves business travel may be $1,000 to $2,000, depending on mode of travel and how many sales calls are clustered into that trip.

> "If travel is not an option, repurpose part of that budget into **lead-generating marketing.**"

In the era of Covid-19, most companies are significantly limiting sales calls. The ability to reduce the cost of a sales call by visiting several companies at once is no longer doable. Salespeople who focused primarily on showing up hoping to get an appointment aren't even allowed in the lobby. Many companies are also restricting employee travel, which means plant tours aren't happening. An added challenge is employees who can work at home are encouraged to work at home, which makes prospects harder to get on the phone.

Therefore, salespeople need to work smarter to both open the door to opportunities and close the sale with a plant tour. Here are a few suggestions on how to creatively approach this challenge:

- Evaluate the contacts in your prospect database. Covid-19 has changed the sourcing strategy playing field, and OEMs have different criteria now. Companies that weren't interested in your EMS company six months ago may be now. Additionally, the prospects in that database have some level of preexisting relationship, which makes opening the door a little easier.
- Remind the prospects in your database you are out there. The rules about mindshare maintenance haven't changed. OEMs will focus on the EMS companies that stay in touch with them.
- Tie your messaging to points of pain. What is likely to keep prospects up at night in a Covid-19 world? Closed factories, resource shortages that delay deliveries and challenges in transferring production are likely to be the top three. Build your message around your company's ability to solve those challenges.
- Create a Skype plant tour. While some OEMs may be happy with a marketing video alone, convincing them to take a plant tour via Skype will enable your team to build a relationship during that tour. However, having someone in the plant wander around with a smartphone is likely to be a disaster. So, create a repeatable format and use someone capable of providing strong visuals and talking the prospect through the tour. Do a dry run before doing it with a prospect to make sure the right person conducts the tour. Keep reasonable time limits, show the right areas of the factory, and point the phone in the right direction.
- Listen to your prospects. Everyone is navigating Covid-19 challenges. What parts of their sourcing analysis process are they having difficulty doing right now? Can your team develop a "virtual" way to provide the answers they need? Every time you help a prospect solve a challenge, you build a stronger relationship.

These are the times that test salesmanship skills. Salespeople with a consistent approach that builds off a network of contacts will navigate Covid-19 challenges. If travel is not an option, consider repurposing part of that budget into lead-generating marketing activities. The entities that normally have trade shows have switched to webinars and other virtual networking venues, so there are opportunities to rethink marketing activities. Consider creating short podcasts or videos that involve conversations with your company's technical resources on issues they've solved for customers for distribution via social media. In short, figure out creative ways to do the things virtually that you used to do face-to-face.

We are looking at a challenge that will likely change the way sales are done for the next year. Pivoting to virtual solutions earlier will open the door to more opportunities and position your company as a creative problem-solver. ▫

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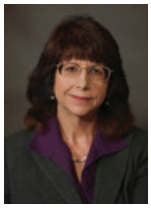

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written by

Charles Pfeil

Charles Pfeil has spent over 50 years in the PCB industry as a designer, owner of a service bureau, and in engineering management and product definition roles at Racal-Redac, ASI, Cadence, PADS, VeriBest, Mentor Graphics, and Altium. He was the original product architect of Expedition PCB.

Generating PCB Footprints for Your First Layout

And why your library naming convention should be memorable.

AS A DESIGNER who has put himself into the public eye, a lot of questions come my way. Several beginners have approached me with basic questions I can usually answer by sharing something I've already written. Sometimes I'll end up writing a few paragraphs that eventually expand into a column to share with everyone. One gentleman, whom I will call Aakash, has leaned on me so many times I think he might be compiling a book. The messages pile up, as do the answers. Let's get to one of those types of answers.

More than one person has asked about starting their first job going from the ground up. "How do I make all the parts I need for my first board?" The short answer is to build them one at a time. This is the internet age. This is the 21st Century. There must be a better way! It's not that we're impatient; we just don't have that kind of time. Software vendors know that, and the internet does too. The software installation comes with a bevy of common parts, but most boards go well beyond the generic SMD capacitors and resistors found in the default library.

You have it so good. In "my day" we finished a layout and saved it to a floppy disk. We walked it over to Document Control, and they put it in a file cabinet. Some veterans may be nodding. For you kids, a floppy disk looks like the icon we use for saving our designs, but that's a story for another time. Now get off my lawn!

The library must start somewhere, and most PCB layouts start at the connector, so I'll start there. Connectors are like snowflakes, more or less by design. You can find at least 100 different circuits that fit on a QFN-16. That's a square with 16 pins spaced maybe a half a millimeter apart with a center ground pad. Meanwhile, every connector mates to only one other connector. An SMA connector doesn't work with an SMB socket.

FIGURE 1. The PCB layout can only be as good as the underlying footprints all the way down to the padstack where it all begins.

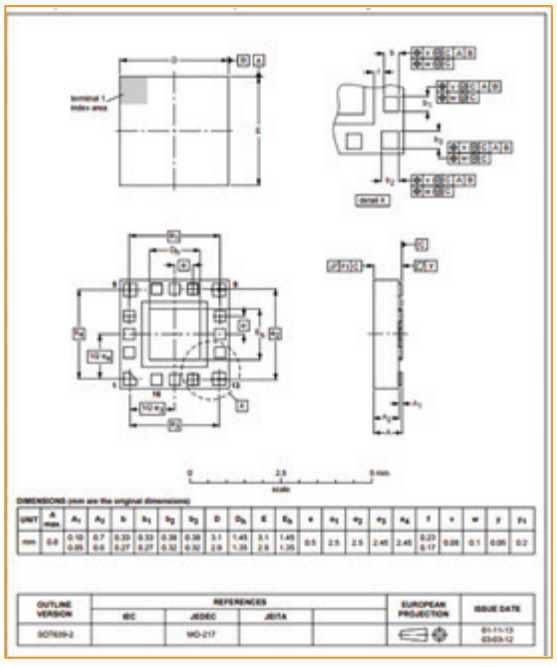

FIGURE 2. One of the most common SMD packages is the QFN, quad flatpack no lead, as opposed to QFP, which has gull wing leads protruding from the body. Credit: Reference Designer.

Why connector catalogs are so byzantine. Worries over patent infringement and protecting their turf work against the connector vendors. I don't expect them to ever standardize on the particulars. The proliferation of connectors is further complicated by the way connectors are documented. You will never find a drawing of the connector you need. What you will find is a representative image used for the entire connector family. Everything from two pins to 300 is represented by that single drawing. Then you get to decode the part number to find the actual body dimensions. Up to 17 pins, it's one row, 18 to 80 is two rows, then three and so on (**FIGURE 3**). Turn to some other page that indicates what the plating letter means. Another table breaks down whether there are zero, one, two or more alignment pins. Go to still another page to find out if your mating connector locks down mechanically or relies on friction. Do you want tape-and-reel? Or is a tray okay?

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Coming to this from the component selection side is the same thing in reverse. You build that part number one character at a time. When finished, you get to contact the vendor to see if it is a standard part or if you get to wait six weeks and pay some nonrecurring engineering fees. Maybe you have to roll the dice again. All for the pleasure of buying some connectors. I just love connectors, and they're on almost every board. I'll try capacitive charging with an array of antennas and still get a swath of board-to-board connectors.

A brief history on library generation. Back in the era of floppy disks, I had catalogs from Amp, Samtec and others to suss out the details. The best ones were from Texas Instruments. One fine day, a new PCB designer rolled into an empty space we called a "cubicle." As he unpacked his box, I couldn't help but notice a large number of UPS-Brown paperbacks that were all identical except for minor variations in width. He owned the entire Encyclopedia Motorola! I didn't even know his name, but I already liked him. Those items were a status symbol to me at least. My generation got tired of lugging all those books around, so we invented the internet.

That's where you come in. Do you want to slog through those books and piece together a component footprint one padstack at a time? Ask your vendor(s) if they can part with more than a .pdf file and provide a CAD file in your preferred format. Some will offer files for a specific ECAD tool or a STEP model to import. Others may be old school and deal only in .dxf files. Either way, you have a leg up on starting from scratch with the "wizard." Verifying the right geometry is still up to you.

FIGURE 3. The 2020 Hirose pamphlet. If you want to build the part, be ready to turn some pages.

Library naming conventions. No matter how you approach library generation, a naming convention is a must. As your library grows, it's possible to spend more time browsing for an existing part than it would take to build it again. IPC-7351 to the rescue. Each revision of this document goes into a little more depth to cover the millions of different footprints and the various ways they will be built.

Circling back to the QFN, a typical file name is as follows: QFN50P_300x300_16_150x150. The newer revision of the document will include another character or characters to define the footprint in greater detail. The point is to stick to a system. If you're starting with chaos for file names, then you want to make renaming your symbols part of each design effort, one board at a time. Twenty percent of the parts cover 80% of the board, so it gets easier as you go.

IPC-7351B, page 17, gives a flavor for how to create footprints in such a way they can be searched by their parameters (**FIGURE 4**). One of the most important characteristics is footprint size: small, medium or large. For everything but Class 3 high-reliability work, I recommend the nominal size, rather than over- or undersize footprints. If big pads present an impedance issue, or the boards are very high-density, it could be useful to minimize size. The Ghostbusters tell us to "never cross the streams"; I'm telling you to never mix the minimum, nominal and maximum size component footprint types. Bad things can happen if you commit either of those sins on the same board, especially with the same part.

COMPONENT, CATEGORY	LAND PATTERN NAME
Thin Quad Flat Packages, 0.50 mm Pitch, Height ≤ 1.60 mm	**TSQFP50P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty
Thin Quad Flat Packages, 0.40 mm Pitch, Height ≤ 1.60 mm	**TSQFP40P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty
Thin Quad Flat Packages, 0.30 mm Pitch, Height ≤ 1.60 mm	**TSQFP30P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty
Ceramic Quad Flat Packages, 1.27 mm Pitch	**CQFP127P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty
Ceramic Quad Flat Packages, 0.80 mm Pitch	**CQFP80P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty
Ceramic Quad Flat Packages, 0.635 mm Pitch	**CQFP63P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty
Quad Flat No Lead Packages 0.80 mm Pitch	**QFN80P** - Body Width **X** Body Length in Metric - Pin Qty + Thermal Pad
Quad Flat No Lead Packages 0.65 mm Pitch	**QFN65P** - Body Width **X** Body Length in Metric - Pin Qty + Thermal Pad
Quad Flat No Lead Packages 0.50 mm Pitch	**QFN50P** - Body Width **X** Body Length in Metric - Pin Qty + Thermal Pad
Quad Flat No Lead Packages 0.40 mm Pitch	**QFN40P** - Body Width **X** Body Length in Metric - Pin Qty + Thermal Pad
Quad Leadless Ceramic Chip Carriers (JEDEC Standard Package)	**LCC** + Body Width **X** Body Length in Metric - Pin Qty
Quad Leadless Ceramic Chip Carriers (Pin 1 on Side)	**LCCS** + Body Width **X** Body Length in Metric - Pin Qty
Quad Bottom Chip Carrier (JEDEC MO-217B)	**QBCC** + Body Width **X** Body Length in Metric - Pin Qty
Resistors, Chip	**RESC** + Body Size in Metric
Resistors, Chip, Array	**RESCA** + Pitch P + Body Width X Body Length in Metric - Pin Qty
Resistors, Molded	**RESM** + Body Size in Metric
Resistors, MELF	**RESMELF** + Body Size in Metric
Small Outline IC, J-Leaded 300, 350, 400, 450 mil Body Width (Pitch 1.27 mm)	**SOJ127P** + Lead Span Nominal - Pin Qty
Small Outline IC, J-Leaded (Pitch 0.65 mm)	**SOJ65P** + Lead Span Nominal - Pin Qty
Small Outline Integrated Circuit, 1.27 mm Pitch (Standard 50 mil Pitch SOICs)	**SOIC127P** + Lead Span Nominal - Pin Qty
Small Outline Packages, 1.27 mm Pitch (Nonstandard 50 mil Pitch SOICs)	**SOP127P** + Lead Span Nominal - Pin Qty
Small Outline Packages, 1.00 mm Pitch	**SOP100P** + Lead Span Nominal - Pin Qty

FIGURE 4. IPC-7351B gives a flavor for how to create footprints searchable by their parameters.

It doesn't take a hero to curate a good library. Help is available. A number of companies will generate library parts by subscription or piece-

continued on pg. 28

Reliability Needs to be Designed-In from the Lowest Level

Cutting-edge technology demands more care to ensure reliability and resilience.

HUMAN NATURE IS to invent, to create technological solutions to the challenges and problems we see. We are increasingly dependent on high-technology solutions as we address more complex issues. Some of these issues are of our own making. Others arise from our increasing expectations: what we want to do, where we want to go, how safe we want to feel.

All this keeps the electronics industry extremely busy. And the equipment we create – remote smart sensors, street-level broadband infrastructure, full-color digital signage, supercomputers on wheels (or wings) – is more and more likely to be required to operate faultlessly in extreme environmental conditions. Gone is the era when advanced electronics assemblies were mostly destined to spend their lives in air-conditioned telecom offices or otherwise benign environments. Now, they are out in the cold. And the heat. And the humidity. And this presents a major reliability challenge that needs to be addressed at every level from the installation and the enclosure down to the substrate.

The effects on components caused by environmental factors such as high ambient temperatures and humidity can be obvious, often manifested as surface oxidation, corrosion, or mechanical distortion. Excessive heat can quickly dry wet electrolytic capacitors, which consequently lose their capacitance over time. The properties of substrate materials also can be liable to change with exposure to environmental factors such as moisture, as well as due to general aging. Substrates exposed to excessive humidity can absorb moisture, which increases the dissipation factor (Df), leading to more lossy behavior that saps signal energy.

Conductive anodic filament (CAF) formation is another phenomenon that gets attention within the industry, although we still have lengths to go to address the issue rigorously and properly. Still often considered a material issue, CAF performance is known to be influenced by design and process, in addition to temperature, humidity and bias. Pathways are also essential for CAF progression. As package I/O pitches continue to shrink, and component placement density continues to increase, these trends are moving against efforts to maximize reliability.

Initial observations of CAF were restricted to laboratory testing. Now, however, we are pushing equipment containing extremely densely populated boards into the field, and it needs to stand up to the environment. Recent trends in e-mobility have also moved CAF performance requirements from tens of volts to thousands of volts, bringing very real challenges in test design and equipment use.

Another modern trend is a large proportion of remotely installed equipment can be considered mission-critical. So many of us are dependent on mobile and Internet-based services to work, do our banking, authenticate our identities, and host our wallets and travel credentials, such as train tickets and aircraft boarding passes, that our world would grind to a halt if we couldn't rely on the infrastructure and sensors distributed liberally throughout the places we go. And this is without mentioning our reliance on automotive safety features and the roadside and trackside technology that support services such as signage and signaling. Looking ahead to when 5G becomes part of the mix of technologies involved in directing autonomous vehicles and remotely managing industrial automation, its capacity for massive machine-type communications (mMTC) and ultra-low-latency communications (ULLC) must come with assured reliability.

In addition, despite clear economic arguments for standardizing hardware across multiple product lines, addressing different applications and different markets, design teams should assess whether an assembly will be reliable when taken out of one context and placed in another. There is an increased tendency to create software-defined products based on a common hardware platform. While this can allow flexibility to address the needs of different markets, hardware must be designed to withstand the harshest conditions it is likely to encounter in any location it may be used. We need to be careful not to send assemblies into environments they were not designed for, in the interests of ease or financial expediency. Recall early failed attempts to migrate low-cost consumer electronics hardware to the automotive environment.

It may be relatively unexciting compared to the science-fiction lifestyles we can foresee coming within our reach. However, reliability is an issue that urgently needs to be addressed. To continue packing more components onto boards, with increasingly high-density interconnects, and continue adding features and raising system capabilities, reliability needs to be designed in from the lowest level – the properties of the substrate material – upwards.

Materials suppliers should be careful to ensure new products are tested fully. This must include properly assessing long-term reliability, such as through thermal aging tests. This can be especially important

continued on pg. 28

ALUN MORGAN
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How to Really Read a Technical Roadmap

It might be factually correct, while also being completely impossible.

QUESTION: I AM looking to add a flex circuit supplier to our vendor base and requested its technical roadmap. After review, it appears almost exactly as the two vendors we currently have. Is this a coincidence, or do most (or all) flex suppliers have the same technical capabilities?

A technical roadmap is basically a document that outlines what a company can and cannot do from a technical standpoint (e.g., minimum trace/space, layer count, pad and via size, overall circuit size, etc.). I have never been a fan of technical roadmaps. Virtually every flex (and rigid) PCB supplier is compelled by their customer base to provide their capabilities, and therefore also their limitations. The problem with roadmaps is twofold. First, every supplier advertises the absolute best it has ever done in every single category. This is true even if it only did it one time, on one circuit, and in a beaker. This is not a fair representation of what the fabricator can or cannot do on production quantities. The second problem is the real answer for what a supplier can or cannot do is "it depends." Let's look at a few examples.

Trace/space feature size. Most flex suppliers will advertise their minimum trace/space feature size at 50µm to 75µm. But these numbers are meaningless without also knowing what copper thicknesses were used to establish these limitations. If they were able to etch 50µm to 75µm features on 9µm or 12µm copper, I say welcome to the club. If they did these feature sizes on 2+ oz copper, they have something to brag about. Unfortunately, this important detail is often missing from roadmaps.

Via/pad sizes. It is practically industry standard that any supplier with a laser drill can form 75µm to 100µm blind vias and hit 250µm pads. But what happens when the circuit size increases to where the dimensional instability of the flexible material starts to wreak havoc on the locations of those vias? Drilling and imaging equipment with scaling capabilities certainly helps, but to be really beneficial, they need to be used in conjunction with sequential lamination construction. Depending on the number of lamination steps, a price tag is associated with that capability.

Layer count. As layer count increases, so does the importance of very high etching yields on internal layers. Consider the following example. Say you have an eight-layer circuit, and the supplier can get eight parts per panel. In this example, let's say your supplier averages one etching reject per layer. Theoretically, there will be panels where they may not get a good part. Murphy's Law dictates the internal etching rejects will be randomly placed on each layer and will almost never line up at a single circuit location. So, maximum layer count is a function of the feature sizes on each layer in the circuit. The smaller the feature sizes, the lower the etching yields. The more layers in the stack that have these small features (i.e., non-plane layers), the lower the overall yield. And as you probably guessed, the lower the overall yield, the higher the price.

Circuit size. This is one of my personal favorites. Most flex suppliers have at some point built relatively long (22" to 24") circuits. These are typically just one or two layers and have relatively large features. This is where proclaimed maximum circuit size on the technical roadmap can come back to bite you. Since you have indeed made a circuit 24" long, you include that on the technical roadmap. No problem, right? Then you get a Gerber package to quote where you find a 24" long and 5" wide six-layer circuit filled with 50µm lines/spaces on four of those layers. You contact the customer to let them know you will have to no-bid, and they may have difficulty finding a source anywhere that can support the application. The inevitable reply: "But the technical roadmap on your website shows this is within your capabilities."

Each feature on a technical roadmap is a standalone statement of that one capability only. When you mix and match these leading-edge capabilities, all bets are off. Again, I am not a fan of technical roadmaps because they are not indicative of the true capabilities of a supplier, or the supplier's ability to stack multiple challenging features into a single design. Rather than relying on a published technical roadmap where you can learn about the best a supplier has done, give your flex vendor a call and provide them with a two-minute "big picture" scope, including the important details. Most vendors will be able to tell quickly if you are on the right track or wandering into never-never land. □

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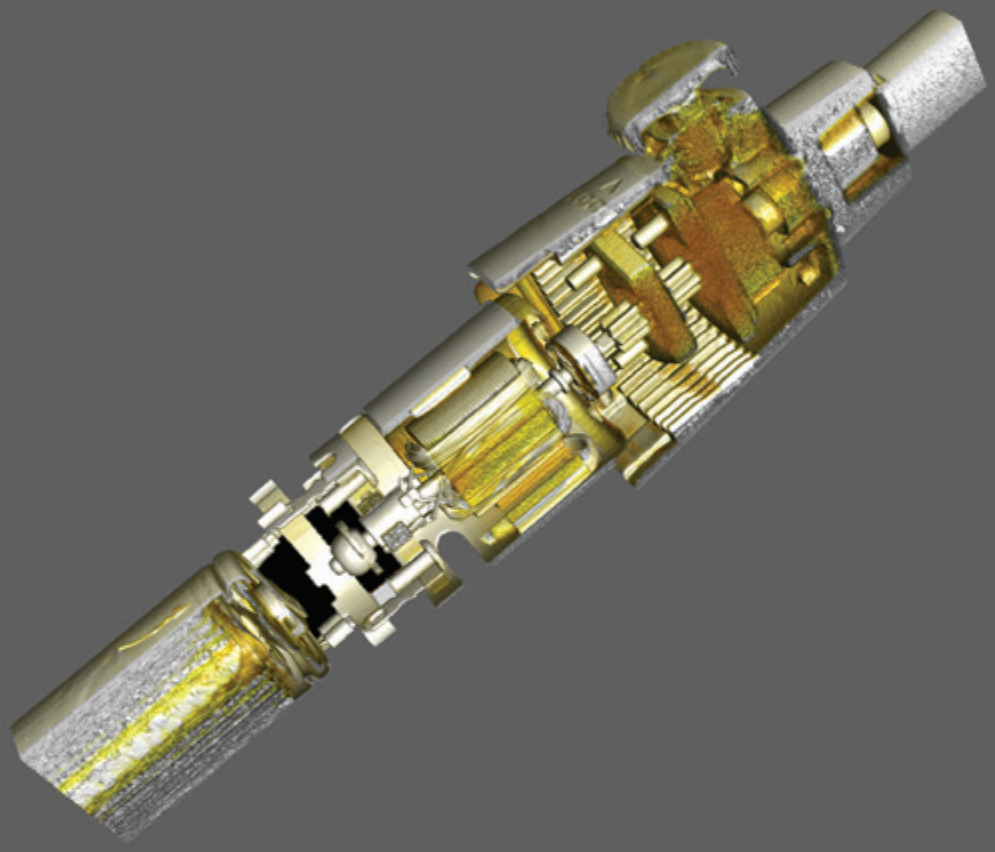

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Why Not ROUTE TWO TRACES Between Pins on a 1mm Pitch BGA?

A look at the geometry associated with plated through-holes in a PCB. **by LEE RITCHEY**

Application notes describe how to save layers in a PCB by routing two traces between pins on a 1mm pitch BGA. A leading FPGA vendor recommends this practice to use its very-high-pin-count FPGAs in a low-layer-count PCB. When this approach is used for a high-layer-count PCB, the result is often, if not always, very poor yields, and the board is unreliable when used in a system under actual conditions, as opposed to in a laboratory or a prototype built in a small volume by a specialty shop. The following discussion will illustrate why this approach results in unsatisfactory yields when volume manufacture is attempted.

To understand the space used to route traces in signal layers of a multilayer PCB (this also applies to four-layer PCBs), it is useful to look at how plated through-holes (vias) are created and the various requirements that must be met by the finished PCB. **FIGURE 1** is an illustrated cutaway of a plated through-hole showing signal and plane layers.

Deciding the dimensions of the features in this diagram is often called padstack design. (This subject is discussed at length in Ritchey.[1]) The elements in a padstack design are the finished hole size, the drilled hole size, the size of the capture pad in a signal or surface layer used to connect to traces and component leads, and the size of the clearance hole or antipad in the plane layers. Things to account for are minimum thickness of copper plating in the hole, allowance for drill wander in the fabrication process, allowance for misregistration between layers of the PCB, minimum insulation thickness between plating in the hole and metal in the signal and plane layers, and adequate copper bonding between traces and the plating in the hole.

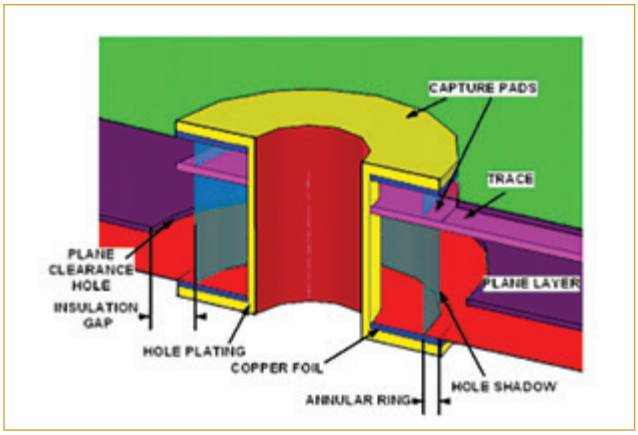

FIGURE 1. An illustrated cutaway of a plated through-hole in a PCB.

As will be seen, the dimensioning involved in designing padstacks is done from the edges of the drilled, plated hole to features inside the PCB or the drill size. Traditionally, the PCB design process begins with the diameter of the finished plated through-hole. The choice of drill size has been left to the PCB fabricator, and the size of clearance holes and capture pads in signal layers is large enough for ample room for a range of drill sizes. As the pitch between device pins has shrunk over the years, this practice has resulted in PCBs with poor manufacturing yields.

To solve this problem, the designer of the PCB padstacks must take charge of specifying the drill size, as well as the finished hole size. To get from finished hole size to drill size, one need only to take the finished hole size and add 4 mils (0.102mm) to the finished hole size. Then, designing the padstack can proceed from the drill size. (Once these dimensions are chosen, the drill size must not be changed. If the drill size is made smaller than that specified, the aspect ratio may grow too large, and plating may not be completed all the way through the hole. If the drill size is too large, the clearances to copper in adjacent layers may be too small, or the drill may break out the side of the capture pad on a signal layer.)

FIGURE 2 is a top-down view of a plated through-hole or via showing the clearance hole or pad in a power plane of diameter F. This is the minimum opening in the power planes needed to guarantee enough room for the drilled hole,

the drill wander, and minimum insulation to the nearest copper in any layer, be it signal or power. **FIGURE 3** shows an array of vias or holes spaced on a 1mm pitch. The web between clearance pads is what is available for traces on signal layers and for copper in the plane layers to conduct the current used by ICs and other devices on the PCB. (Note: If the trace width is the same as the web in the plane, the impedance of the trace raises several ohms as it passes over the array of holes under a BGA. To minimize this effect, the web should be wider than the trace by about 2:1.)

Calculating Width of Plane Webs and Routing Channels in Signal Layers

Clearly, the width of a plane web is the hole pitch minus the diameter of the clearance pad or hole. The question is how to arrive at the diameter of the clearance hole needed to satisfy all the constraints. These constraints are a drilled hole large enough to ensure proper plating; room around the drilled hole to allow for drill wander; and minimum insulation thickness.

Minimum drilled hole size. Determining the minimum drill size needed to ensure proper copper plating requires knowledge of the maximum aspect ratio of the drilled hole. Aspect ratio is defined as the ratio of hole length to diameter. This is covered in detail in Ritchey, Chapter 4.[1] For now, the maximum aspect ratio for the top fabricators in the world is 12:1 for volume production. For the mid-tier fabricators it is 10:1, and for low-end fabricators it is 8:1. Of course, the minimum drill size is also influenced by the thickness of the PCB. For example, if the PCB is 120 mils thick and is built by a top-tier fabricator, the minimum drill size is 10 mils. For a mid-tier fabricator it is 12 mils, and for a low-end fabricator it is 14 mils. (As will be seen from the following analysis, with component lead pitches of 1mm or more, a 10-mil drill works well. For this reason, this is my default smallest drill size, even if the PCB thickness is less than 120 mils.)

Most high-performance PCBs designed today are 120 mils thick. This analysis will be for such a PCB built by a top-tier fabricator.

Allowance for hole wander. Drilled holes are often not exactly where they are designed to be for many reasons. Among them are the drill's ability to locate the exact spot where the hole is to be drilled; layer shrinkage of the PCB during lamination; dimensional errors in the film used to image the layers of the PCB; and misregistration of the layers during lamination. All these errors add up to a position error

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for the drill that is often referred to as TIR (total included radius) of TID (total included diameter). Top-tier fabricators can hold a TIR of 5 mils (TID of 10 mils) across an 18" x 24" panel – the most common panel size.

Therefore, we must allow 5 mils per side of the drilled hole for drill wander. This produces what is called a hole shadow the drilled hole casts all the way through the PCB. This shadow defines where we might find copper connected to a via or trace. We must keep away from this shadow in all layers by a distance defined by the insulation requirement for the PCB.

Minimum insulation requirement. Most laminate has a breakdown voltage on the order of 1000V per mil of thickness. Many systems require a minimum breakdown voltage or hipot test of at least 500V, and most Internet or telco products require 2000V. Being conservative, it is good to design for the more difficult requirement of 2000V. This requires a minimum of 2 mils of dielectric between opposing circuits or between traces or planes and plating in the hole. This requires the clearance hole diameter to be 4 mils larger in diameter than the hole shadow.

The problem with this small dimension is it does not account for the chemistry involved in etching, cleaning and plating wicking along the glass fibers in the weave of the laminate layers. **FIGURE 4** is a microsection of a plated through-hole showing wicking along the glass fibers. To lend some scale to the photo, the copper layers are 0.5 mils thick. Some of the wicking is as much as six times this, or 3 mils. This wicking is conductive. Therefore, it effectively increases the diameter of the plated through-hole by this amount per side, or 6 mils total.

Adding the 2 mils per side required for insulation and 3 mils per side for wicking, the total insulation thickness required to meet the insulation requirement is 5 mils per side.

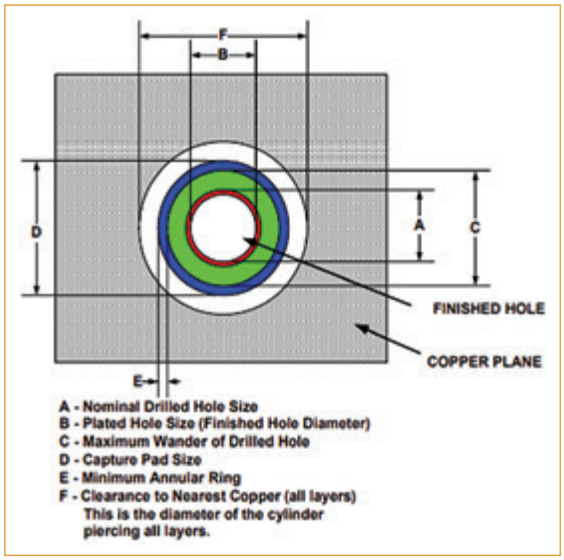

FIGURE 2. A top-down view of a plated through-hole.

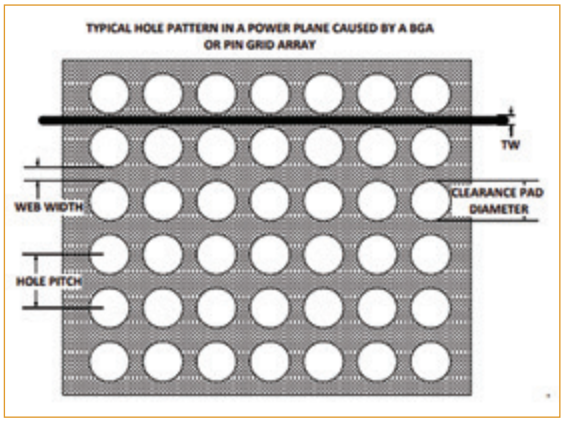

FIGURE 3. A view of a plane with a trace traveling over it.

Adding It All Up

Using the above information, it is possible to determine the plane web available for conducting current and space available for routing traces between pins of a 1mm pitch BGA. For the 120-mils-thick PCB, the minimum drill size is 10 mils. Referring to Figure 2, the diameter of the finished hole size is 4 mils less than this, or 8 mils nominal. The hole shadow is the 10-mil drill plus 10 mils for hole wander, or 20 mils. The clearance hole in a plane is 20 mils plus 10 mils for insulation allowance, or 30 mils.

The hole-to-hole distance of a 1mm pitch BGA is 39.37 mils. Subtracting 30 mils from this results in a web width or trace routing channel width of 9.37 mils. This is ample room for a 5 or 6 mil trace. If one attempted to route two traces between holes (assume they are 4 mil traces with a 4 mils space), the total width required would be 12 mils. Clearly, one of the requirements spelled out above would be violated, and the PCB would suffer from yield problems.

Preventing breakout of capture pads on signal layers. The connection between a trace and a plated through-hole is made by flashing a pad on the signal layer connected edge onto the plating in the hole. This can be seen in Figure 4 on the second layer from the top. The size of this pad has a direct relationship to overall reliability of the assembled PCB. If the contact between the trace and the plating in the hole is just the cross-section of the trace, a butt connection, this bond is not strong and is likely to be broken during soldering or rework, resulting in an intermittent PCB. The solution is to make the capture pads on signal layers larger than the hole shadow by enough to guarantee no butt connections occur, no matter where the drilled hole lands within the shadow. This allowance is called an annular ring. Depending on the reliability level of a product, the annular ring may be 1 mil, 2 mils or 0 mils. (IPC Class 3 is 2 mils.)

Products intended for the consumer market have lesser reliability requirements than those destined for computers, military or telco equipment. In the latter case, the minimum annular ring for a capture pad in a signal layer is 1 mil. This means these capture pads must be larger than the hole

shadow by 2 mils. In the above analysis, the hole shadow was calculated as 20 mils. This requires a capture pad of 22-mil diameter.

When the insulation requirement of 5 mils per side is added, the result is 32 mils. Subtracting this from the 39.37 mil pitch of the BGA, one arrives at a useful space for traces of only 7.37 mils. Clearly, there isn't even room for a single 6 mil trace, much less two!

Note: Often, when the capture pad is not large enough to prevent breakout, a fillet is added where the trace enters the capture pad to prevent a butt connection. This is often called "teardropping."

Nonfunctional pads. When early CAD systems created artwork for internal signal layers of a multilayer PCB, the same pad artwork used on outer layers was used for innerlayers. This resulted in pads on every internal signal layer, even when there was no signal connected to the hole on that layer. As experience was gained fabricating multilayer PCBs, it was discovered shorts often occurred between these nonfunctional pads and traces passing by. The solution was to remove these nonfunctional pads. Most fabricators do this as a standard practice. Newer CAD systems do not put nonfunctional pads in the artwork.

The notion removing nonfunctional pads creates room for more traces is not true. The size of the nonfunctional pads is the same diameter as the useful pads whose size was calculated to permit clearance for hole wander and insulation.

Conclusions

The features associated with a drilled hole in all layers are commonly called a padstack. In this example the pad stack is as follows:

- Drill size = 10 mils
- Finished hole size = 6 mils nominal
- Capture pad size = 22 mils
- Annular ring = 1 mil
- Clearance hole 30 mils
- Web with 1mm pitch = 9.37 mils
- Maximum trace width =5.37 mils

To preserve routing space throughout the signal layers, the minimum pitch of routing vias or component holes for surface mount parts is 1 mm. Any via or hole for connecting a lead of a surface mount part to an internal layer should use this pad stack and this hole pitch.

All other plated through-holes should have their pad stacks designed as follows:

- Drill size = finished hole size + 4 mils
- Capture pad size = drilled hole size + 10 mils + allowance for annular ring
- Clearance hole size = drilled hole size + 20 mils

Minimum hole pitch = (d1 + d2) +18 mils + minimum web requirement (usually no less than 7 mils), where d1 and d2 are the two different hole sizes.

Some observations. From the above it can be seen routing two traces between pins of a 1mm pitch BGA will result in a low-yield, unreliable PCB. Once it is agreed it is only possible to route one trace between pins, provided the trace width is 5 mils or less, it is possible to specify a minimum drill size of 10 mils. There is no good reason to specify a smaller drill size and the difficulties it entails, especially potentially unreliable plating.

If one is fortunate to have access to 50-mil pitch (1.27mm) BGAs, the space available for traces is 50 mils less 30 mils or 20 mils. This is plenty of room for two traces between

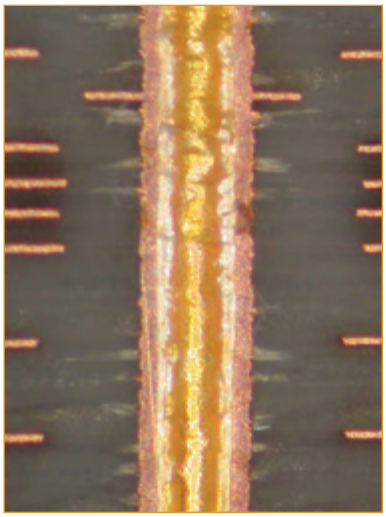

FIGURE 4. A microsection of a plated through-hole showing wicking along glass fibers.

pins and the space needed to separate them. When picking between a 1mm pitch component and a 50-mil pitch component, the choice is clear. IC manufacturers would do their customers a great service to stick with 50-mil pitch BGAs when the pin count is high. They do their customers a grave disservice when they specify 0.8mm pitch components. □

REFERENCES

1. Lee Ritchey, *Right the First Time: A Practical Handbook on PCB and System Design,* vol. 2, 2003, Appendices 6, 7 and 10.

LEE RITCHEY is considered one of the industry's premier authorities on high-speed PCB and system design. He is the founder and president of Speeding Edge (speedingedge.com), an engineering consulting and training company, and will speak at Virtual PCB West in September; leeritchey@earthlink.net.

Designer's Notebook, continued from pg. 18

meal. A service bureau may be willing to share its library for a nominal one-time fee. The task group chairman of the IPC naming convention standard is in the library business, and his company (PCB Libraries) is a place to start. Ultra Librarian is another that comes to mind.

You don't have to be a hero and do it all yourself, but since the PCB is no better than the underlying library, checking every part against the data sheet is strongly recommended. At Google, we weren't allowed to tape-out a board until every part to be used had been checked by a person not involved with the part creation. That extra pair of eyes helped prevent scrap.

A bad part can be costly. You lose money on scrap, but more important, you lose time, which you can only spend once, and it's gone. Library symbols built incorrectly enough times can cost the company customers. Bear that in mind from the moment you open the padstack editor to create the first brick of your building. It can come crashing down that quickly. Getting off the ground starts with the basics. A good foundation for your PCB starts in the library. □

Material Gains, continued from pg. 19

with high-performance materials, as board designers seek increasingly fast data signals and RF circuits operating up to mm-wave frequencies.

On the other hand, reliability is a challenge for everyone in the industry to address. Resistance to deterioration can be designed in through astute circuit design, ingress protection and establishing appropriate installation protocols that are also simple and straightforward for field teams to observe. None of these alone solves the entire problem. Applied in combination, however, it should be possible to create reliable, high-performing equipment for deployment in remote and challenging environments. □

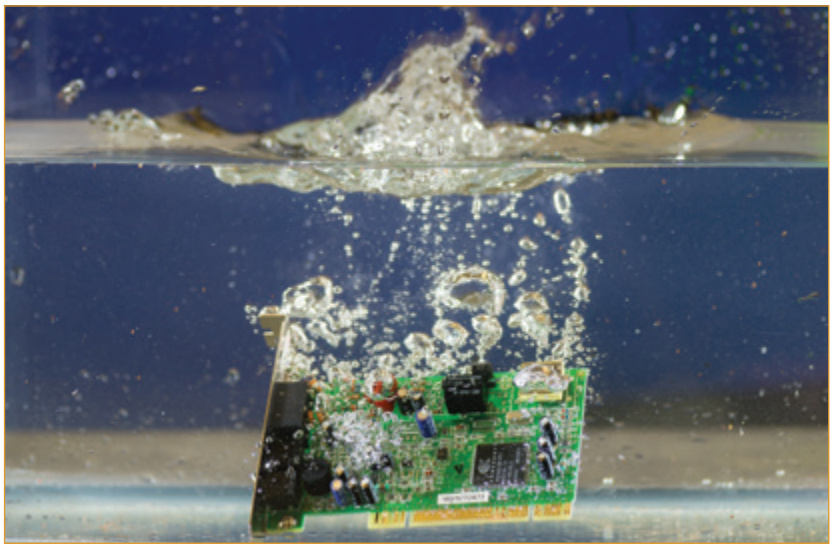

FIGURE 1. Properties of substrate materials can be liable to change with exposure to environmental factors such as moisture.

The PCEA's Grand Opening

THIS MONTH, I spoke with Rick Hartley about his presentation for the PCEA's grand opening webinar on Jul. 14. Next, PCEA Chairman Steph Chavez shares a timely message on how our time working from home is a serious matter, and how letting our guard down could be a mistake.

Again, PCEA chapters are in transition, and due to social distancing requirements, no face-to-face meetings have taken place to date, but a lot of virtual activity is happening. I also share our most updated list of professional development opportunities and events, which we hope you find useful.

PCEA Updates

In this interview with Rick Hartley, we discuss the PCEA's grand opening webinar on Jul. 14, where he presented a free class on PDN tips for successful power distribution. For access to the on-demand event, click here.

Kelly Dack: Today, I am speaking with renowned electronics industry educator and PCEA executive team member Rick Hartley. I'm so glad to talk to you. You have been kind enough to share your knowledge during the grand opening webinar. Tell us a bit about the event and why designers won't want to miss what you share.

Rick Hartley: The PDN is where everything starts. All the transmission lines and energy moving have to come from somewhere. They come from the power supply, but the high-frequency portion that gets loaded into the drivers and onto transmission lines so that driver "A" can drive load "B" and so on comes from the power distribution network (PDN). Generally, the PDN consists of either power planes or power routes with ground planes, decoupling capacitors, and sometimes other devices as the main ingredients.

I have done a longer version of this class at PCB West that was 3.5 hours and took the audience through everything I consider important for power delivery. For the PCEA grand opening, I share an hour of good tips on key features that need low inductance, how to maintain that, and other things regarding PDNs that they need to understand first and foremost. For example, one of the most important elements of good PDN design is maintaining a low inductance through the PDN at a broad range of frequencies at which the energy gets delivered. One of the myths engineers believe is the principal energy of the circuit is the clock frequency, but it isn't; it's driven by the rise and fall times of the IC outputs. They run at a much higher frequency than the clock.

Dack: Will you tell the audience some horror stories about how this misconception can play out in design? I love the horror stories you sometimes share because they illustrate what can go wrong when improper assumptions are made at critical points in the design process. What do designers miss about this topic?

Hartley: Designers need to care about inductance because high inductance at any of the frequencies of concern can cause major problems, and there is a broadband of frequencies that the PDN has to deliver. It starts at the clock and extends to a very high-frequency level based on the rise time. All that energy has to be delivered through the inductance of the power bus. If the inductance – or impedance – is high at any of those frequencies, you get large voltage drops that lead to switching noise, which leads to signal integrity and EMI problems, as well as others. It is important to understand how to design the PDN to ensure these things do not happen.

Dack: That sounds outstanding. This is you speaking about physics in action. It sounds like you provide the audience with visual representations of stackups and show how the conductors work to distribute power.

Hartley: Yes. With everything I present, I try to bring a simple but realistic view of the physics to people so they can understand why things happen, including a behind-the-scenes approach on how this stuff works and why people need to know it. I do not approach the subject matter like a professor in college who launches into high-level math.

Instead, I talk about subjects like the proper location of decoupling capacitors. For example, with a BGA part, do the caps belong under the BGA, or do they go on the same side of the board, next to the BGA? The answer to a question like this is "it depends."

It depends on the board stackup, the BGA, the power, and a number of factors. Designers must possess that knowledge when they deal with these elements so they won't do it incorrectly. Without considering these elements, they will end up creating some amount of power starvation, resulting in inductive losses and switching noise that will lead to other problems. It is very important to know these tips, and I have chosen the important ones to go through dur-

KELLY DACK, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). Read past columns or contact Dack; kelly.dack.pcea@gmail.com.

ing the one-hour class.

Dack: It's something for our design community and membership to look forward to. As you know, our PCEA membership is not limited to PCB engineers and designers. Tell us how PCEA membership is relevant to other electronics industry stakeholders from the manufacturing side.

Hartley: What is the PCEA going to do for manufacturing and test engineers and many of the other professionals involved in getting a PCBA to market? This whole spectrum of people needs to be involved with the PCEA because it will give them a better ability to share their knowledge with one another and make each other better at what they do. The PCEA exists to facilitate collaboration between all these disciplines.

You may remember the story of when I first got into board design. I thought that because I had just obtained my EE I was going to be the best board designer in the world. Nobody could tell me anything. The very first board I designed caused the board shop to show up at our company for an important meeting in the conference room with me and my boss. The DfM reps from the PCB supplier sat us down and said, "The other EEs at your company may think you are a great designer, but we think you are an idiot! (laughs) This thing you have designed is completely non-producible." And I admit that it was. While I put all my design efforts on electrical performance, I did not know how important manufacturability or DfM was to the overall process of getting a design to market. One of the things the PCEA needs to do is focus heavily on getting manufacturing engineers involved for that reason.

Dack: Amen! The PCEA is on its way to attracting all the cross-sections of the electronics industry. It's going to make the electronics world a better place. I look forward to hearing your presentation, and I appreciate you giving us a preview of what you are going to share. I'll see you at the webinar!

Hartley: Thank you. It has been my pleasure.

In addition to this webinar, there are so many ways to get involved! Join the PCEA by visiting our website (pce-a.org) and registering as a member to become part of the PCEA collective, which is more than 1,000 members strong. You can always reach out to me (kelly.dack.pcea@gmail.com) or PCEA chairman Stephen Chavez (stephen.chavez.pcea@gmail.com) for more information.

Message from the Chairman

by Stephen Chavez, MIT, CID+

Another month has gone by, and many of us continue to work remotely from our homes. It has been a challenge to get the foundation of the PCEA set in place. The executive board has done an amazing job juggling their day jobs, while putting in so much extra personal time to help the PCEA succeed. We are extremely excited about the release of our official website that took place on Jun. 1. All the hard work has paid off so far, with a lot of activity coming from our website, including new members joining, webinar collaborations with SMTA, and our grand opening webinar. Stay tuned for more activities coming your way now that the PCEA is up and running!

Now, the "new normal" has become our new way of life. I, like many, have been working remotely for about three months, if not more. I don't see an end to this remote isolation in the near future as the world battles Covid-19. With the constant barrage of meetings through WebEx, Zoom, GoToMeeting and other platforms – as well as virtual seminars – it seems to be getting a bit tiresome and overloaded when you add in isolation, constant sanitation and wearing face masks in public.

As we have adapted, we continue to push on successfully. Work has not stopped for many of us, and in many cases, we are busier than ever. The industry had already made the jump many years ago to the ability to work remotely. For the most part, the toughest challenges today are usually network connections and remote access onto VPNs, Mobil Pass, or Duo Mobile. Security is paramount, but, at times, it comes with its own set of issues. However, we continue to do what we do best; we do what it takes to get the job done!

Again, this new way of living is taking its toll on us. We eagerly look forward to the day we can get back to those days of old before this virus hit the world. Businesses have started to slowly reopen, even though the world is seeing spikes of the virus in certain locations. It's scary! Many people have let their guard down, though, and have relaxed social distancing requirements, as well as not wearing facial masks in public. I've heard and read that some people have even felt this virus is not real and is more of a political conspiracy attack. Everyone has their right to their own beliefs – this is America – but I can tell you from a very personal and recent experience this virus is real; it's no joke.

It's amazing how one's perspective changes when the virus hits close to home, and someone close to you dies from Covid-19. This happened to me on Jun. 7. My extremely close and dear friend Alvin was as healthy as anyone I knew. I grew up with him over these past 43 years, and he was like a brother to me. He lost his battle with Covid-19. From the time he contracted this virus to the time he passed was fewer than 30 days.

As we continue to work remotely in isolation, my personal belief is it's necessary for all our safety. We need to continue doing our part, maintain social distancing, sanitize, and wear face masks when we are in public until the world gets a handle on this virus, and a vaccine is developed. I continue to wish everyone and their families health and safety.

Professional Development and Events

It has been our custom to highlight all up-and-coming industry events to look out for in 2020. We will continue to do this; however, with the challenges brought on our industry by the Covid-19 outbreak, we can only remain hopeful that

these events will not be affected. If you are interested in any of these events, please search and contact the event coordinators directly for the latest event status.

- Aug. 11–13, 2020: CadenceLIVE Americas 2020 – Virtual
- Sept. 7–10, 2020: PCB West Virtual 2020
- Sept. 16–17, 2020: Del Mar Electronics & Manufacturing Show (San Diego, California)
- Sept. 28 –Oct. 23, 2020: SMTA International – Virtual
- Oct. 7-9, 2020: AltiumLive (San Diego, California) – Virtual
- Jan. 23-28, 2021: IPC Apex Expo (San Diego, California)
- Jan. 26-28, 2021: DesignCon (Santa Clara, California)
- May 11-13, 2021: IPC High-Reliability Forum 2021 (Baltimore, Maryland)
- Nov. 10, 2021: PCB Carolina (Raleigh, North Carolina)

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Conclusion

We have many choices with which to occupy our time during the Covid-19 era. From wherever you work – whether at home or in an office – it's a good time to gain knowledge and take it seriously. Use that knowledge to become part of the solution.

EMBEDDING MAGNETICS in a PCB Design

Leveraging common fabrication processes to encapsulate transformers. by JIM QUILICI

Like embedded resistors and capacitors, embedded magnetics provide a means for reducing system size and cost. Transformers and inductors used in power and telecommunication applications are often the more expensive devices in a system design. When realizing a power converter or RF module, cost and size reductions can be realized by combining the magnetics and PCB functions. This article provides an overview of embedded magnetics design and construction.

Inductors and transformers are basic building blocks of power and communication systems. A simple transformer or inductor can be implemented between two PCB layers. **FIGURE 1** shows a cross-section of an embedded magnetic transformer. A cavity is milled into an FR-4 substrate. Ferrite cores are inserted and encapsulated in place with low-shrink epoxy. For those unfamiliar with ferrite material, it is a ceramic made by mixing iron oxide and metallic elements like manganese, nickel and zinc. The mixture is molded and fired to create a magnetic core. The materials are classified as ferromagnetic, meaning when a conductor is wrapped around the material and a current is applied, a magnetic flux will develop within the core and remain there as long as the current is applied. Permeability is a measure of the materials' ability to build a magnetic flux. High permeability materials (5000 to 20,000) use a mixture of manganese and zinc (MnZn) and are generally used to produce RF inductors and transformers. Power applications also use MnZn, yet at a mixture that produces a much lower permeability, in the range of 1000 to 3000. RF and power applications also use inductors and transformers to filter noise. Nickel-zinc (NiZn) ferrites have lower permeability (800 to 2000), yet operate over a wider frequency band and are commonly used to filter noise. A system implementation may use a combination of ferrite cores. For instance, a power converter may use MnZn ferrites to temporarily store energy in a transformer or inductor, while also using inductors wound on NiZn cores to filter noise.

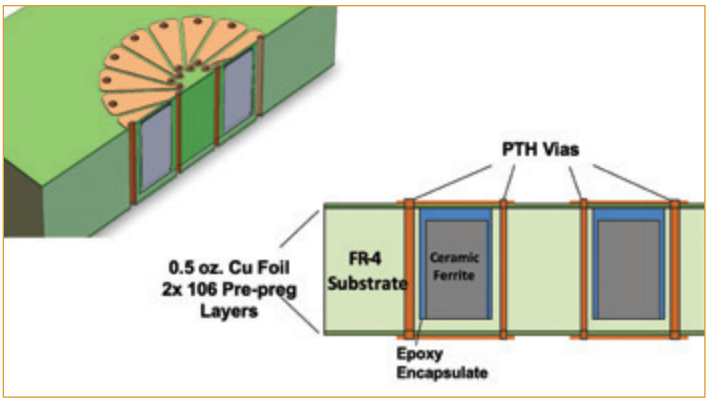

FIGURE 1. Cross-section and layer stack.

Fabrication methods. Fabrication begins with routing "donut holes" into an FR-4 substrate. Once the cavities are milled, cores are inserted either manually or automatically. Given a ring-shaped core, it is practical to simply pour them on the routed panel and use a vibratory shaker table to distribute the cores into the cavities. Low shrink epoxy is then screen-printed on the top surface to protect the core. After the epoxy is applied, the panel should be placed in a vacuum chamber for a few minutes to draw out any air trapped underneath the core, prior to epoxy cure. **FIGURES 2** and **3** show examples of the routed panels and encapsulated cavities. After encapsulation, the top surface of the panel should be planarized (sanded) and cleaned prior to lamination. One may consider removing the epoxy encapsulation step and simply filling the gaps around the ferrites with prepreg epoxy during lamination. This presents two problems. One, much of the prepreg epoxy around the cavity can flow into the small gaps, reducing the amount of epoxy at the rim of the cavity and diminishing lamination integrity. Second, during lamination the panel will see pressures as high as 150psi, and the prepreg epoxy that fills the gaps will cure under high pres-

sure. Residual pressure will remain on the ferrite after the panel is removed from the lamination press. Ferrite materials are sensitive to pressure, and their permeability will be impaired. By first encapsulating the cores with low shrink epoxy, they will be "cushioned" during lamination. When the panel is removed from the press, no residual pressure will remain from the lamination process.

Once the cores are encapsulated in place, fabrication follows normal PCB processes. FR-4 prepreg and copper foil layers are laminated to the top and bottom surfaces. Via holes are drilled and plated to interconnect the top and bottom surfaces. Conductive winding patterns are then imaged and etched on the top and bottom surfaces. **FIGURE 4** shows examples of winding artwork for an inductor, transformer and common mode filter (choke). The two colors indicate separate layers. These devices can be combined, arrayed and stacked to realize complex circuit functions. For example, **FIGURE 5** shows an ethernet media filter, realized with embedded magnetics. This device has two stacked subpanels, each containing two transformers and two common mode filters, for a total of eight transformer elements. By stacking, the parts fit in the same footprint as conventional wire-wound transformer modules.

Conclusion

Magnetics are some of the last electronics components still fabricated by hand. Embedded magnetics provide a means to fabricate these devices with automated and batch processes. The process is portable and can leverage the existing capital equipment investments of most printed circuit board manufacturers. Since the winding elements are defined by photolithography and chemical etching, the resulting product is highly consistent and has the reliability consistent with PCB technology. Essentially, the embedded magnetic device is a PCB that permits other passive and active devices to be placed for higher integration. Finally, if a design already uses a PCB, embedding the magnetics can help reduce system cost by combining the cost of the PCB and magnetic components. □

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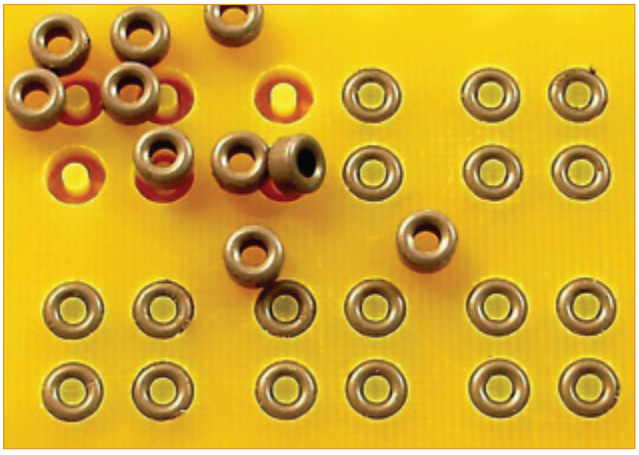

FIGURE 2. Routed cavity and ferrite cores.

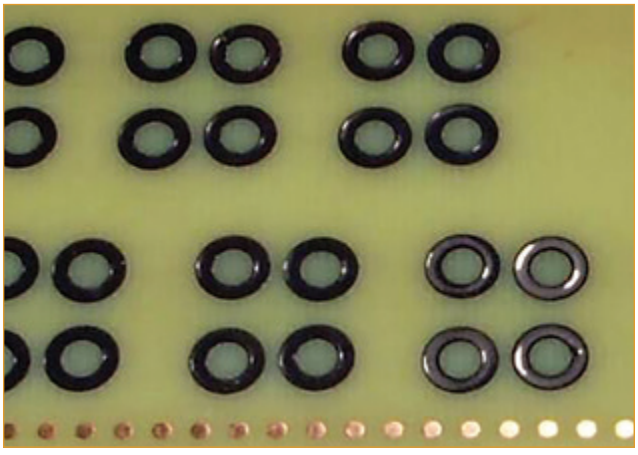

FIGURE 3. Encapsulated panel.

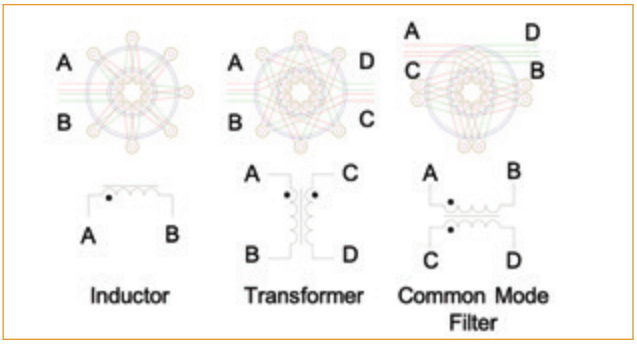

FIGURE 4. Example artwork for common magnetic devices.

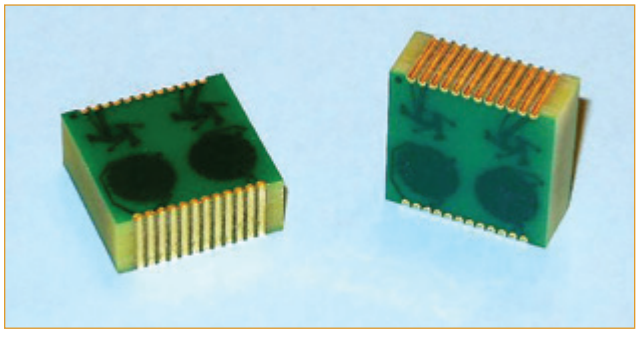

FIGURE 5. Ethernet media filters.

Hidden Trouble in a BGA PACKAGE

Does a small node suggest anomalies – and potential failure?

by TOM ADAMS

A small raised area was initially noted on the top surface of the plastic ball grid array (BGA) package discussed here. To learn whether there were other structural anomalies deeper within the package, it was imaged by both x-ray and ultrasound. The x-ray imaging was performed first, using a Nordson-Dage Quadra 7. When traveling through a sample, the x-ray beam is locally attenuated by the density and thickness of the material through which it passes. Very dense materials such as metals may limit the thickness of the sample that can be imaged, while materials such as plastic are far less attenuating. The completed x-ray image reveals in very high-resolution local changes of attenuation over the area being imaged.

FIGURE 1 shows one corner of the BGA's die and the attached wires. All the wires are intact here and on the rest of the BGA. All features are encased in the nearly transparent (to x-ray) mold compound. The black circular features are the solder balls under the BGA. The indistinct gray feature just above the edge of the die is caused by the variable thickness of underfill material extruded from beneath the die. Within the area of this image there could be delaminations or voids – i.e., air-filled gaps – on top of the die or in the die attach material below the die, but air attenuates an x-ray beam so slightly, and the gaps are typically so thin, that these gaps would not be imaged.

The acoustic micro imaging tool, a Nordson-Sonoscan C-SAM, was then used to image the BGA. **FIGURE 2** shows the topography of the BGA package but no internal features. In this viewing mode, the transducer emits a pulse of ultrasound and accepts for imaging only the first echo from each of the thousands of x-y locations. This mode is frequently used on components such as BGAs where surface irregularities can indicate internal structural irregularities that may cause electrical failures. Ultrasound was pulsed at the surface of the BGA package in single tiny pulses, emitted by the moving transducer that is coupled to the surface of the package by an accompanying water column. The speed is high: The moving transducer can launch and receive echoes from tens of thousands of launched pulses per second. At each x-y location, the pulse is launched and its echo received before the transducer images the next location. A completed acoustic image may contain thousands or even millions of pixels, each the product of an echo from one pulse.

To make a topographic map of the surface of the BGA package, the acoustic micro imager software first recorded the arrival time for the first echo to arrive at the transducer from each x-y location. The surface of the BGA package is not flat. The earliest arriving echoes were imaged with white pixels. In Figure 2, such echoes are found only at the highest portion of the surface bump near

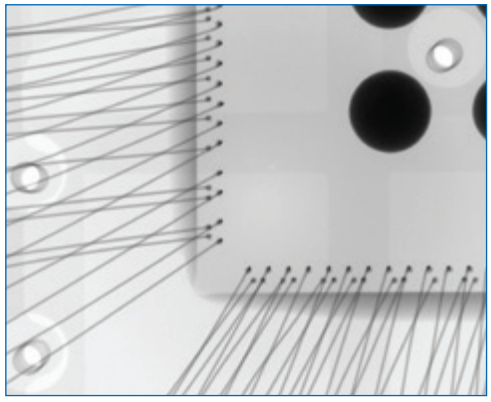

FIGURE 1. X-ray image of one corner of the BGA package reveals no broken wires.

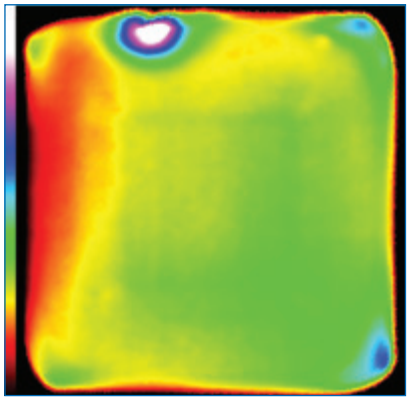

FIGURE 2. Acoustic topographic map of the BGA package surface. White points are highest; red-black points are lowest.

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the top left of the image. Echoes arriving next were colored magenta and surround the white area. The next arrivals were made dark blue, and so on.

The color map used to make this image is at left. White – the color of the first arrivals – is at the top of the color map. Next is magenta, then dark blue, then green, and so forth. The lowest portions of the package's surface are red-to-black pixels at the edges. The difference in altitude between the highest and lowest points on the surface is approximately 0.25mm.

FIGURE 3 used an interior imaging technique that is probably the most commonly used acoustic mode. A gate is first decided on, a defined vertical depth within the part. Only echoes reflected by material interfaces within this gate are accepted for imaging. Echoes are ignored if they were re-flected by material interfaces above or below the gate. Vertically, the gate can be as wide (vertically) or narrow as desired, even down a tiny fraction of a micron. Here, the gate's width is approximately 0.732mm, extending from near the surface to the tops of the wires.

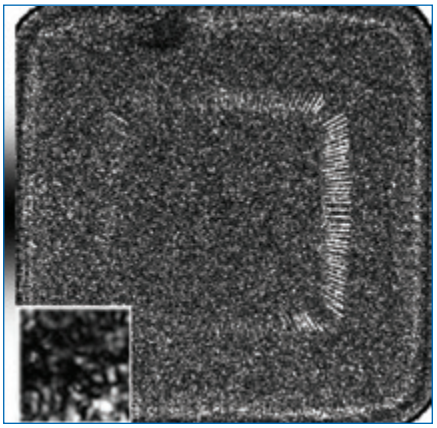

FIGURE 3. Gating echoes on a thin slice just above the die shows the die is tilted.

Two items are of interest. The first is a darker spot near the top edge of the image, just left of center. At first glance it might appear the mold compound is much denser here, but that is very unlikely. But the dark spot is also positioned directly below the excess mold compound on the surface.

What is happening is this: Ultrasound is pulsed into the BGA and reflected by material interfaces, including interfaces between the filler particles and the mold compound. The ultrasound is also somewhat attenuated simply by traveling through the mold compound. Ultrasound striking this dark area had to travel through the bump on the surface of the package twice, going to the gate and returning as an echo to the transducer. Because it traveled through more mold compound than in surrounding areas, it is more attenuated than surrounding areas, and the area of the bump appears darker than the areas around it.

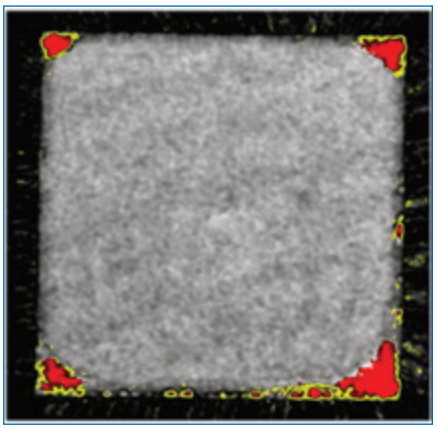

FIGURE 4. Red mark delaminations of the mold compound from the die at all four corners.

The dark area closely resembles the shadow that would be cast by an air-filled void of this size higher in the package. Even if an air gap is extremely thin, the air-to-solid interface at its top reflects virtually all an arriving pulse back to the transducer. None of the ultrasound crosses the interface, so an image of a lower interface will show the dense black sharply outlined shape of the gap.

The inset at lower left shows the southeast portion of the dark area magnified. Two details prove it is not the shadow of a void: First, it contains white reflections from filler particles within this gate; second, the border of the dark region is not sharp.

The second item – the fine white lines in the image – could be more serious. The lines are the loops of wires running from the die to nearby lead fingers. The interface between the mold compound and the metal creates a high amplitude echo imaged in white. White is at the bottom of the color bar at left.

The tops of the wire loops appear along the right side of the die and along the righthand portions of the top and bottom. To the left of these areas, they are missing because the tops of the loops are below the bottom of this gate. The defect is not with the wires but with the die they are attached to, which is tilted downward to the left. Such tilting puts mechanical stress on many of the wires and makes eventual wire breakage and field failure more likely.

The die face itself is shown in **FIGURE 4**. The die is tilted, but the gate used here was wide enough vertically to accommodate the entire depth range used by the surface of the die. Some of the wires are faintly visible around the edges of the die.

The problems here are obvious: the red areas at each of the corners. These are disbonds between the mold compound and the die, which reflect nearly 100% of the arriving ultrasound as a powerful echo. The two materials on either side of the gap have different coefficients of thermal expansion, with the result that the heating and cooling of normal operations will encourage the cracks to grow and break wire bonds. The x-ray image of one corner of the die in Figure 1 showed no broken wire bonds. Air gaps were present when the x-ray image in Figure 1 was made, but the attenuation of the x-ray beam by an air gap that may be only a few microns thick is negligible, and there was no trace of an air gap in Figure 1. Because no wires are broken, this BGA might pass an electrical test at this point.

The bottom portion of **FIGURE 5** includes much of Figure 4, but with a white horizontal line near the bottom of the image. The line marks the path along which the transducer repeatedly scanned back and forth. On the first scan, it accepted echoes only from a very narrow gate at the base of

the die. It moved very slightly upward to scan back, collecting any echoes from that narrow gate. When it reached the surface of the part, the scans were in effect stacked on top of each other to give a nondestructive cross-sectional view of the package along the white line. The blue arrow connects the two views. (The two red delaminations seen in Figure 4 at this location have been removed to show this sectioned view.)

There are no surprises in the cross-sectional quantitative B-scan analysis mode (Q-BAM) view: The delaminations are present, and no anomalies are not seen in the planar view. The yellow flecks present higher up in the Q-BAM image are filler particles added to plastic to create the mold compound mixture.

To sum up: This BGA package has an uneven top surface, which might cause a handling problem during assembly. X-ray shows no broken wires, although the tilted die could cause wires to break in the future. Most seriously, at each of the four corners of the die are delaminations capable of expanding over time and shearing off wires. ▫

TOM ADAMS is a consultant with Nordson Sonoscan (nordsonsonoscan.com); info@nordsonsonoscan.com.

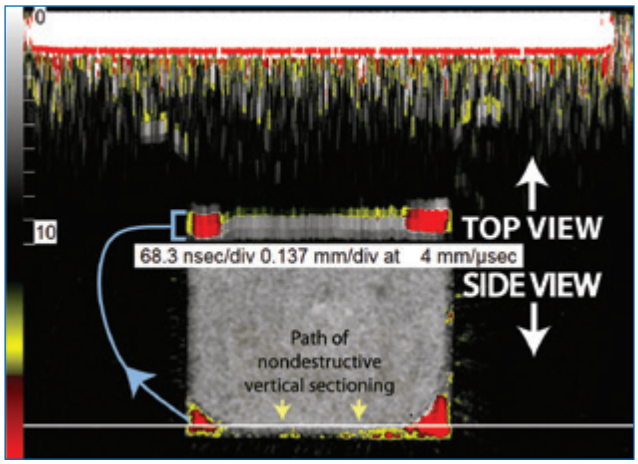

FIGURE 5. Bottom half: location of path for cross-sectional scanning. Top half: resulting cross-sectional view.

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Leveraging SYSTEMS AND PROCESSES to Evolve NPI

A cross-functional team approach for completing prototypes and ramping to production. by JOHN SAMMUT

Faster, better, cheaper has always been a mantra in electronics manufacturing services (EMS) because leveraging the benefits of companies selling manufacturing expertise and infrastructure has been the primary motivation behind the growth of outsourcing. Improvements in computing technology, networking infrastructure and systems interconnection now give EMS teams unprecedented real-time visibility into the product realization process. But like the guy who buys a Porsche and drives mainly on city streets, these systems are rarely tested to their full potential. Firstronic's new product introduction (NPI) team recently needed to break that paradigm when the Covid-19 pandemic drove a new customer to request a product ramp at high speed when other supply chain options were unexpectedly shut down.

A medical device manufacturer with an infrared thermometer had production shut down in its Tijuana-based EMS supplier as a result of Baja California-mandated Covid-19 restrictions. They needed to dual source as quickly as possible since this was a critically needed product.

Firstronic had extra capacity available and was chosen as the alternate supplier. This article looks at ways its cross-functional team (CFT) model and real-time systems were used to complete an 800-piece validation order in fewer than 10 days and begin full production in less than two weeks.

A CFT was assigned to the account. In this CFT model, the team includes a tactically focused program manager, a strategically focused account director, a buyer, a product engineer, a process engineer, a test engineer, a quality engineer, a production supervisor or leadperson and a customer service representative focused on materials and scheduling. CFTs are this EMS provider's frontline resource to ensure what is delivered to customers meets their requirements. They provide the rest of the organization clear focus on what resources are needed to support the customer. The broad-based nature of this team structure ensures each customer has a complete set of subject matter experts focused on project execution and continuous improvement. The teams measure a number of metrics, including process and specific product yield relative to key performance indicators (KPIs), customer and product line gross margin, forecast accuracy, revenue to project budget, on-time delivery performance, customer satisfaction, corrective actions and inventory turns. If issues arise in the metrics, the team analyzes the root cause and recommends appropriate corrective action.

Materials were the critical path. The EMS provider had an existing relationship with the printed circuit board (PCB) fabricator, and the customer redirected existing orders for the PCB to ensure an immediate bare board supply was available. The printed circuit board assembly (PCBA) had four components including an IC, making the rest of the materials strategy easy to manage.

The other key element was ensuring validation requirements were met. This EMS provider's standard NPI program is rigorous. The PCBA went through a complete purchased part approval process (PPAP), process failure mode effects and analysis (PFMEA), advanced product quality planning (APQP) techniques, development of a control plan and run-at-rate validation process. The CFT presented the initial ramp timeline to the OEM via a teleconference on May 12 and shipped 800 units for validation on May 22 utilizing this process.

The OEM shared reflow profiles, and the EMS provider used the same solder paste, helping process validation. This speeded up the approval process.

The EMS provider's Plex Online ERP system was a critical tool in achieving a fast ramp. Plex allows searching for process and product risk. As part of every new customer transition, CFTs look at the top ten product risks for that customer to eliminate potential issues before they become issues.

From an operational standpoint, the ERP's capabilities integrate well with Firstronic's Lean manufacturing philosophy. Product is barcoded and integrated with the ERP to create a permission-based system that can stop production at any point, freezing material and production until the identified issue is resolved by the CFT analyzing machine, man and methods to determine the best corrective action. Centralized

verification documentation and real-time data within the ERP provide management with significant visibility into project status, quality trends and operational efficiency.

Some challenges required fast resolution. The PCBA was too small to carry a serialization number on each unit within its panel, so the entire product is controlled at the top-level assembly under ISO 13485 in the OEM's system. Originally, the PCBA was supplied by an EMS provider adjacent to a molder that performed final assembly after the housing was molded. Since PCBAs were now shipped from Michigan, a more robust packaging solution was needed. The CFT devised a packaging solution to support this. The validation process also found the routing operation to separate assemblies from panels was leaving rough edges, and a process modification was made to correct the issue. Approval for volume production was received on June 4, and products are shipping now.

While fast ramps are the exception, not the rule, at this EMS provider, the Covid-19 pandemic continues to drive the need for this type of option. While as of this writing all states in the US are open and nonessential industries are beginning to restart production, restrictions are still being enacted in impacted regions around the world. EMS providers with the systems and internal processes to achieve fast ramps without sacrificing required validation procedures or impacting product quality are one solution to these challenges. ▫

JOHN SAMMUT is president and CEO of Firstronic (firstronic.com); jsammut@firstronic.com.

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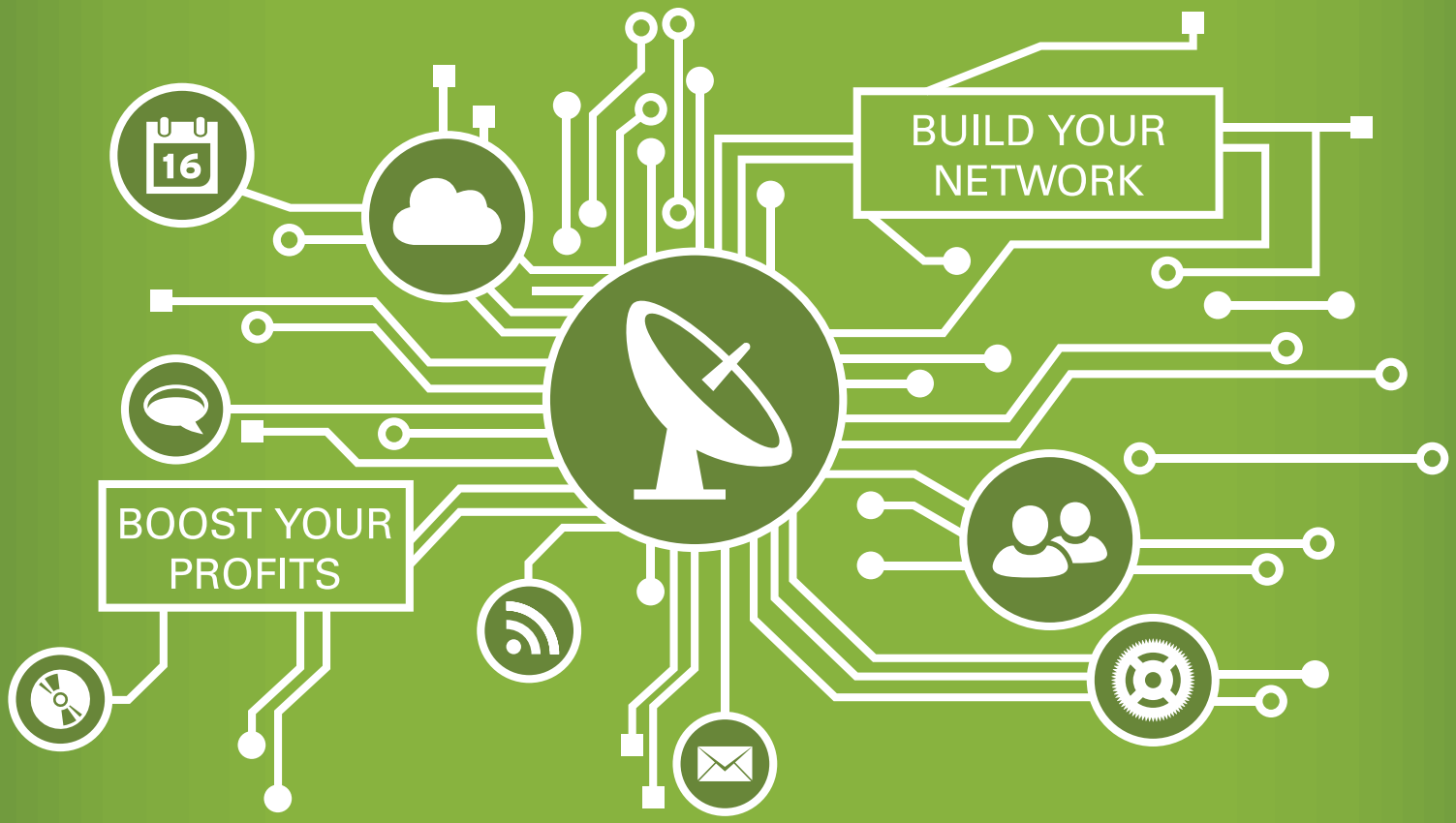

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FPGA ISSUES and Concerns: A Real Danger and a Call to Action

The reality of a brittle supply chain could mean harsh consequences for failure to deliver. **by MARTIN HART**

A field programmable gate array (FPGA) is an integrated circuit configurable by customers in the field, making such devices desirable for space and defense applications. A fortified version, known as a Radiation Hardened (RadHard) FPGA, can withstand attacks from electromagnetic and particle radiation in outer space.

Columns, rather than solder balls, are a critical subcomponent in the final assembly of FPGA packages.

A sudden shortage of mission-critical FPGA devices could result in warfighters not flying and rockets not launching. This is not an exaggeration. But how could this be? Quite simply, makers of ruggedized FPGA devices depend on a single subcontractor to provide services to attach copper-wrapped solder columns.

Past production shortages in the semiconductor industry have been short-lived because multiple vendors have been able to quickly step in to fill voids in the supply chain. Today, only a single subcontractor is designated on the Qualified Manufacturer List (QML-38535) as a provider of copper-wrapped solder column attachment services for the entire FPGA industry. Any supply chain dependent on a single supplier is inherently vulnerable. Action is needed to develop a solution to resolve this vulnerability.

Business continuation can become an issue for any number of reasons, ranging from natural disasters to the loss of a key manager due to death or retirement. An existential threat could materialize if a hostile foreign actor acquires or otherwise takes control over a single-source supplier, particularly if production is offshore. In terms of repercussions, a facility relocation typically results in the loss of QML status, pending requalification. It can take up to 24 months for a new candidate to undergo the arduous approval process prior to attaining QML status to provide column attachment services. A prolonged production shutdown of FPGA devices directly impacts US national security, affecting thousands of downstream customers who would be unable to complete systems and black box builds. Proactive steps taken now to identify and monitor the risks can mitigate such a threat.

The US Department of Defense (DoD) provides guidelines to help industry identify and mitigate dependency on services from single-source subcontractors. The Defense Standardization Program Office publishes a helpful document, SD-22, titled, "Diminishing Manufacturing Sources and Material Shortages (DMSMS), a Guidebook of Best Practices for Implementing a Robust DMSMS Management Program." It is a useful resource to aid FPGA device makers seeking to broaden their supplier base for components critical to the welfare of national security. The DMSMS guidebook presents the concerns and recommended remedies to mitigate the risk of loss, or impending loss, of manufacturers or suppliers of items, software, and raw materials.

The Under Secretary of Defense for Acquisition and Sustainment delivers an annual report to Congress titled "Industrial Capabilities" stating the mission of the Office of Industrial Policy (INDPOL), to ensure a robust, secure, resilient, and innovative industrial capabilities upon which the DoD can rely.

Eight companies making the majority of the world's FPGA devices may consider issuing forward-looking cautionary statements to stakeholders, citing their reliance on a single QML vendor to attach copper-wrapped columns. These statements disclose potential risks from the perspective of management's reasoning or beliefs.

Fabrication of copper-wrapped solder columns is not trivial and requires the correct know-how, manufacturing equipment and proficient operator skills to properly attach columns to FPGA packages. Solder column attachment services are not available from your friendly catalog distributor.

Risk of an FPGA production shutdown is preventable by taking prudent action now. The most direct solution is to qualify multiple vendors for critical processes, including column attachment services. This remedy requires a relatively low investment by FPGA device makers.

Supply Chain Resiliency

A production stoppage of critical FPGA devices could result in the failure of the defense industry to fulfill commitments for delivery of warfighters. Furthermore, failure to deliver RadHard FPGA packages could disrupt mission schedules.

Several risk archetypes for achieving a robust and resilient production of FPGA devices include a diminishing domestic manufacturing base and a fragile market. FPGA packages with solder columns are produced in a low-volume manufacturing environment; as such, around 75,000 individual FPGA devices spread over 100 different outline packages are produced annually.

Total annual volumes of FPGA and ASIC devices, with as much as 70 million copper-wrapped solder columns, are minuscule compared to volumes of commercial off-the-shelf (COTS) FPGA devices consuming billions of solder balls. Attaching solder columns to FPGA packages is substantially different from attaching solder balls that dominate the COTS market.

Solder columns are cylindrically shaped pins that must be held vertically in place by precision fixtures without slanting or falling over during the attachment and reflow process. A final assembly step requires the entire matrix array of up to 1,752 columns be planarized without damaging a single column. No manufacturing defects are allowed. Talented operator skills must be employed during every step in the process of attaching columns to FPGA packages. Attaching copper-wrapped solder columns to FPGA packages is fundamentally a nonautomated, artisan process.

Royalty-free, US-manufactured copper-wrapped solder columns are readily available today in the supply chain. But starting from scratch, it could take 24 months for multiple subcontractors to undergo the arduous process of attaining QML status to provide column attachment services.

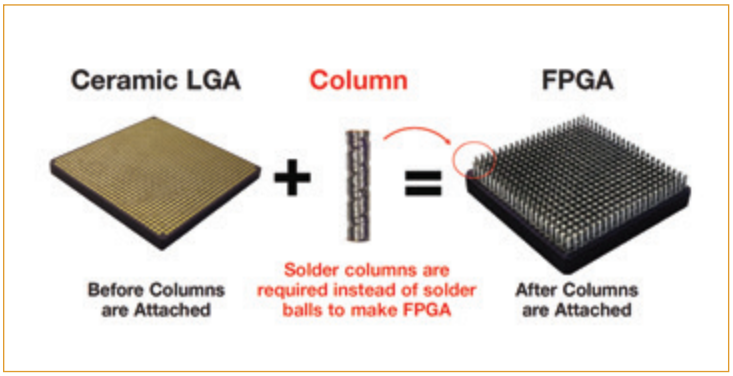

FIGURE 1. Sequence of FPGA package assembly with solder columns.

Monetary considerations. Companies that produce FPGA devices are not required to voluntarily qualify multiple subcontractors to attach copper-wrapped solder columns to their products. A lack of funding by FPGA manufacturing is most often cited as the primary reason for not qualifying a second source. Multiple microelectronic subcontractors in the US supply chain are ready, willing and able to provide column attachment services, provided funding is available to pay for the cost of QML qualification. An accelerated initiative by FPGA makers to mitigate risk and qualify multiple subcontractors to attach copper-wrapped solder columns requires a sizable investment. FPGA makers must take the lead in initiating the qualification of alternative subcontractors. As a practical matter, subcontractors cannot independently apply for QML status without the support of the FPGA maker.

The DoD speaks. The Department of Defense published an unclassified report titled, "Assessing and Strengthening the Manufacturing and Defense Industrial Base and Supply Chain Resiliency of the United States," in fulfillment of Executive Order (EO) 13806, which describes risks that threaten America's manufacturing and defense industrial base.

The 10 "risk archetypes" described in the report are as follows: 1) sole source; 2) single source; 3) fragile supplier; 4) fragile market; 5) capacity constrained supply market; 6) foreign dependency; 7) diminishing manufacturing sources and material shortages (DMSMS); 8) gap in the US-based human capital; 9) erosion of US-based infrastructure; and 10) product security.

Most of the risk archetypes described in the report apply to FPGA manufacturing. Risk archetypes lead to a variety of impacts upon America's industrial base. These include reduced investment in new capital and R&D; reductions in the rates of modernization and technological innovation; potential bottlenecks across the many tiers of the supply chain; and lower quality and higher prices resulting from reduced competition.

Sole source vs. single source. A sole source risk exists when only one supplier can provide the required capability. Fortunately, manufacturing capability for producing copper-wrapped solder columns exists today in the US. Also, multiple subcontractors capable of providing column attachment services for FPGA packages currently exist in America.

A single source exists when only one supplier is qualified to provide a required capability. EO 13806 draws a key distinction between sole source and single source. Multiple suppliers may exist, but only a single source for copper-wrapped solder columns is qualified, according to the Qualified Manufacturing List (QML-38535) published by the Defense Logistics Agency (DLA). Companies that produce FPGA devices are not required to voluntarily qualify multiple subcontractors. It could take 24 months for an alternative candidate starting from scratch to attain QML status should a single source supplier unexpectedly shut down.

Other risks. A fragile supplier is an individual firm that is financially challenged or distressed, and this potentially includes most subcontractors in the US microelectronics industry today. A fragile market occurs when domestic markets have structurally challenging economics and face the potential to move toward foreign dependency.

Presently, a capacity-constrained supply market may not be thought of as problematic. However, a single-source supplier may not be able to keep up with a sudden surge in market demand. Foreign dependency on wafer foundries could become an elevated risk, especially when a domestic foundry does not produce a critical item.

Diminishing manufacturing sources and material shortages risk are often associated with obsolescence that might result

when a relevant supplier issues end-of-life warnings.

Gaps in US-based human capital are an ongoing concern. Think the "graying" of Silicon Valley. The industry needs to keep fresh science, technology engineering and math (STEM) talent in the pipeline, especially within the microelectronics assembly base. Attaching copper-wrapped solder columns to FPGA packages is fundamentally a nonautomated, artisan process, requiring highly developed operator skills. Erosion of US-based infrastructure, including the loss of specialized capital equipment, is a risk, since attachment of solder columns to FPGA packages requires precision tools and fixtures that are difficult to fabricate. Last, product security could be of heightened concern under circumstances where FPGA packages require an assembly step overseas, opening the risk of reverse engineering or embedding trojans by hostile foreign actors.

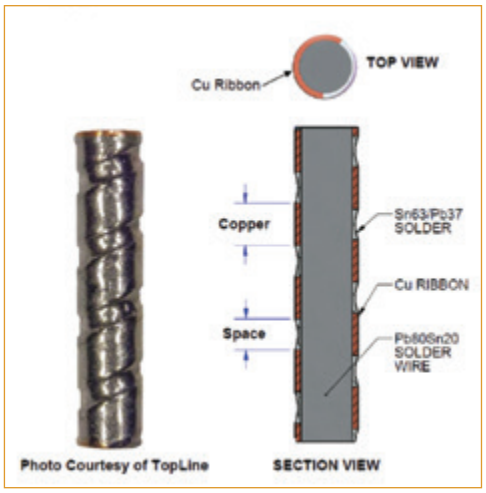

FIGURE 2. Cutaway of copper-wrapped solder column.

FIGURE 3. Braided solder column developed and patented by Topline.

Supply base recovery? FPGA devices used in defense and aerospace applications must be produced by suppliers on the QML. Multiple contractors are at various stages of tooling up, awaiting DLA certification to provide copper-wrapped column attachment services on FPGA and ASIC packages. Six-Sigma, based in Milpitas, CA, is already QML-38535-approved for attaching copper-wrapped columns. VPT Components and Micross Components have also demonstrated the capability to perform these services, and other suppliers, including Golden Altos, plan to offer them. By the end of 2021, it is probable five contractors will be qualified to attach columns to FPGA packages, pending certification.

Most recently, the Covid-19 pandemic has introduced risks not previously considered that can potentially derail America's dominance in warfighter technology. An early casualty of Covid-19 was an advisory to halt travel to conduct QML-38535 audits by DLA employees. DLA audits scheduled in March 2020 were abruptly cancelled. This unexpected event blocks new suppliers from participating in the QML market. The stoppage of DLA field audits means an indeterminate delay in qualifying additional qualified suppliers to make QML FPGA devices. Would DLA consider conducting virtual QML audits using video platforms, such as Zoom or Microsoft TEAMS, to support the supply chain?

The copper-wrapped column attachment service business is currently dominated by a single-source monopoly. Historically, monopolies, left unchecked, tend to drive up costs, extend delivery times, and generally dampen customer satisfaction. The introduction of fresh competition to perform column attachment services is expected to establish competitive pricing and speed deliveries. Multiple vendors offering copper-wrapped column attachment services increases the likelihood that a strong, resilient manufacturing and defense industrial base and supply chain in the United States will result. Original device makers (ODM) have noted FPGA and ASIC packages are suspended in financial limbo for more than a year, while products remain in a state of work-in-process (WiP) before generating cash flow.

Many manufacturing steps are required to produce ceramic FPGA devices. In the first stage, it takes a minimum of six months to procure and produce land grid array (LGA) packages, consisting of ceramic housings, along with necessary die bonding and lid sealing.

Then, it takes a reported additional six months for the current monopoly supplier to attach solder columns to convert the LGA package into a column grid array (CGA or CCGA). Finally, it takes months to perform final testing before the customer receives delivery. This lengthy procuration and production cycle can be significantly reduced by having multiple capable vendors, because they collectively have the bandwidth to perform column attachment services in weeks rather than many months.

New markets imminent. Emerging markets for AI and 5G utilize supersized organic packages, components too large for reliable BGA packaging. Alternative interconnects, other than solder balls, are needed to ensure reliability. This is a burgeoning market sector wherein solder columns can reduce stress caused by mismatches in the coefficient of thermal expansion (CTE) in the package and connection to PCBs. A new type of solder column utilizing copper braid, rather than copper wrapping, has the potential to dissipate more heat, while offering compliancy to extremely large AI and 5G base station packages.[1]

It's time for advocacy stakeholders to initiate a shared vision to ensure a robust, resilient, and sustainable supply chain for FPGA devices. Domestic manufacturing of copper-wrapped solder columns is already available. The next step is to qualify multiple microelectronic subcontractors ready and willing to

provide this process. A prudent investment today can mitigate the risk of waiting for an unexpected disaster to strike, potentially costing the defense industry hundreds of millions of dollars. A production stoppage of critical FPGA components could ultimately diminish market readiness. US manufacturing of copper-wrapped solder columns is available today. By the end of 2021, it is anticipated several subcontractors will offer column attachment services to the industry, once DLA is able to resume auditing and certifying new QML suppliers of column attachment services. Greater US government support to help fund programs to strengthen this critical area will result in enhanced readiness, greater security of supply, and fewer program delays caused by the potential inability to deliver FPGA components in a timely manner.

Where we go from here depends on raising the amplitude for a call to action. Not just rhetoric, but the successful execution of deliberate steps. The speed to which the current brittle market can be fortified depends on judicious access to funding, which will drive the next steps in the roadmap. For example, step one is the US Department of Defense funding an industry effort to strengthen the supply chain for attaching copper-wrapped solder columns to FPGA devices. Step two requires the engagement of subject matter experts (SME) with intimate knowledge of components used in the defense industry to vet proposals from the supply chain. If neither step is initiated, then step three should be initiated. In this step, the eight dominating ODM producers of FPGA components allocate reasonable funding to aggressively encourage multiple subcontractors to qualify solder column attachment services in preparation for certification by DLA. If none of those steps occurs, then we have step four, in which independent subcontractors in the supply chain deploy their own sources of funding to develop processes to attach solder columns to prepare for DLA certification. Step five follows, a proactive discussion with stakeholders, including the DoD, SMEs, FPGA makers and downstream customers to gain momentum for developing a resilient, robust supply chain for column attachment services. This course of action is much more desirable than waiting for calamity to strike. ▫

REFERENCES

1. Topline Corp., New Copper Braided Solder Columns for FPGA and Large Ceramic Modules, Jan. 1, 2020; www.topline.tv/pdffiles/Braided_Column_Introduction.pdf.

MARTIN HART is chief executive officer of TopLine Corp. (topline.tv) and holds a US patent related to CCGA assembly; hart@topline.tv.

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Print Productivity, Reliability and Remote Access: The Pillars of the Covid Era

Multitasking platforms are becoming the standard.

WHILE PRODUCTIVITY – MANUFACTURING more product, more efficiently in less time – has been center stage in electronics assembly for decades, today's razor-thin margins, coupled with the requirement for limited human intervention, have put an exclamation point on managing output proficiency. (This is especially true as the world restricts building access and maintains safe personal distances.) An optimized stencil printing process, as I've said many times, comes down to depositing the right volume in the right place at the right time. These are the three pillars of the print operation. Ultimately, for maximum productivity, a manufacturing operation needs a stencil printer that is always available and, when it is available, efficient and reliable.

It wasn't long ago the bottleneck on the production line was usually the placement machine, so the stencil printer was generally available and had plenty of time to run the print routine. With recent modular approaches to manufacturing line setups, however, this is no longer the case. Placement platforms have exponentially improved speed. The printer now must maintain a much faster pace; this starts with mechanics and cycle time. In mass production settings, getting a printer down to a core cycle time of five seconds has become a necessity.

> "For mass production, a **printer core cycle** time of 5 sec. has become a necessity."

Designing in technologies like three-stage conveyors and linear motors helps all systems work more efficiently. Take the understencil cleaner, for example, which is a complex, multi-stage device. While speed is important, cleaning takes time and should not always run faster just because it can. An intricate stencil may need a slower, more thorough clean. Linear motors enable the system to run faster during the cleaning process when appropriate and, even within slower, more methodical routines, facilitate movement of the cleaning head out of the print nest at an accelerated pace, reducing dead time and adding value with efficient, fast process cycle time.

Likewise, consumable replenishment is a time-constraining part of the understencil cleaning process. Changing the fabric roll can eat up as much as five minutes in best-case scenarios, and solvent replenishment also uses valuable production resources. The industry wants to be able to run an eight-hour shift without changing the fabric roll or adding solvent, so printer designs that allow this or enable multitasking (i.e., filling the solvent tank while the machine is running) are answering the productivity call.

Machine control and software capability are central to the productivity equation. Ensuring print platform availability also means not using vital production time for programming of the next product. Nor should the machine be sourced to run boards to get dialed into a process. Tools that allow offline programming, so the printer is ready to go as soon as the new product is loaded, provide greater system availability. Likewise, the capability to model a process offline and generate the ideal starting positions, and maintain alignment through self-diagnosis in real time during production, accelerates the throughput even more. Open software protocols aligned with Industry 4.0 objectives are now a requirement for output efficiency. Print systems that deliver on Hermes and CFX connectivity for open data communication to the line, factory and cloud are in demand for next-generation manufacturing.

At the end of the day, the goal is to build a stencil printing system that is reliable, run-ready for an entire shift and highly accurate. Naturally, there will be times when things don't go as planned. In the case of troubleshooting as well, modern solutions are required. Remote access to machines that allows service personnel to assess and correct issues from anywhere saves time, cost and valuable production resources. Today, with more open protocols and the Covid situation dictating limited factory access, remote factory management has enabled ongoing productivity at production sites around the world.

All this boils down to more reliable, self-directed, limited intervention required systems. It's important for productivity in normal production times with regular staffing and in challenging situations where limited personnel is the directive. Simply put, productivity is profitability. ❑

CLIVE ASHMORE
is global applied process engineering manager at ASM Assembly Systems, Printing Solutions Division (asmpt.com); clive.ashmore@asmpt.com. His column appears bimonthly.

Is SMT Ready for Low-Temperature Solders?

With no standard in sight, emerging alloys require unique fluxes and processes.

LOW-TEMPERATURE SOLDERING is a subject of considerable interest and development. Several forces are driving implementation of solders with lower peak reflow temperatures than SAC 305 and its variants. The most technically significant is reduced warping of component and substrates. Chip suppliers are particularly interested in lower reflow temperatures, as thinner components are needed to meet dimensional limitations of thinner, smaller and faster devices. When a component deforms during reflow, the solder interconnect may be compromised, resulting in non-wet opens (NWO). NWO defects are difficult to detect and may not manifest until after a product is in the field. Other advantages of low-temperature soldering include the incorporation of lower-cost plastics, component and laminate materials, and reduced energy consumption and related environmental benefits.

As a practical matter, SnBi alloys are the only elements available to reduce peak reflow temperatures. Unfortunately, high-bismuth alloys have a number of disadvantages compared with the tin/silver/copper alloys currently in use. Bismuth alloys exhibit poorer mechanical and thermal fatigue performance than SAC-based materials. Minor element additions and micro-alloy elements can improve the performance of SnBi alloys, but, in general, they will retain the properties of their main constituents and lack the reliability and performance of their SAC-based relatives. Even with these limitations, SnBi alloys can be adopted for use in SMT and through-hole, but the main benefits are derived in surface-mount assemblies.

Low-temperature alloys usually refer to alloys with peak reflow requirements lower than 190°C, with typical SnBi-based materials having peak reflow requirements of 170° to 190°C. The brittleness imparted by bismuth can be reduced by increasing the ratio of tin to bismuth from the eutectic Sn42Bi58. However, reducing bismuth content significantly increases the pasty/plastic range of the SnBi alloy, potentially impacting both process capability and product reliability. Incorporating additional elements into a SnBi system can improve mechanical and thermal performance but can increase melting temperature, thus negating the primary reason for adopting low-temperature materials, or even adversely impacting processing characteristics. Historically, silver has been used with SnBi to improve strength and is a common SnBi addition. Other elements incorporated are copper, which slightly reduces the melting temperature and improves mechanical performance. Antimony will also improve strength but can significantly increase melting temperature, while nickel will suppress brittle intermetallic formation at the joint interface. These additives also impact alloy ductility (reduced brittleness), depending on the amount incorporated. In addition to these alloy challenges, entirely new flux systems need to be developed to address the unique properties of bismuth-bearing alloys. Not only do these alloys have different mechanical and thermal properties, their soldering characteristics and requirements can be quite different from the SAC alloys they replace.

In addition to the alloy element variables, the new alloys must be compatible with other materials on the PCB. The effects of surface finish, component tinning and other soldered surfaces are yet to be clearly defined. Solder suppliers are promoting many low-temperature alloy options, and a "standard" has yet to emerge. With all these input variables, constituent elements, additive elements, and their amount and effect on solder alloy performance, a single low-temperature alloy is unlikely to meet all application requirements.

SAC alloys are successful substitutes – albeit with considerable expense and disruption – for most electronics applications. Now, with nearly 20 years of history, most industries are comfortable with the SAC alloy system performance and requirements. As the electronics world continues to evolve, lower temperature alloys are the next frontier of solder interconnect materials. Some industries can adopt low-temperature systems relatively easily with minimal risk, with consumer and disposable applications likely to be early adopters due to cost advantages. Other industries will watch these developments carefully to understand the hidden risks and requirements. The question for most users is can or should I use low temperature on my assemblies? The answer is complicated by the number of available options, the risk/reward equation and the resources required in investigating and developing a viable low-temperature assembly process. We say it often, but let your solder supplier help guide you. □

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Root Causes of Component Lifting

Soldering in nitrogen or vapor phase environments can increase the likelihood.

BOB WILLIS
is a process engineering consultant; bob@bobwillis.co.uk. His column appears monthly.

SUBTLE COMPONENT LIFTING can be an issue to find during inspection. Most modern AOI systems should be able to detect drawbridging on small passive and active parts. Old systems may struggle with defects like the two shown in **FIGURE 1**.

There are many papers on lifting of parts during reflow and many suggestions on the root causes. In our experience, the most common reasons are excess solder paste, an excessively thick stencil, or poor pad design. These issues are exaggerated by fast wetting, as seen in nitrogen and vapor phase soldering. To be clear, nitrogen or vapor phase do not cause lifting; they just increase the possibility of component lift.

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at youtube.com/user/mrbobwillis. □

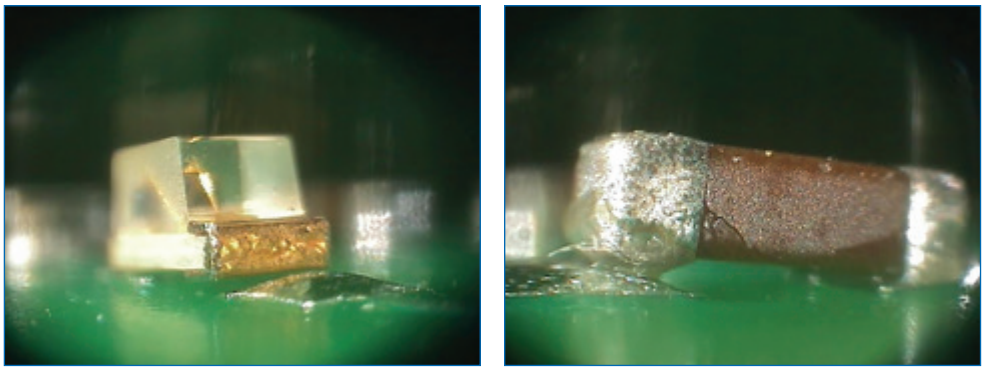
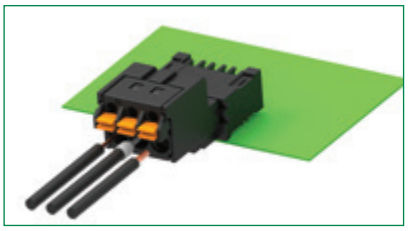


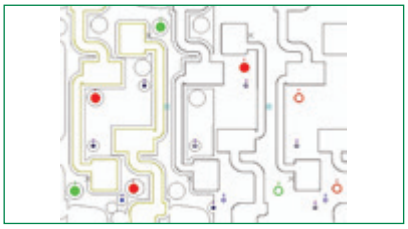
FIGURE 1. Passive parts printed with excessive solder or on incorrect pads are more susceptible to lift.



WIRE-TO-BOARD CONNECTORS

D-2970 Dynamic series compact wire-to-board PCB connectors have field-installable push-in clamp terminations. 5mm-pitch PCB connector operates at up to 20A and 400V at a typical ambient application temp. of 55°C without further derating. Features include audible and tactile locking latch, contacts that support shock- and vibration-exposed applications, and IP20 finger-safe housing. Push-in clamp and single-hand-operating center-locking lever reportedly cut mating time up to 90%.

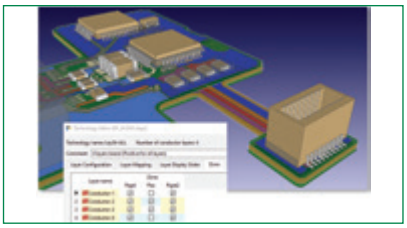
TE Connectivity
te.com



FLEX TOOLING CAM

InCAM Pro 2.1 offers intelligent flex tooling hole placement in which all flex tooling holes on the board are visible at a glance. Adds and manipulates flex tooling holes on a new graphic mask layer that maps all flex tooling holes on the printed circuit board. The mask provides visibility to other layers when working with flex tooling holes. Automatically synchronizes tooling holes with relevant layers, saving hours of work and ensuring accuracy.

Frontline PCB
frontline-pcb.com



3-D MULTI-BOARD CAD

CR-8000 2020 has improved design efficiency, comprehensive system-level design and verification, and support for the latest advancements in packaging technology. Includes enhancements in schematic design, FPGA optimization, skew group routing and support of back-drilled vias; electro-mechanical co-design of flex-rigid PCBs and multi-domain analysis through direct integration of products from Keysight and Ansys; functionality for tile bump and 3-D wire design planning.

Zuken
zuken.com/en/cr-8000-whatsnew

OTHERS OF NOTE

AUTOMOTIVE MLCC

NFM18HC106D0G3L three-terminal low-ESL MLCC is for automotive safety-critical applications. Delivers capacitance of 10µF in a 0603 (1.6 x 0.8mm) package. Reportedly features capacitance 10x higher than similarly sized products.

Murata Electronics
murata.com

3-D MODEL VIEWER

3-D viewer previews 3-D models available on SnapEDA before download. New features include dimensions to verify measurements before downloading; ability to zoom in and out with mouse wheel; ability to rotate parts to see them from every angle. For immediate visual feedback of designs, confirming clearances between component and enclosure or between other components, and verifying correct positions of component outlines and part designators. View measurements of models.

SnapEDA
snapeda.com

THIN-FILM CHIP RESISTORS

CSRT resistors offer resistance values from 10mΩ to 10Ω, with TCR ranging from 50 to 200ppm, depending on resistance value. Sizes and power ratings range from 0.2W for 0201 to 3W for 2512. Low TCR and higher relative resistance value are for power supplies for currents between 2A and 17A, industrial power control, consumer electronics, telecom, computer, measurement equipment, battery management, and LED drivers.

Stackpole Electronics
seielect.com

PE ADHESIVE

IQ-Bond 5976-ACE provides adhesion strength on different flex and rigid substrates, such as PET, polyimide, FR-4, copper, aluminum and silver. Has been tested in moisture (85°C/85%RH – 1,000 hr.), as well as temp. cycling (-40°/+125°C) testing. Cures in seconds with thermode or induction curing systems, enabling assembly of 20,000 to 40,000 microchips per hr. on flip-chip production systems.

Roartis
iq-bond.com

CARBON POTENTIOMETER

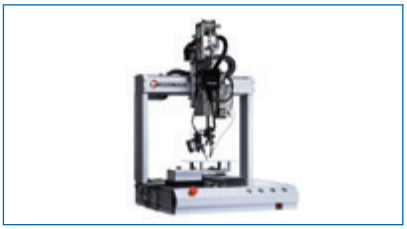
PT-6 is for high-temperature Pb-free SMD production. Features high-temperature plastics, flat suction areas for vacuum pipettes and a new pad design for automated placement on PCBs using reflow soldering. Options include stop positions (detents) that provide users tactile feedback on each position setting and selection. Detent feature is for 6mm potentiometer lines. Detents include up to 10 equally spaced positions, have a spring feature incorporated into rotary action, and can be set at custom angles.

Piher Sensing Systems
piher.net/sensors/

BLIND MICROVIA FILL

Systek UVF 100 is a 2-in-1 plating system for buildup of redistribution layers. Pattern plating process fills blind microvias and laser-drilled x-vias, as well as plating fine lines, pads, and other surface features with coplanarity and controlled profile. RDL blind microvias and x-vias can be filled with dimples of less than 5µm and overfill of less than 3µm.

MacDermid Alpha Electronics Solutions
macdermidalpha.com



1-HEAD SOLDERING ROBOT

TMT-R8000S has one head to simplify and automate hand soldering processes with precision ballscrews, servo motors and IP software. Includes vision/mapping, fiducial marks and dynamic laser height control. Separate drive motor for adjustable solder wire feeder.

Thermaltronics
thermaltronics.com

HEAVY DUTY SCARA ROBOTS

YK610XE-10 Scara robot has 610mm arm length. YK710XE-10 Scara robot has 710mm arm length. Both deliver 10kg max. payload and standard cycle time of 0.39 sec. (YK610XE-10) and 0.42 sec. (YK710XE-10). Cover broader range of applications, encompassing assembly, conveyance, and sorting of small and large components.

Yamaha Motor Corp.
global.yamaha-motor.com/business/robot/

LARGE BOARD AXI

V810i 3-D x-ray inspection system inspects PCBs weighing up to 25kg. PCBs up to 1.3m x 1.3m can be inspected. Features algebraic reconstruction technique with model of sharp geometric 3-D CT. Produces quality images with digital tomosynthesis and x-ray autofocus technology. Inspects all forms of defects in SMT and PTH components. Monitors radiation exposures on component.

ViTrox Technologies
vitrox.com

OTHERS OF NOTE

PRINTER WITH JAR DISPENSER

MPM Momentum II 100 has footprint of 56" x 47". Features new cover set with larger window and wider access inside printer. Quick-release squeegee requires no tools; takes less than 30 sec. to change blade. Jar or cartridge dispenser. Windows 10 operating software. QuickStart programming included. Paste management system enables Industry 4.0 traceability. Includes paste temperature monitor, measured for proper paste viscosity, and roll height monitor that measures upper and lower limits.

ITW EAE
itweae.com

PLASMA-BASED FLUX ACTIVATOR

PlasmaFluxer uses cold-active plasma to melt micrometer-sized powder of adipic acid and deposit it on PCB. Liquid carrier material reportedly not needed. Nitrogen used to create plasma flame. Aerosol formed from meltable flux particles. and nitrogen is led into plasma flame and directed to PCB surface. Once aerosols touch surface, particles solidify and form long-term coating. Substitutes wet-chemical flux activation with dry process. Soldering results are reportedly comparable to standard liquid fluxes.

Seho
seho.de

LOW R TIM

Sarcon PG45A is a putty-like thermal interface material. Modulus gap filler exhibits thermal resistance as low as 0.02°C•in²/W at 43.5PSI with thermal conductivity of 4.5W/m°K. Requires low compression force at high compression rates. For applications with delicate or wide-variation component heights requiring material compression up to 70-90%. Comes in sheet thicknesses of 1.5, 2.0 and 2.5mm up to a max. dimension of 300mm x 200mm. For environments with operating temp. ranging from -40° to +150°C.

Fujipoly America
fujipoly.com

DISPENSING COMPONENTS

Optimum ECO components include syringe barrels, pistons, end caps, and tip caps. Are molded using up to 96% bio-based Polyethylene resin derived from sugarcane. Deliver repeatable fluid dispensing results while reducing waste. Include 3cc, 5cc, 10cc, 30cc, and 55cc syringe barrels and pistons. Are used in precision fluid dispensing applications. Are sustainably sourced.

Nordson EFD
nordsonefd.com

WIREBOND AOI

TR7700QE-S 3-D AOI inspects and detects defects in wirebonds, die bonds, SMD, bumps, wafer IC/chip, underfill, and solder joints. Metrology capabilities provide high accuracy and repeatability. Has 5.5µm high-resolution 12MP imaging technology.

Test Research Inc.
tri.com.tw/en

PARTS INSERTION ROBOT

MCell Insertion is software-defined robot for inserting electronic components. MCell Insertion uses ABB YuMi collaborative robots, feeders, zero touch programming and can be installed and deployed remotely. Uses MBrain, part of factory intelligence system, to deliver zero touch programming, as well as performance data.

MTEK
mtekusa.com

In Case You Missed It

Plating

"Vertical Interconnections by Electroless Au Deposition on Electroless Ni Immersion Au Surface Finish"

Authors: I. A. Weng, H. T. Hung, W. C. Huang, C. R. Kao and Y. H. Chen

Abstract: Electroless Au is used to vertically connect copper pillars with electroless Ni immersion Au surface finish on two stacked chips by a microfluidic electroless interconnection process. A low bonding temperature of 50°C and a pressure-less bonding process can be achieved. The vertical interconnections are formed by a forced flow of electroless Au plating solution through a microchannel, so the reduced Au atoms self-assemble between the gaps of facing copper pillars to complete the interconnections. The deposited Au grains span the entire gap across the two copper pillars, suggesting the rate-limiting step is more likely to be the nucleation than the growth of the Au grains. Four-point probe measurements show the average resistance of the electroless-Au-bonded interconnections is low. Mechanical shear testing reveals the bonding of the interconnections is strong. Further, it is demonstrated that this process can accommodate a high degree of pillar misalignment. (*Journal of Electronic Materials,* Jun. 5, 2020; link.springer.com/article/10.1007/s11664-020-08245-0)

Smart Devices

"The Journey Towards Intelligent Catheters"

Author: Joe Rowan

Abstract: New intelligent catheters are eschewing conventional designs involving twisted pair coaxial and flexible printed circuit technology in favor of microwaves insulated with innovative shielding/grounding materials. Multi-Filar cables have a capacity of up to 60 power lines – depending on AWG size or pitch – and are designed to provide not only increased functionality but also more signals into formerly inaccessible areas of the body. Using precision-engineered PTFE lamination technology, single strand configurations are joined into a Multi-Filar assembly that can be used in electrophysiology catheters for applying pacing and recording protocols from inside the heart, ablation and balloon ablation catheters for atrial fibrillation, as well as cardiac mapping. The Multi-Filar technique also permits easier assembly of the signal or power wires into the final medical device, making the manufacturing process simpler and more cost-effective. (*Medical Plastic News,* Jun. 16, 2020, www.medicalplasticsnews.com/news/the-journey-towards-intelligent-catheters)

Solder Materials

"Attachment Quality and Thermal Fatigue Reliability of a Surface Mount Chip Resistor Assembled with a Low-Temperature Solder"

Authors: Charmaine Johnson, Richard Coyle, Ph.D., Martin Anselm, Ph.D., *et al.*

Abstract: Technical, economic, and environmental requirements are driving the development and usage of low-temperature solders (LTS) for electronics assembly. The leading alloy candidates for achieving soldering below 200°C are based on the BiSn solder system that has a melting point of 138°C at its eutectic composition. One concern with these alloys is low thermal fatigue life, which has been linked to their characteristically brittle, two-phase lamellar microstructure. The industry has been focused largely on the challenges of mixed metallurgy BGA assembly (SAC BGA assembled with LTS paste), while a gap exists in assembly and reliability data for other components attached solely with an LTS paste. In this study, a daisy-chained PCB test vehicle was used to evaluate the thermal fatigue reliability of the solder joints of a 2512 chip resistor assembled with a commercial LTS compared to a SAC 305 performance baseline. Two PCB surface finishes were included as variables: immersion Ag (IAg) and immersion Sn (ImmSn). ImmSn may have solderability limitations due to CuSn intermetallic growth and oxidation resulting from multiple reflow processes or exposure during long-term storage. The potential for final finish degradation and loss of solderability was addressed using high-temperature storage and reflow preconditioning as additional variables. Thermal cycling was used to characterize and compare the resistor thermal fatigue reliability with LTS and SAC 305, and to assess any effects of surface finish and preconditioning. The interconnect metallurgy and microstructural characterization were compared for all solder alloys and surface finishes and discussed in relation to the thermal cycling results. (SMTA e-news, vol. 15, no. 14, Jul. 9, 2020)

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

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ZESTRON ACADEMY

SIEMENS
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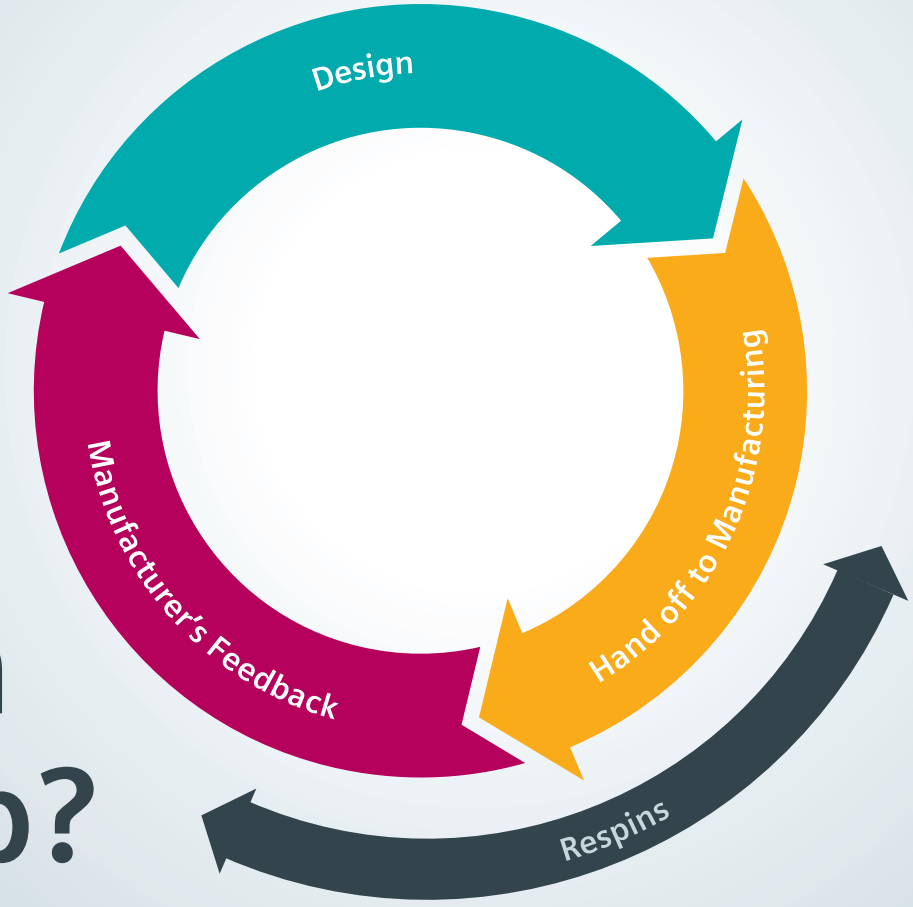

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