IPC Apex Expo Recap, p. 29

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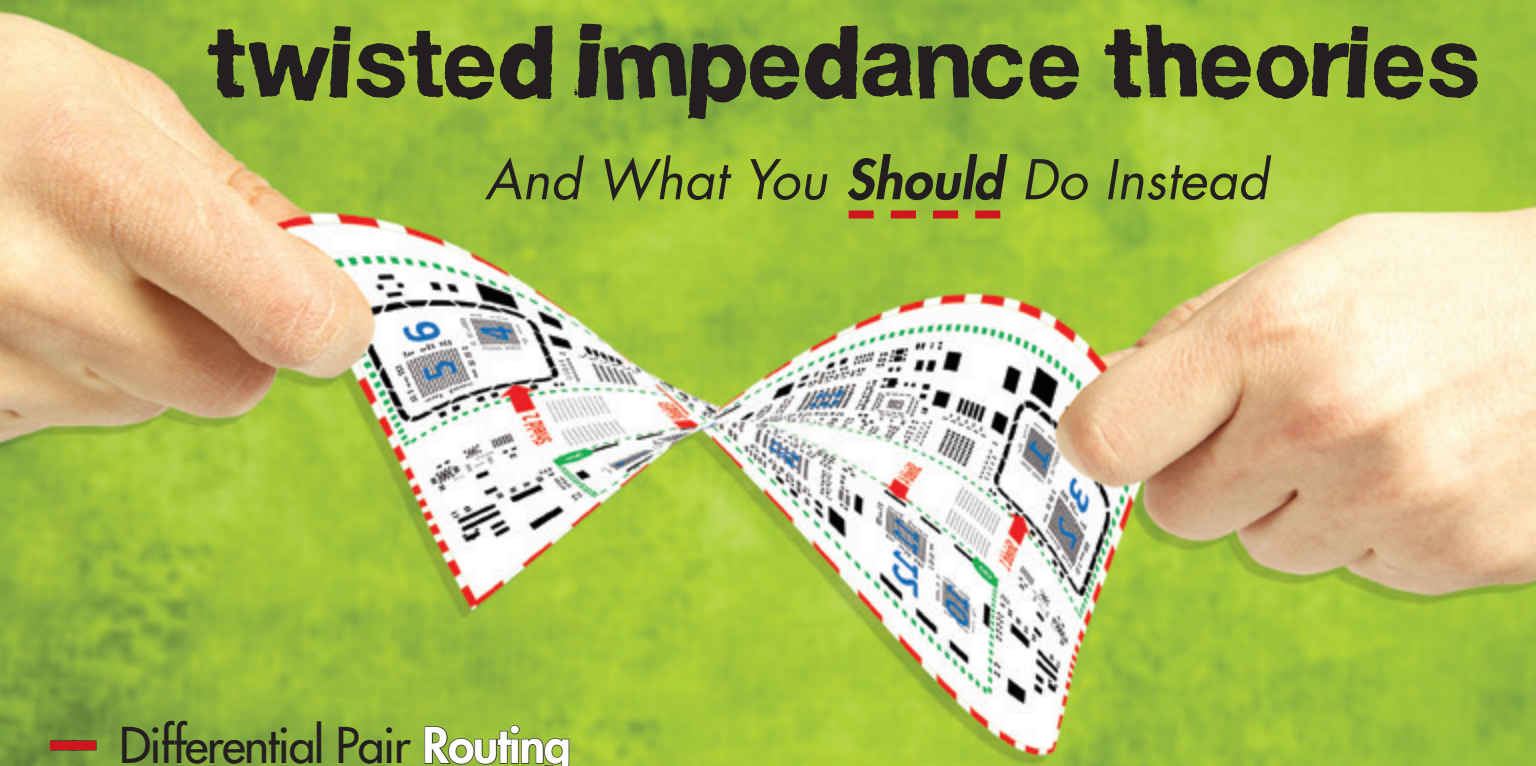
March 2020

PRINTED CIRCUIT DESIGN & FAB

CIRCUITS ASSEMBLY

twisted impedance theories

*And What You **Should** Do Instead*



- Differential Pair Routing
- Stencil Tension Effects
- Is X-ray AI a False Call?

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MARCH 2020 • VOL. 37 • NO. 3

PRINTED CIRCUIT DESIGN & FAB CIRCUITS ASSEMBLY

FIRST PERSON

MONEY MATTERS

TECH TALK

FEATURES

About that cover:
Yes, that's a stencil (thanks, ASM!), not a board. But we liked the way it looked.

IN THE DIGITAL EDITION

DEPARTMENTS

ON PCB CHAT (pcbchat.com)

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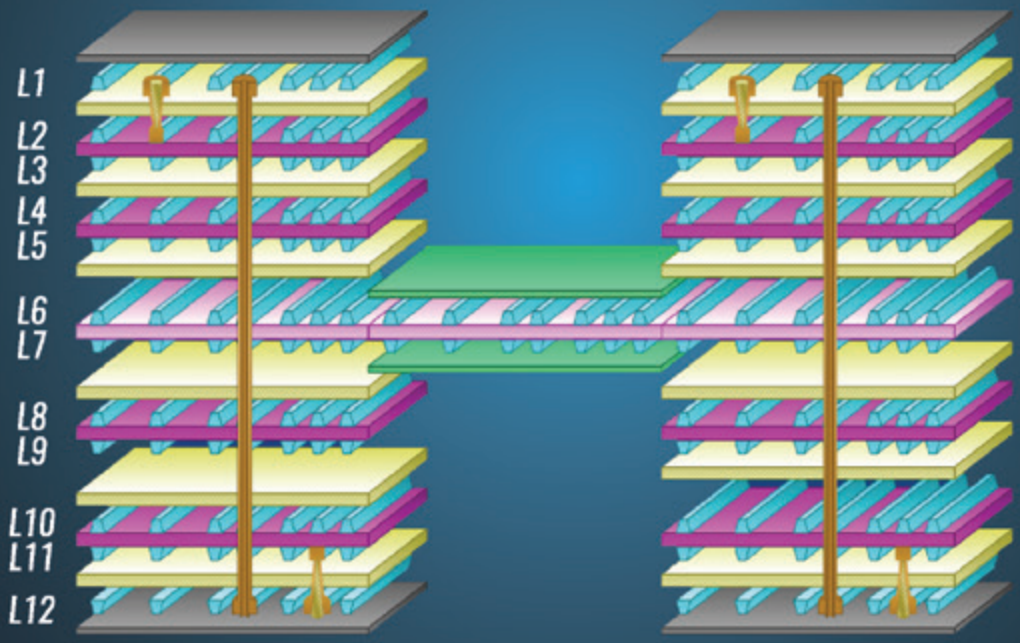
Blind Via L1-L2 & L11-L12, 0.003" Hole, Resin Filled,
0.002"/0.002" Trace/Space, Controlled Impedance



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MIKE BUETOW
EDITOR-IN-CHIEF

Finding the Spotlight

IN 2018 the US Department of Commerce conducted an industrywide survey of all the nation's printed circuit board manufacturers. Fabricators groused about the scale of the paperwork, which was massive, as well as the focus of the questions, which in many cases required extraordinary data mining to provide the sought-after information. Still, the rationale for the Bare Printed Circuit Board Supply Chain Assessment was sound: That American PCB capacity issues extend beyond military needs into the medical, automotive and telecom sectors, and that Washington was largely unaware of the degree the nation's supply base has degraded relative to the rest of the world over the past two decades.

The findings made it into an interagency report titled "Assessing and Strengthening the Manufacturing and Defense Industrial Base and Supply Chain Resiliency of the United States" and was provided to President Trump that same year, showing bureaucracy is still capable of moving at times. Even better, they correctly summarized the situation:

> In multiple cases, the sole remaining domestic producer of materials critical to DoD [is] on the verge of shutting down their U.S. factory and importing lower cost materials from the same foreign producer country who is forcing them out of domestic production.... The case of printed circuit boards likewise highlights the growing risks to the industrial base.... Today, 90% of worldwide printed circuit board production is in Asia, over half of which occurs in China; and the U.S. printed circuit board sub-sector is aging, constricting, and failing to maintain the state of the art for rigid and rigid-flex printed circuit board production capability. With the migration of advanced board manufacturing offshore, DoD risks losing visibility into the manufacturing provenance of its products, as many domestic manufacturers have offshore manufacturing facilities or relationships. In addition to the potential dissemination of design information, many of the offshore facilities do not meet or comply with DoD quality requirements.

Fast forward to today. Has the effort paid off?

It depends on whom you ask. The interagency report called for "relief from unlawful and otherwise unfair trade practices." The ongoing tariffs speak – loudly – that the message was received at the highest level of government.

The report also mentioned the DoD Executive Agent for Printed Circuit Board Technology. But it failed to advocate for funding, and today there appears little progress. While the position exists, critics say the infrastructure needed to make it an effective part of an improved and lasting procurement process is MIA.

A critical agency of Commerce Department is the Bureau of Industry and Security. One mission of BIS is to "work with industry to protect the health and vitality of the US defense industrial base, resulting in a stronger US economy." But BIC's presentation in support of the President's fiscal 2020 budget ignores printed circuits.

There is a disconnect between the goals of the Defense Department and those of Commerce. The former is concerned with security, the latter the entire industrial marketplace. The EA's role is tied to the former and is highly political. Funding comes from earmarks, subject more to legislative whim than an overarching strategy. IPC seems to recognize this, stating that "direct funding is needed for the PCB EA to competently fulfill the congressional mandates."

I would argue automotive, medical and telecom are equally important to the US, especially in the wake of 5G and the concerns over Huawei, because our strength lies not just in our capacity to make weapons but our ability to leverage our economic might in pursuit of national objectives. As such, I wonder whether the EA would be more effective as a part of Commerce, rather than Defense.

I put the question to Chris Mitchell, vice president of global government relations at IPC. Mitchell continues to believe the EA is best placed within Defense, which has access to resources and is philosophically in line with the industry's concerns over supply chain resiliency, innovation and security.

That said, he adds that the challenge for the EA and industry is to raise the profile of our concerns among decision-makers in government. where electronics manufacturing hasn't always fared well.

I do wonder if, in this age of government by tweet, a more aggressive approach would be more effective. And I worry, if we cannot find consistent funding for the spot in a decade-long upturn, how we will do so in a recession.

Mitchell seems convinced progress is there. There is "real change" taking place at the DoD, he says, where a host of factors are leading a charge for greater transparency over the entire supply chain. "Electronics is an ecosystem, and the entire ecosystem needs to be strong for Defense to have its needs met. International, technological and economic events are driving policymakers to have a greater appreciation for this ecosystem." The EA, it seems, is a reflection of the greater electronics manufacturing industry's ability to attract the government spotlight. Is that enough?

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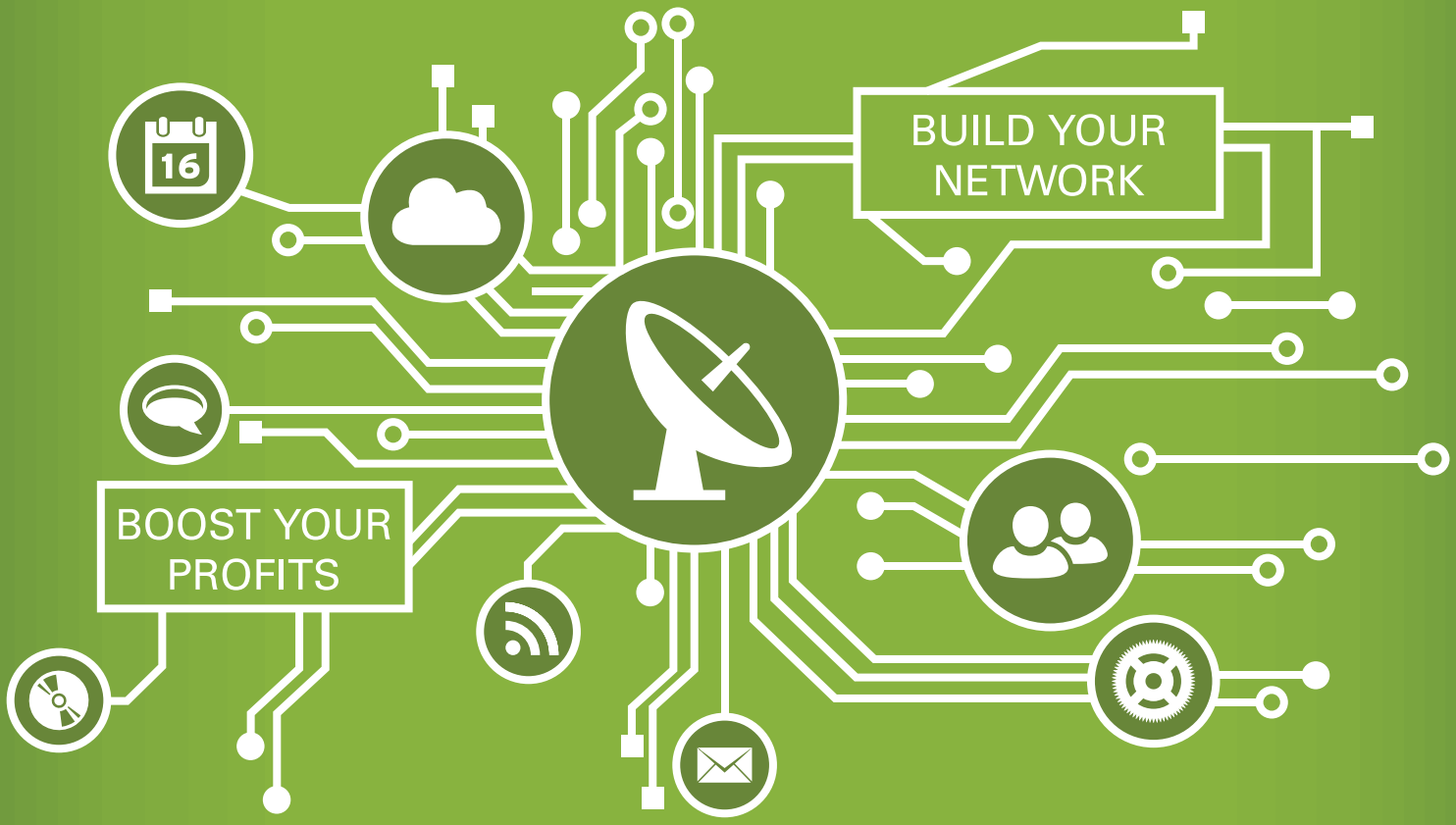
@mikebuetow

The *Circuits Assembly* *Directory of EMS Companies*



- Build your EMS database
- 3,000+ facilities worldwide
- Sortable in Excel
- Unrestricted use
- Includes contact info, no. of lines, markets served and more!

CIRCUITS ASSEMBLY

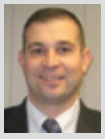
circuitsassembly.com/dems

PCDF People

Bowman XRF named **Rob Coleman** sales manager for North America, responsible for XRF instrument sales and service. He was most recently Midwest sales manager for Uyemura, and previously vice president of operations for American Standard Circuits.

Kunal Shah, Ph.D., of LiloTree won the IPC Apex Expo best paper award in the domestic paper category for "Reliable Nickel-Free Surface Finish Solution for High-Frequency-HDI PCB Applications."

Mentor named **Mark Forbes** product marketing specialist.



RBP Chemical Technology promoted **Ernest Litynski** to president. He had been vice president of operations since 2010.

Ventec appointed **Leigh Allinson** technical sales manager, UK. He has over 28 years' technical and sales experience in PCBs with MacDermid Alpha and eXception PCB.

PCDF Briefs

The 2020 International Electronic Circuits (Shanghai) Exhibition, originally scheduled for Mar. 16-18, is postponed in response to China's coronavirus outbreak.

American Standard Circuits has licensed **Averatek's** A-SAP PCB manufacturing technology.

Apex Circuit, a subsidiary of **Taiding**, the largest PCB manufacturer in Thailand, has approved a 670 million baht ($21.6 million) plant in Sinsakhon Industrial Park.

Atotech is planning to list on the New York Stock Exchange.

Averatek announced **Calumet Electronics** as its first A-SAP licensee.

The Center for Systems Science and Engineering has launched an online dashboard that is tracking the spread of the deadly coronavirus as it makes its way across China and beyond.

DuPont is reportedly discussing with advisers the possible sale of its electronics business.

DuPont Interconnect Solutions named **Insulectro** distributor of its Pyralux flexible circuit materials in Canada.

FTG received AS9100D certification for its PCB manufacturing facility in Fredericksburg, VA (formerly **Colonial Circuits**).

Printer OEM Inkjets Conductors Inside Via Holes

MIGDAL HA'EMEK, ISRAEL – An inkjet-based conductive digital printer maker announced it has successfully printed and tested a novel method for printing inside vias.

PV Nano Cell said it printed inside vias 0.6mm (0.024") in diameter and 1mm (0.04") high on an FR-4 substrate. The printed vias were measured at a minimal resistance of 0.1Ω.

One side of the substrate is a printed pattern consisting of multiple widths and thicknesses (heights) of conductive features. This pattern forms an accurate resistor that heats to high temperature in less than milliseconds.

The company said it could print smaller-sized vias as well.

"In this special application, we first print inside the via," explained Dr. Fernando de la Vega, chief executive, PV Nano Cell. "Then we print the first designated pattern on one side of the FR-4. The substrate is then flipped over, and we print the second designated pattern on the other side of the FR-4. The via printed in the beginning of the process electrically connects between the two patterns printed on the two sides of the substrate.

"The unique printing process that we developed cuts approximately 50% of the cost of production compared to the existing manufacturing solution. We are positive we can improve the process even more and print smaller-sized vias."

Hanan Markovich, chief of business development, added, "The printed parts have gone through intensive, demanding standard testing by the customer, and we expect the production to begin in the near future. Such an achievement demonstrates the feasibility and attractiveness for mass-production applications."

PV Nano Cell said the technologies allow customers to fully realize the potential of inkjet-based electronics printing for mass production applications. The company also makes silver-based conductive inks. – *MB*

Plexus to Close Colorado Design Center

LOUISVILLE, CO – Plexus is closing its Plexus Boulder Design Center here, eliminating 104 jobs, according to reports. The move comes two years after the firm moved into the facility.

Plexus filed a notice with the Colorado Department of Labor on Jan. 22. The closure is scheduled for Mar. 22.

Layoffs will include engineers, project managers and management/administrative personnel.

Plexus plans to consolidate the Boulder operation with a facility in Boise, ID, and cites certain engineering programs that will cease.

"We are proactively responding to the engineering program pauses by strategically repositioning our Boulder Design Center to colocate with our existing manufacturing facility in Boise, Idaho," Plexus president and CEO Todd Kelsey said. "This opportunity will allow for the creation of an Aerospace and Defense Center of Excellence. This combination of engineering and manufacturing services will provide the synergies and cost advantages of a campus environment, while delivering a compelling service offering for our customers in the aerospace and defense sector." – *CD*

TTM to Sell 4 China Manufacturing Plants, Exit Mobility Business

SANTA ANA, CA – TTM Technologies has agreed to divest its four China manufacturing plants comprising substantially all the assets of its Mobility business unit as a separate enterprise for $550 million in cash consideration.

The buyer is AKMMeadville Electronics (Xiamen) Co., a Chinese consortium consisting of Meizhi Investment (Xiamen) Co., Xiamen Semiconductor Investment

Group, AKM Electronics Industrial (Panyu) and Anmei Ventures (Xiamen).

The sale does not include certain accounts receivable of the divested business, estimated to be $110 million in cash receivable to TTM.

"After years of double-digit growth, the cellular market has matured, resulting in lower growth rates," said Tom Edman, CEO of TTM. "However, this market still demands substantial investment and capital commitments. In addition, the cellular market is highly seasonal and is driven by short-term product cycles. The combination of these trends posed increasing challenges to our strategic direction and desired business model. We are pleased to have found a buyer we believe is stra-

InspectAR Augmented Interfaces, whose technology helps simplify the production of printed circuit boards, has received an $850,000 investment from **Royal Circuits** and **Advanced Assembly**.

Seica opened a new test house and demo center in Los Angeles.

The government of Tianjin is discussing the sale of two firms, including **Tianjin Printronics Circuit**, according to reports.

The continued epidemic in Wuhan will directly impact Hubei, mainland China's production center for memory chip displays and PCBs, and will also affect the start time in other provinces in the mainland, while resulting in the "blockage" in the supply of three electronic key components, **TPCA** said.

ZHKRPCB launched PCB Instant Quote online ordering service.

CA People

Advanced Assembly announced **Jorge Ramos** as quality assurance manager.

Advanced Instruments named **Joe Perault** manufacturing engineering manager.

AIM appointed **Leopoldo Valdez** sales manager for Central and Western Mexico.

Akrometrix promoted **Neil Hubble** to president.

Automation Engineering named **Jean-Marc Peallat** general manager and vice president.

BJG Electronics named **Kent Smith** president.

BTU named **Brandon Hannaman** regional sales manager for Arizona, Southern California and Mexico. He has been in the industry for more than 18 years as a field service technician, IT manager, and most recently product manager.

Enics named **Markus Jeck** general manager.

Enics appointed **Udo Streller**, Ph.D., chief operations officer. He spent the past 22 years with Osram Opto Semiconductors in a variety of technical and management roles.

Hanwha Techwin promoted **Bryce Timms** to regional sales manager.

Indium promoted **Claire Hotvedt** to product development specialist.

Inovar named **Gregory Bradfield** president, Logan Division. He joins from L3 Harris, where he was vice president of operations for Communication Systems. He also served in various leadership roles at Raytheon, Boeing, Applied Materials and Austin Semiconductor.

Insituware named **Denis Barbini**, Ph.D., chief scientist. He has held roles in product marketing and management at Vitronics-Soltec, AREA Consortium and Crucial Machines.

IPC named **Matt Kelly** chief technologist. He will focus on factory of the future standards and technical research; industry intelligence funding; and the creation and launch of an Industry CTO Council. He comes to IPC following a 14-year career at IBM.

IPC inducted **Steve Pudles** into the IPC Raymond E. Pritchard Hall of Fame. Currently president and CEO of Zentech Manufacturing, Pudles has been an active IPC volunteer and leader for more than three decades.

Libra Industries named **David Chavez** vice president of integrated business development.

Microart Services hired **Charles Tonna** as executive vice president.

Promation named **Kevin Brennan** sales manager for PCB handling systems and automation.

Rocket EMS hired **Ofer Maltiel** as strategic sales director. He spent eight years leading the hardware engineering team for a startup that created the first smart, connected underwater navigation systems.

Saki America named **Jeff Mogensen** general manager. He has nearly 40 years of experience in electronics equipment sales, including key account manager, vice president of sales, and general manager for MPM, Parmi and CyberOptics.

Varitron promoted **Leah Slaughter** to vice president of supply chain, customer experience and AI program.

Virtex named **Shawn Brady** business development manager.

Z-Axis named **Matt Switzer** quoting engineer and **Katie Boesl** process engineer.

Zentech named **Jason Glass** chief financial officer.

tegically committed to cellular market leadership, growing the Mobility business and supporting the customers and the approximately 7,500 employees that support this business. We expect after the transaction is complete, the remaining TTM business should be less seasonal and more exposed to longer cycle markets that fit our strategic direction. We remain excited about the anticipated growth opportunities in 5G base stations, cloud data centers, aerospace and defense electronics, and increasing automotive electronic content."

In the 12 months ended Sept. 30, the Mobility business unit generated revenues of $528 million, non-GAAP operating income of $5.5 million and adjusted EBITDA of $82.5 million. – *CD*

CIRCUITS ASSEMBLY Announces 2020 Service Excellence Award Winners

SAN DIEGO – CIRCUITS ASSEMBLY announced the winners of its 2020 Service Excellence Awards (SEAs) for EMS providers and electronics assembly equipment, materials and software suppliers. CIRCUITS ASSEMBLY recognized companies that received the highest customer service ratings, as judged by their own customers, during a ceremony at IPC Apex Expo in San Diego.

In the EMS category, the overall winners were Kimball Electronics (sales over $500 million), Mack Technologies (sales of $101 million to $500 million), Qualitel (sales of $20 million to $100 million), and XLR8 Services (sales under $20 million).

The EMS companies with the highest scores in each of five individual service categories also received awards. (Overall winners were excluded from winning individual categories.) In the small-company category, Silicon Forest Electronics won for dependability/timely delivery and responsiveness. MacroFab took top honors for manufacturing quality and tied Spectrum Assembly for technology and value.

For firms with revenue between $101 million and $500 million, Applied Technical Services took home all five individual category awards, tying Firstronic for value.

For EMS companies with revenue over $500 million, Creation Technologies won for dependability/timely delivery, responsiveness, technology and value. NEO Tech took first prize for manufacturing quality.

"The EMS industry gets more global and more competitive every year," said CIRCUITS ASSEMBLY editor in chief Mike Buetow, in presenting the awards. "That many of this year's recipients are repeat winners suggests they have developed a model and culture that breeds consistent excellence."

Electronics assembly supplier award winners were Europlacer Americas for pick-and-place; Speedprint Technology for screen printing; Kyzen for cleaning/processing materials; MIRTEC for test and inspection; Nordson Asymtek for dispensing; ECD for soldering equipment; Aegis Industrial Software for automation/manufacturing software; Count On Tools for automation/handling equipment; Data I/O for device programming equipment; ECD for component storage systems; and Datest for test laboratories.

Customers of SEA participants rated each company on a scale of 1 (poor) to 7 (best in class) in five service categories.

This is the 28th year CIRCUITS ASSEMBLY has sponsored the awards program. – *CD*

CIRCUITS ASSEMBLY, PCD&F Announce 2020 NPI Award Winners

SAN DIEGO – CIRCUITS ASSEMBLY and PRINTED CIRCUIT DESIGN AND FAB announced the 2020 New Product Introduction Award winners for electronics assembly equipment, materials, software, and PCB fabrication.

The 13th annual NPI Awards recognize leading new products during the past 12 months. An independent panel of practicing industry engineers selected the recipients.

The winners are:

- Air-Vac Engineering: Rework and Repair Tools (AVX250)
- Anda Technologies: Cleaning Equipment (AP-3P)
- Anda Technologies: Curing Ovens (VCO Series)
- ASM Assembly Systems: Component Placement – Accessory Technologies (Siplace SmartFeeder AutoRefill)
- Cogiscan: Software – Production (Quality Driver Software Suite)
- CyberOptics: Software – Process Control (CyberCMM)
- CyberOptics: Test & Inspection – SPI (SQ3000)
- Data I/O: Device Programming (PSV2800)
- Hanwha Techwin: Component Placement – High Speed (HM520)
- Henkel: Thermal Interface Materials (Bergquist Gap Pad TGP 10000ULM)
- Indium: Soldering Materials (Durafuse LT)
- Inspire Solutions: Automation Tools (Toolmaker)
- ITW EAE: Soldering – Wave (Electrovert DwellFlex 4.0)
- Juki: Component Placement – Multi-Function (JM-100)
- Kyzen: Cleaning Materials (Kyzen E5631)

CA Briefs

Amtech is selling its solar unit and will concentrate on its thermal processing businesses, including **BTU**.

Apple has a goal to become a closed-loop manufacturer.

Apple has asked suppliers to make up to 80 million iPhones over the first half of this year, reports say, up 10% from last year, but suppliers fear fallout from the coronavirus.

BlueRing Stencils acquired **Stone Mountain Tool** for an undisclosed sum.

BTU now supports the Hermes Standard, officially referred to as IPC-Hermes-9852.

Compal Electronics is planning a second plant in Vietnam, with its first reaching full capacity around the second quarter of this year.

Critical Manufacturing appointed **Technica** representative in California, Nevada, Washington, Oregon, Idaho, Utah, Arizona, New Mexico, Montana and Wyoming.

Critical Manufacturing appointed **FHP Reps** representatives in Texas, Oklahoma, Arkansas, Louisiana, Missouri, Nebraska and Kansas.

EMS firm **Electronic Technicians (ETL)** has been acquired via a management buyout.

Foxconn plans a joint venture with **Fiat Chrysler** to make electric vehicles for the Chinese market.

Foxconn's Terry Gou vows to fire up the company's plant in Wisconsin this year.

Foxconn invested $26 million in **Nanox** to produce futurist and affordable x-ray machines.

Laritech opened a new EMS facility in Moorpark, CA.

Mycronic implemented a new group structure.

New Kinpo Group (Cal-Comp) expects many of the group's subsidiaries will go public beginning this year.

Pegatron plans to set up production facilities in South Vietnam.

Rohde & Schwarz signed a strategic partnership with **Benchmark Electronics** to improve its production capacity.

Samsung Electronics installed an **ABI BoardMaster** PCB diagnostic system.

ScanCAD named **Southwest Systems Technology** representative in Texas, Oklahoma, Arkansas and Louisiana.

SEMI is postponing Semicon China and suspending Semicon Korea in response to the coronavirus outbreak.

Wistron plans to start ramping up output, including smartphones, from its third plant in India after kicking off trial production at the plant in November 2019.

Yekani Manufacturing, a South African EMS company, is reportedly facing liquidation.

- Magnalytix: Process Control Tools (Magnalytix OE-250 SIR Testing)
- Nihon Superior: Cored Wire (TipSave N)
- Nordson Asymtek: Dispensing Equipment (Qadence)
- Nordson Dage: First Article Inspection (Prospector)
- Nordson Dage: Test & Inspection – AXI (Assure Stock Line)
- Part Analytics: Software – Management (AI Driven Spend and RFQ Management)
- Promation: Soldering – Alternative (Panda)
- Rehm Thermal Systems: Soldering – Reflow (Vision TripleX)
- Rogers Corporation: Laminates (TC350 Plus)
- Rohde & Schwarz: Test & Inspection – Functional Test (R&S NGM200)
- Saki: Software – Production (Quality Driver Software Suite)
- Viscom: Test & Inspection – AOI (3D AOI system S3088 DT)
- VJ Electronix: Component Storage (XQuik III)
- Weller Tools: Soldering – Hand Tools (Weller Active Tip Range)

The awards were presented during IPC Apex Expo in San Diego last month.

"The new products continue to impress," said Mike Buetow, editor-in-chief of CIRCUITS ASSEMBLY and PCD&F. "Judges were especially enthralled with equipment that gives manufacturers more in-house control over process consumables. – *MB*

Libra Industries Acquires Ex-Benchmark Facility in Mexico

GUAYMAS, MEXICO – Libra Industries has acquired a contract manufacturing facility here formerly run by Benchmark Electronics. Libra Guaymas will be Libra's fifth plant and first international operation.

The 52,000 sq. ft. plant previously was operated by Benchmark Electronics and makes complex assemblies and subassemblies for customers in the aerospace/defense, medical, semiconductor and industrial end-markets. Benchmark had slated the site for closure this year.

"The facility is complementary to our current operations in Ohio and Texas and will help Libra accelerate its growth strategy by providing customers with more technical capabilities," said Rod Howell, CEO of Libra. "Our goal is to provide customers with a full suite of capabilities and be a trusted partner for all of their outsourced manufacturing needs. This investment further helps us achieve that strategy."

Financial terms were not disclosed. – *CD*

Prime Technological Buys 2 EMS Firms

ATLANTA – Prime Technological Services has acquired TeligentEMS for an undisclosed sum. TeligentEMS has a plant in Havana, FL, and was founded in 2003.

The acquisition is important in expanding Atlanta-based Prime's presence in the US market, the firm says.

Separately, in February Prime also bought I. Technical Services for an undisclosed sum. Mike Thompson, president and CEO of ITS, will continue to work with Prime as a strategic advisor.

"The acquisition of TeligentEMS is a key element of our customer-driven strategy of providing the manufacturing services and geographic footprint our customers require," said CEO Greg Chesnutt. TeligentEMS is strategically located in the Southeast and represents a significant expansion of our value delivery platform for customers in targeted vertical markets.

TS offers quickturn prototype and NPI capabilities, plus testing and after-market services that will "really resonate with customers in our targeted aerospace, defense, medical, industrial and communications markets," Chesnutt added. – *MB*

ZENTECH ACQUIRES TRILOGY CIRCUITS

DALLAS, TX – Zentech Manufacturing in January acquired fellow EMS Trilogy Circuits, extending its geographic reach into the middle of the US. Following the transaction, Trilogy Circuits becomes Zentech Dallas and joins the Zentech family of companies that also includes Zentech Baltimore (MD) and Zentech Fredericksburg (VA).

Financial and other terms were not disclosed.

Trilogy Circuits is AS9100D certified and provides electronics manufacturing services and support for the defense and other high-reliability industries.

"We are extremely excited to welcome Charlie Capers and the Trilogy Circuits team to the Zentech family," said Steve Pudles, CEO, Zentech. "The transaction was driven in large part by requests from our established military customers for Zentech to deliver our highly certified, high-complexity processing model to the Southwest region, as they all have significant operations in this vibrant geography. Zentech is on the leading edge of many emerging DoD programs, and the formation of Zentech Dallas will provide seamless engineering collaboration with our customers to support their mission-critical NPI requirements."

Capers, who founded Trilogy Circuits in 2002, will continue to manage Zentech Dallas. – *CD*

CAN'T COMPUTE

Trends in the US electronics equipment market (shipments only).	% CHANGE Oct.	Nov.	Dec.	YTD%
Computers and electronics products	0.3	0.3	-0.3	3.1
Computers	1.1	1.3	-1.5	-25.0
Storage devices	28.7	22.0	-17.2	27.2
Other peripheral equipment	0.6	5.6	-7.1	6.5
Nondefense communications equipment	-0.8	-0.4	3.1	10.0
Defense communications equipment	-8.5	3.8	-1.2	-7.6
A/V equipment	2.3	-14.8	6.2	13.6
Components[1]	-0.2	3.9	0.2	4.5
Nondefense search and navigation equipment	4.8	-0.3	-2.3	1.7
Defense search and navigation equipment	0.6	2.5	-1.0	3.5
Medical, measurement and control	0.6	-2.5	0.1	-0.8

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, Feb. 4, 2020

US MANUFACTURING INDICES

	SEPT.	OCT.	NOV.	DEC.	JAN.
PMI	47.8	48.3	48.1	47.8	50.9
New orders	47.3	49.1	47.2	47.6	52.0
Production	47.3	46.2	49.1	44.8	54.3
Inventories	46.9	48.9	45.5	49.2	48.8
Customer inventories	45.5	47.8	45.0	41.1	43.8
Backlogs	45.1	44.1	43.0	43.3	45.7

Source: Institute for Supply Management, Feb. 3, 2020

KEY COMPONENTS

	AUG.	SEPT.	OCT.	NOV.	DEC.
Semiconductor equipment billings[1]	-10.5%	-5.7%	2.5%	9.1%[r]	17.8%[p]
Semiconductors[2]	-15.4%	-14.6%	-12.7%	-10.7%[r]	-5.5%[p]
PCBs[3] (North America)	1.02	1.04	1.11	1.08	1.09
Computers/electronic products[4]	5.48	5.52	5.49	5.50[r]	5.49[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

METALS INDEX

Report: 61% of Mfg. Cos. Need to Reevaluate AI Implementation

PALO ALTO, CA – While manufacturing companies see the value in implementing artificial intelligence, many are struggling to deliver clear results and are reevaluating their strategy, according to a new report commissioned by Plutoshift.

The findings revealed almost two-thirds (61%) of manufacturing companies said they need to reevaluate the way they implement AI projects.

While companies are making progress with AI initiatives, many planning and implementation struggles remain, from defining realistic outcomes, to data collection and maturity, to managing budget scope and more, according to Plutoshift.

A major reason companies are rethinking their AI implementation plans is a lack of data infrastructure needed to fully utilize AI. Eighty-four percent of respondents said their company cannot automatically and continuously act on their data intelligence.

Some 72% of manufacturing companies said it took more time than anticipated for their company to implement the technical/data collection infrastructure needed to take advantage of the benefits of AI.

Hot Takes

- **Worldwide semiconductor revenue** totaled $418.3 billion in 2019, down 11.9% from 2018. (Gartner)
- **Total capital expenditures** of Taiwan PCB factories in 2020 will exceed NT$50 billion ($1.67 billion), on demand for 5G mobile communications. (TPCA)
- **Worldwide IT spending** is projected to total $3.9 trillion in 2020, an increase of 3.4% from 2019. (Gartner)
- **Global server shipments** from Taiwanese manufacturers declined 1.4% in 2019 but will show growth of 6.6% in 2020, totaling 16.01 million units. (Digitimes Research)
- **Worldwide smartphone shipments** decreased 1.1% year-over-year to 368.8 million in the fourth quarter. (IDC)
- **Singapore's electronics factory output** edged higher from a year ago in December. (Singapore Economic Development Board)
- **The worldwide tablet market** declined 0.6% year-over-year during the fourth quarter to 43.5 million units and was down 1.5% for the year to 144 million units. (IDC)
- **Taiwan's manufacturing production index** rose 6.4% year-over-year to 118.79 in December, the highest-ever monthly mark. (Ministry of Economic Affairs)

The Coronavirus Took Industry by Surprise. Why?

Disaster planning should be part and parcel of our business toolkit.

WITH ONLY TWO months of the year behind us, it may be prudent to take any and all business plans you had and rip them up.

Entering a new year is always exciting, when embarking on interesting initiatives that will generate greater profits. Regrettably, sometimes disruptions sideline those exciting new thoughts, replaced by triage efforts that were never in your plans. This year that disruptive event is the coronavirus, and businesses are trying to work through a potentially altered global supply chain.

First and foremost, the coronavirus is just that: a virus – a highly contagious disease debilitating thousands around the world who have or will contract it. Our first thoughts must be with the victims who are infected, hoping they recover. And yes, other viruses and diseases over the years have wreaked havoc on various locations, countries and peoples. By itself, the coronavirus should not derail business planning, business plan execution, or business itself. However, sometimes "things" happen!

"Things" is often plural: a series of events that individually are relatively benign, but when they converge take a very different life. In this case, we have a global economy that has become efficient and sophisticated, so much so that manufacturing production of everything from raw materials to finished product can be sourced from anywhere in the world, transported across oceans and continents, sometimes several times, arriving at their given destination just in time to enable the next manufacturer to pull from stock and keep the pipeline going through its production process. Transportation time, queue time, and processing time appear to seamlessly flow in our global economy.

What happens if one of the links in this chain stretches, twists or breaks, however? Alternative sources usually can be inserted in a "plug-and-play" manner with little impact on the overall end-product. Yet, at times two benign "things" together can cause everyone to rethink and refocus.

When a virus, especially one as contagious and lethal as the coronavirus, begins to spread, and does so quickly, people are impacted in at least a couple ways. First, of course, is self-preservation: They do not want to catch the disease. Second, they, or their management, or government, etc., may react in a way that causes a widespread exodus. If and when these actions occur, manufacturing plants don't operate, materials are not made, and the global supply chain slows, has shortages, and may out-and-out stop functioning.

So back to "things." The coronavirus struck in a huge country with vast manufacturing capacity that supplies companies in virtually all industries globally. It struck fast, just before a major and long holiday, which accelerated the annual exodus of workers returning home. And those workers do not want to return to factories until the all-clear sign is raised, and they are comfortable their health is not at risk. In short, ground zero for the virus is also ground zero for the supply chain, and the consequences have rippled the world over.

The disruption to the supply chain moves the best plans to be implemented this year to the backburner, as the priority becomes the flow of supplies. No one knows how long interruptions may last. No one knows if this is going to be a blip on a chart or cause serious supply shortages for several quarters. These are the times when having a solid plan "B" (or "C", "D") is worth its weight in gold.

That may be the most important takeaway: the need for a backup plan that can be pulled out at moment's notice to guide your company through the rough or uncharted waters brought about by a global disruption. I am rethinking inventory levels, staff safety, travel, and reviewing where my supply chain is – where do the things I need come from – so I can better develop a workable plan B. At the same time, I am redoubling efforts to communicate with key suppliers to reduce the potential for unpleasant surprises if events deteriorate further. Taking for granted the situation is normal may be riskier than this or any virus.

The coronavirus outbreak could also be a wake-up call for other strategic planning areas. Benign "things" such as tariffs, trade agreements, and a record-long bull market – events out of our personal control – could individually or collectively become the "things" that disrupt our businesses and cause a major change in plans. Being better prepared for the unforeseen must be a higher priority, as our industry, and industry in general, coexists with supply chains that rely on mutual support and available options.

Hopefully the drama of the moment will not morph into something worse. Very hopefully the coronavirus will impact fewer people than feared and fade away more quickly than predicted. In the wake of such events, however, thinking and rethinking how to navigate such disruptive global "things" should become a priority for us all. ❑

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Contrary Routing Schemes

Why you should be mindful of long parallel routing situations.

IT WAS A warm Saturday morning last August when we decided to visit my favorite Swedish flatpack furniture store. We, of course, means me tagging along with my spouse as she chose some stuff to seal the back-to-school deals. (One more year!) We weren't the only ones with that plan, so it was fortunate I knew the parking lot well.

For the uninitiated, the store layout – including the garage – is a giant maze of hallways. You pass by little rooms of staged furniture on the top floor, then another habitrail running past an assortment of sundry household items on the floor between that one and the parking level. It is supposed to be a treasure hunt, with cheap, bland food at either end.

All along these meandering paths, little projectors built into the ceiling provide arrow-shaped beams showing which way to go so you don't get disoriented. Lines of yellow tape extend for miles. The tour would probably take about 20 minutes if you weren't shopping. Walking the crowded habitrail with a shopping cart is easier when everyone is going the same direction. One problem: those renegade shoppers who decide to backtrack. That messes up the flow.

When it comes to printed circuit board design, we are often faced with a few renegade shoppers. Once a board has all the components placed, a tool called rat's nest shows a line between all the open connections. From the start, all of them are open, and routing is the secret sauce that solves the puzzle. A renegade connection runs counter to the main bias of the design.

Starting at the brains of the operation, it could be a common microcontroller or perhaps a silicon monster with two dozen graphical processor cores. Either way, all the component locations are chosen based on the best way to communicate with the mothership. Rivers of connections stand out as dense collections of lines going more or less to the same place. We know what to do with those. If you're wondering, route them side-by-side and clear up the crossovers by thoughtful fan-out. The idea is to use the layer pair to untangle the data bus. There is usually more latitude to cross over near the secondary device or somewhere in between. A lot of data are in the confusion of an unrouted PCB. Routing that SDRAM (**FIGURE 2**) on two layers, including the series resistors, looked impossible until a few hours later.

Always present the best I/O by routing away from "the chip." Let that be the factor that drives component placement. Once all that is done, it looks like a simple and apparent solution. More likely, an elegant board like that took a great deal of effort.

Where to start? Back to the bare board with rivers of data or smaller collections of traces that seem to go everywhere. Start with the foundational connections that require the most attention. Clocks, differential pairs, any other high bit rate or high-frequency routing set the tone for the general direction of the circuit flow on a by-layer basis. By using the term "general direction," I hope to steer you toward a conclusion of your own.

You've got it, right? A primarily horizontal layer can change its stripes and become a vertical channel out near the perimeter. If components near the edges

FIGURE 1. The habitrail. Hamsters were using vias before vias were cool! (Source: Living World)

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tend to use the outer layer to establish a more inboard via location, it becomes possible to skirt past the river of PCIe.

Typically, some long connections go from one corner of the board to the other. That diagonal passes right through the chip! Face it. If that connection is important in terms of length, we would have to rethink the placement.

It's a thing to route, no other rules. From the start, that trace and its cousins go around the edges. If you were going renegade and routing on a ground plane layer, near the board-edge might be the one safe space place.

One by one, every trace that passes through the gnarly core gets detoured around the hot spot in the rat's nest. Bit by bit, it starts to become a little more transparent as a web. It becomes manageable, and the challenge becomes incorporating improvements as they materialize.

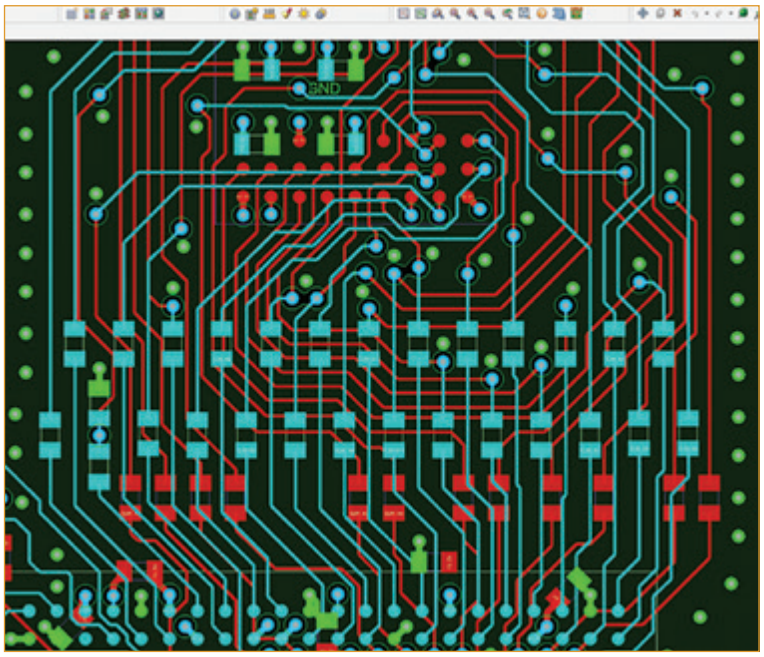

FIGURE 2. Sorting after the fan-out.

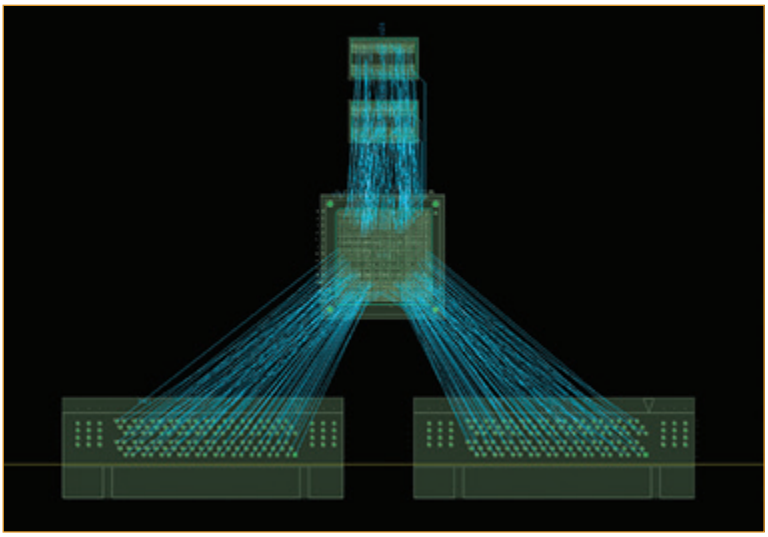

FIGURE 3. We don't even place the unimportant stuff until this stuff is routed and tuned. (Source: Embedded)

Evasive tactics. Up, down, left, right; there may only be one direction left for the last GPIO. It is unlikely to be the right direction, but we'll use any port in a storm. A popular plan among our EE patrons is to send an I2C bus to all the main chips on the layout. They get to send an all-is-well report back to the brain. "Route this last," they say.

Things like a common JTAG bus for functional testing are hard to do wrong in terms of wrecking test results. The risk is routing will cause some effect that wasn't considered by the SI/PI simulation teams. Clever placement may allow most of those connections to remain on the top or bottom layers from end to end. Components may creep and most likely will have to be moved more than once, as the routing demands.

The final 100 (or 1). In conclusion, the edges within the Faraday cage of ground vias present some off-axis opportunities to go around the outside and come back in at the correct routing channel. As PCB aspect ratios favor long skinny boards, we can save precious space in the dense areas by finding an escape route wherever that layer takes you. This can end up saving a layer pair, so don't knock it until you master it. The rogue shoppers are going to make it difficult as they cut across the aisle, so a little defensive routing is in order.

The last 100 "unimportant" traces can be disruptive to power and ground planes if the traces hopscotch from layer to layer through vias. As all the previously routed critical nets are being digested by the team, we must tread lightly, even when "this one doesn't matter." Components placed a long distance from the center have a chance of being related to a connector or antenna where important things are happening. Be mindful of long parallel routing situations. Like when you get to the check-out and there are 26 very long lines to choose from. You'll get to know your neighbors as you shuffle along. We don't want our traces getting too friendly. Open another lane. □

The New Printed Circuit Engineering Association

IN THIS MONTH'S column, we'll take a first look at the new Printed Circuit Engineering Association (PCEA), including an overview of membership and why we established the organization. We'll also look at the mission of PCEA, and how it will unfold to the industry.

Membership. PCEA is an international network of engineers, designers, and specialists related to printed circuit development. We are a mixed group of individuals that covers the entire product development cycle. There are no limitations or restrictions as to who can become a member. Membership is free and open to all those interested in gaining and sharing their knowledge with others. We will serve the industry as a nonprofit organization.

Why we established PCEA. Several well-organized groups cater to the electronics industry. These organizations tend to feature a specific segment of this industry by hosting highly focused, major conferences for their followers. These conferences tend to be one or two times a year at different locations.

Each of these conferences specifically focuses on a skill segment, such as design, assembly, manufacturing, etc. With technology changing at a rapid pace, it becomes very difficult and expensive for professionals to attend the plethora of major conferences conducted in the course of a year.

In an attempt to address the changing demands, some organizations, in addition to major conferences, have set up local chapters to address our rapidly changing industry. They have found it difficult to fully address the needs of each industry discipline required to produce a workable PCB product. The main theme was to understand each other's challenges and how to assist each other. Unfortunately, printed circuit engineers were often not understood by other industry segments and these organizations.

Printed circuit engineers are technologists who must understand the needs and requirements of all the disciplines that build the final product. They must have a comprehensive understanding of electrical engineering, design, mechanical engineering, printed board materials, fabrication/assembly processes and limitations, quality assurance testing, and fully populated test requirements at all levels of the product development process. In addition to these disciplines, printed circuit engineers must have an understanding of compliance and field service requirements of each product. PCEA is structured to meet the challenges we face today and take on the challenges that are coming for printed circuit engineers.

The PCEA's mission. PCEA's mission is to promote printed circuit engineering as a profession and encourage, facilitate, and promote the exchange of information with the integration of new design concepts through communication, education, seminars, workshops, and professional certification through a network of local, regional, and international PCEA-affiliated consortiums. We're seeking to provide a constructive, professional environment working with all other industry organizations.

Since our inception, we have achieved great industry acceptance. We have received endorsements from professionals across the electronics industry. In the coming months, we will expand the number of affiliates, while realizing steady growth of our membership. If you're interested in joining or starting an affiliated consortium in your area, feel free to participate and join the many professionals who are the backbone of our industry. Join us by visiting our website (pce-a.org) and contacting us for more information.

Action items. Here are our first quarter 2020 action items:

1. Continue to develop our website.
2. Elect an executive board to care for the oversight of the association.
3. Expand the content of our current communication vehicles.
4. Assist in the formation of new, regional affiliate groups.
5. Establish a working relationship with other associations, such as IPC, SMTA and IEEE.

Professional Development and Events

Here are some upcoming industry events to look out for in 2020. I hope you have the opportunity to attend one or more.

- Apr. 7-8: CDN Live (Silicon Valley)
- Apr. 27-30: Zuken Innovation World Americas 2020 (Coronado, CA)
- Jun. 9-10: PCB2Day – SMT Assembly Boot Camp (Austin, TX)
- Jun. 9-10: PCB2Day – Design Essentials for PCB Engineers (Austin, TX)
- Jun. 22-25: Realize LIVE 2020 (Las Vegas)
- Sept. 8-11: PCB West (Santa Clara, CA) □

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PCB2DAY
Bringing two-day workshops on design and assembly to you!
AUSTIN, TX
June 9-10, 2020
SMT Assembly Boot Camp
PHIL ZARROW
AUSTIN, TX
June 11-12, 2020
Sponsored by:
EMA Design Automation
Design Essentials for PCB Engineers
SUSY WEBB
Early bird specials! Register now!
PCB2DAY.COM

AUSTIN, TX

June 9-10, 2020

SMT Assembly Boot Camp, PHIL ZARROW

This SMT electronics assembly class is a practical overview of the many different processes and materials used in through-hole and surface mount technologies (SMT). It is a focused, two-day long class, which provides students with the opportunity to learn and understand the processes, tools, and materials used in today's manufacture of electronic assemblies.

The course combines lecture, videos and discussion and is intended for those that are new to electronics assembly and want to come up to speed on the processes, materials, equipment and procedures.

AUSTIN, TX

June 11-12, 2020

Design Essentials for PCB Engineers, SUSY WEBB

Engineers designing their own boards will need to understand and use the same science that seasoned PCB designers have built up over many years. For example, the way parts are built, or a board is designed can make a huge impact on the ease of fabrication and assembly, just by the practices put into place while working. Those practices can increase yields and lower the cost for all, and this two-day workshop starts with thoughts about that. There are many ways to place parts on a board, but some work much better than others for the physics, electrical and mechanical purposes. We will discuss the order of placing parts, setting up routing, and placement ideas that will lead to better flow.

On Day 2, fine-pitch BGAs will be examined. Their size and pitch make them increasingly challenging to work with, as do the signal integrity and EMI issues that come along with them. We will look at through-hole and HDI examples for fanout, grid and routing information, and their specific manufacturing needs. In the last section we will delve more into the science of how everything works together by discussing the electronics and physics, controlling impedance and high-frequency energy, and stack-up and power issues. There will be examples of how a signal's field energy actually flows through layers of the board, and steps to take when routing signals through the board. The workshop will conclude with a brief discussion of autorouting vs. hand routing.

Preparing for Next-Gen Loss Requirements, Part 3

The relative permittivity for FR-4 is just that: relative.

Ed.: This is Part 3 of a three-part series on preparing for next-generation loss requirements.

LAST MONTH, IN Part 2 of this series, I outlined the means by which insertion-loss requirements are determined. Here, I'll suggest a better method for obtaining accurate Df numbers without having to go to the trouble of building test boards.

A longtime PCB industry technologist asked me recently, "What's a good Dk (dielectric constant) number for FR-4?" As the interest in signal integrity (SI) was growing roughly 25 years ago, it started to interest me that many SI practitioners considered FR-4 to have monolithic properties. The question reinforced that some still hold that view. One might say the relative permittivity (ϵ_r) of FR-4 is 4.3. Someone else would say 4.1. A third says they always use 4.0. As I read up on it, I realized it varies with frequency, resin content (as a percentage, with the inverse being the glass percentage), and the resin system. At lower frequencies, static numbers for vanilla FR-4 were probably fine for impedance calculations and signal integrity, but those days are far behind us at this point.

Looking at the hundreds of materials in the Z-planner software library, there's a clear relationship between Df and Dk values. **FIGURE 1** summarizes this relationship, along with the bullet list below:

- "High-loss" materials – typically defined as materials with dissipation factors (Dfs) greater than 0.020 – have Dks greater than 4.0.
- "Standard-loss" materials, with Dfs between 0.015 and 0.020, typically have Dks greater than 4.0, with some standard-loss materials in the 3.75-4.0 range.
- "Mid-loss" materials, with Dfs between 0.010 to 0.015, follow a similar pattern to standard-loss laminates for Df and Dk.
- "Low-loss" materials, with Dfs between 0.005 to 0.010, typically have Dks between 3.5 and 4.0.
- "Ultra-low-loss" materials, with Dfs below 0.005, typically have Dks between 3.0 and 3.5.

So far, so good, but this is where the discussion gets interesting. I wrote a good bit about this, as published in this space between December 2018 and February 2019, so I'll try to avoid duplication. As I'm unpacking from a pair of trade shows last month, I'm recalling a discussion with a laminate manufacturer that mentioned they use four different fixtures to measure Dk and Df up to 20GHz.

The values represented above come from eight different manufacturers, using a smattering of 12 different IPC test methods measuring Dk and Df. As a result, there's no way to correlate Dk and Df values directly across the different laminate vendors that use different test methods.

To make matters even more confusing, laminate manufacturers may use:

- One test method for datasheets and another for Dk/Df tables.
- One test method at 1GHz and another test method above 1GHz.
- One test method for Dk and another test method for Df.

PCB fabricators typically use their own Dk fudge factors, based on actual circuit boards, in which they attempt to remove copper effects in order to backwards-engineer Dk and Df values. And multi-gigabit Serdes signals will often be planned using Dk values at 1GHz. And we haven't even discussed temperature impacts or that half the Dk values from laminate manufacturers are in the x-y plane, which a signal will never see!

In this environment, Dr. Eric Bogatin introduced me to Dr. Don DeGroot of CCN Labs, and through meetings across multiple industry conferences we found we share an interest in developing what we called an "apples-to-apples" dielectric-characterization methodology that basically took the best practices from the most common IPC test methods for dielectric characterization, combined with a commercial stackup-design solution.

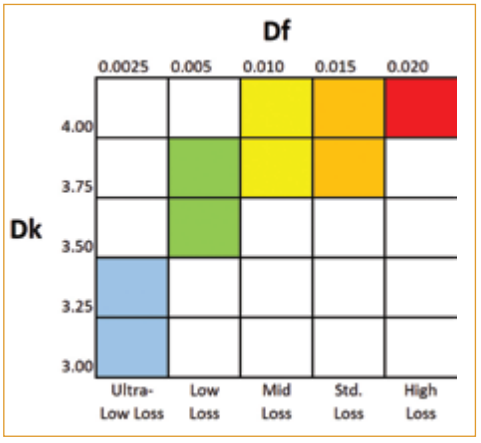

FIGURE 1. Summary of the Dk and Df relationships across hundreds of laminates in Z-zero's Z-planner software library.

Measurement comparisons. As part of our journey toward the "ideal" dielectric-measurement system, our goal was to gain

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insight into how closely *published* copper-clad laminate (CCL) manufacturers' table values for Dk(f) and Df(f) correlated to our *calibrated measurements* of the dielectric's Dk and Df from 1 to 20GHz. What we found was that within specific CCL manufacturers, published Dks varied by +/-10% from our measurements – a 20% variation from minimum to maximum. For signal-integrity purposes, it would be advantageous to remove this additional source of uncertainty, both during new product introduction (NPI)/prototyping activities and in volume production.

Dk and impedance. To provide an idea of the impedance implications associated with accurate Dk values, consider a symmetrical differential stripline model with 5-mil thick dielectrics and 5-mil wide traces.

Published: Incorporating a *published* Dk of 3.74 produces a 50.8Ω simulated single-ended impedance and a 97.2Ω differential impedance on 12-mil spacing.

Measured: Using the *measured* Dk value at 10GHz for a laminate in our study, the simulated single-ended stripline impedance result was 48.5Ω, with a 92.8Ω differential impedance.

Depending on frequency and other factors, the design may be able to survive a 4.5Ω differential impedance gap, but this difference will be in addition to other tolerances and manufacturing variations you must account for, which can pose problems if all the variance works in the same impedance direction. And impedance mismatches – assuming you were targeting 100Ω differentially – cause rise-time degradation that contributes to eye closure, as discussed last month. SI simulations based on the questionable Dk values will be inaccurate. My view is giving away this accuracy when it's so easily avoidable is not good design practice.

Df and insertion loss. One of the more significant findings in our research is the degree to which *published* Df values tend to diverge from our calibrated stripline-resonator results. These differences vary in magnitude, but always in the same direction: Our *calibrated* stripline-resonator measurements were always higher than vendor-published values. The Df differences were particularly striking at 1GHz, ranging from 33% for one material to 200% for another common material.

To get an idea of the propagation-loss implications for underestimating Df, consider the same stripline configuration noted above, assuming copper foil with R_z=2µm roughness on the laminate and processing on the prepreg side that results in R_z=1.5µm.

Published: Incorporating a *published* Df of 0.006 produced an insertion loss of 0.72dB/in at 10GHz.

Measured: Using the *measured* Df value of 0.010 at 10GHz for a laminate in our study resulted in an insertion loss of 0.88dB/in at 10GHz, as shown in **FIGURE 2**.

Multiply these values by a 10" interconnect length and we're talking about a 1.6dB difference. That's not a long signal path, and the unplanned loss delta is enough to cause headaches, especially for longer run lengths. There's a cost element as well. In this example, you paid for 0.006 and received 0.010. That's a *caveat emptor* moment. The only foolproof way for engineers or PCB fabricators to know they're getting the loss performance they're paying for is to measure dissipation factors at frequencies of interest on their own test benches and in the production environment.

Parting thoughts. As engineers and PCB designers are preparing to implement next-generation technologies, we no longer have reason to employ multiple dielectric-characterization methods or fixtures when moving from one frequency to another, to use different methods for Dk and Df, using in-plane measure-

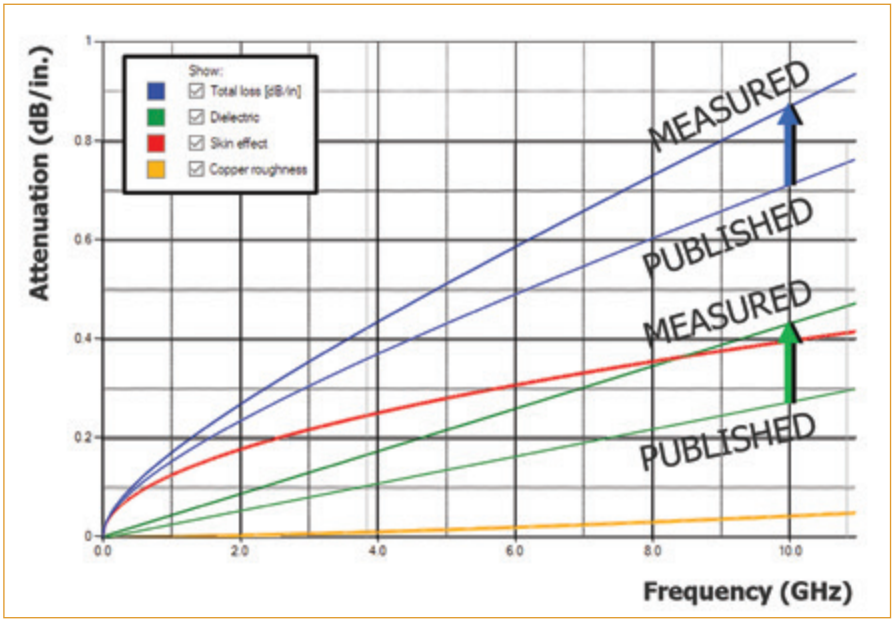

FIGURE 2. Published vs. measured Df values, shown in the form of two different dielectric-loss curves (green), as well as different total-loss curves (blue). Simulated in Z-zero Z-solver using the HyperLynx field solver.

TABLE 1. Low- and Ultra-Low Loss Laminate Measurements

Material	Dk(1GHz)	Dk(10GHz)	Dk(20GHz)	Df(1GHz)	Df(10GHz)	Df(20GHz)
A	3.12	3.11	3.10	0.003	0.003	0.003
B	3.51	3.46	3.46	0.006	0.007	0.007
C	3.53	3.51	3.50	0.007	0.008	0.008
D	3.77	3.74	3.72	0.007	0.007	0.007

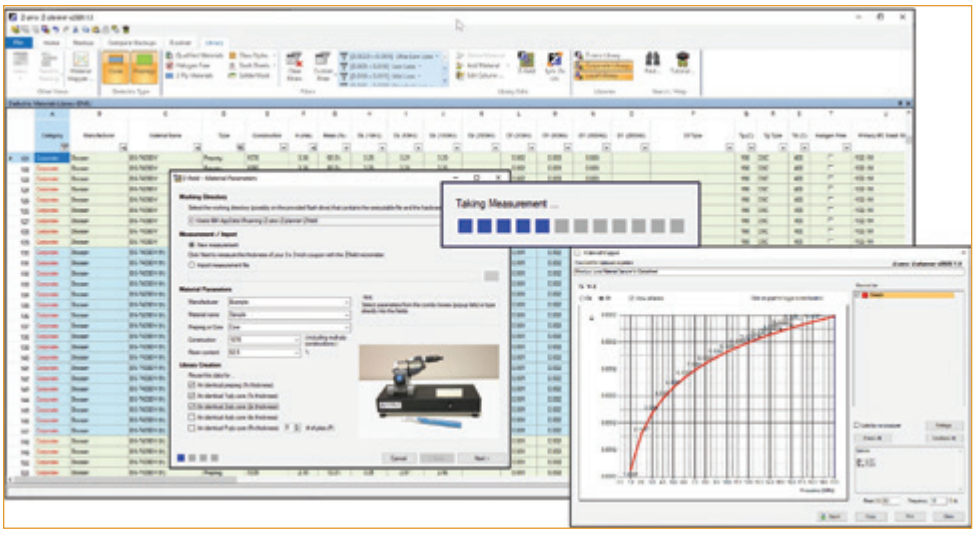

FIGURE 3. Z-field tests Dk and Df from 1 to 20GHz. Output formats include Excel and the Z-planner stackup-planning software library, shown above.

ments that a signal will never see, or using different test setups among laminate manufacturers, PCB fabricators and OEMs.

At DesignCon, we unveiled the first set of low- and ultra-low loss laminate measurements from this system, called "Z-field," shown in **TABLE 1**. The system itself, a combination of hardware and software, is shown in **FIGURE 3**. Results should be similar to what would be expected from a well-calibrated Bereskin Stripline system (now IPC-TM-650, no. 2.5.36), while obviating the need for IPC-TM-650, no. 2.5.5.5, 2.5.5.9 and 2.5.5.13. Game-changing! □

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Conference & Exhibition

Connecting Design to Fab to Assembly

Conference: September 8 - 11
Exhibition: Wednesday, September 9

WHO'S EXHIBITING

Accurate Circuit Engineering
Aculon, Inc.
Advanced Assembly
Advanced Circuits
AGC Chemicals Americas, Inc.
AGC Nelco America Inc.
All Flex Flexible Circuits & Heaters
Altium, Inc.
American Standard Circuits, Inc.
APCT
Arlon EMD Specialty
Bay Area Circuits, Inc.
Beta LAYOUT
Bittele Electronics Inc.
Bowman XRF
Cadence Design Systems
Cicor Group
Clear Blue Engineering
dalTools
Dino-Lite Scopes (Big C)
DownStream Technologies, Inc.
DuPont
DYCONEX AG
Dynamic Electronics Co., Ltd.
Elgris Technologies, Inc.
Elsyca
EMA Design Automation
EM Solutions Inc.
Firan Technology Group - FTG
Fischer Technology, Inc.
Flex Interconnect Technologies
Flexible Circuit Technologies
Freedom CAD Services, Inc.
Fujipoly America
Goal Searchers Co., LTD Zhuhai
Green Circuits
GS Swiss PCB AG
GTS Flexible Materials Ltd.
HIE Display Limited
HSIO/Ironwood
ICAPE Group
Imagineering, Inc.
Insulectro/Isola
Integrated Technology Ltd. (ITL Circuits)
IPC-2581 Consortium
JetPCB USA
JS Electronic Co. Ltd.
Kinwong Electronic Co., Ltd.
Krypton Solutions
Kyocera International, Inc.
Leader Tech, Inc.
LPKF Laser & Electronics
Medcadtron GmbH
Mentor, A Siemens Business
MicroConnex
Minco Products, Inc.
Multek Technologies, Inc.
MV Circuit Technology Co., Ltd.
MVINIX Corporation
NTS
Oak-Mitsui Technologies LLC
Ohmega Technologies, Inc.
Oki Printed Circuits Co., Inc.
Optiprint AG
Panasonic Electronic Materials
PCB Power Inc.
PFC Flexible Circuits Limited
Polar Instruments, Inc.
Polyonics
Printed Circuits
Pulsonix PCB Design Software
Quadcept
RelianceCM
Risho
Rogers Corporation
Royal Circuits
San Diego PCB Design
San-ei Kagaku Co., Ltd.
Sanmina Corporation
Screaming Circuits
SEP Co., Ltd.
Shenzhen Danyu Electronics Co. Ltd.
Shenzhen JDB Technology Co., Ltd.
Shin Yi PCB Co., Ltd.
Sierra Circuits, Inc.
Slingshot Assembly
Somacis Inc.
Summit Interconnect
Sunshine Global Circuits
Sunstone Circuits
SVTronics, Inc.
Tempo Automation
Ticer Technologies
Ultra Librarian
Varioprint AG
Vayo Technology
Ventec International Group
Victory Giant Technology (Huizhou) Co., Ltd.
VYCOM Global Sources Ltd.
Xiamen Bolion Tech. Co., Ltd.
Zuken USA Inc.

Does Differential Signaling Require a DIFFERENTIAL IMPEDANCE?

Or does it distract from the actual need of the signaling protocol? **by LEE RITCHEY**

Much engineering time is spent on designing differential signaling circuits to maintain a differential impedance between the two sides of the differential pair. A similar amount of time is spent measuring the final PCBs to ensure the differential impedance specification is met. The most common differential impedance target is 100Ω. A fair question is whether this impedance requirement is necessary. Once differential signaling is understood, it will be seen as unnecessary and distracting from the actual need of the signaling protocol. This article will clear up this confusion.

FIGURE 1 is a schematic of the original emitter-coupled logic (ECL) differential pair as used in early computer rooms to move ECL signals from one large gray box to another. It was not possible to ensure the ground connections between boxes were of enough quality to permit single-ended ECL signals to function properly. Differential signaling compensated for this ground offset as follows:

In Box A, the single-ended logic signal A is converted into two identical but mirror image signals, A and A-. These two signals have two things in common. They are mirror images of each other, and they are tightly timed to each other. **That is all they have in common.** The designer's goal is to ensure these two signals (A and A-) arrive at the two transistor bases in Box B with maximum fidelity. This is achieved by sending each on its own 50Ω single-ended transmission line with a parallel termination in Box B to V_{tt}, the termination voltage. Neither signal knows the other exists. They are two independent single-ended logic signals.

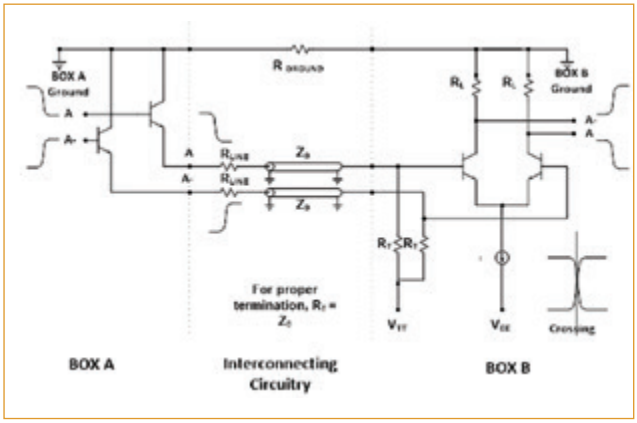

FIGURE 1. Typical ECL differential pair circuit.

All the action takes place in Box B. The two transistors in Box B are called an emitter-coupled pair or current switch. Sometimes they are mistakenly called a differential pair. Their job is to switch the current, I, up one side or the other depending on the logic state being sent. It is necessary to ensure the voltage difference applied to the bases of the two transistors is sufficient to guarantee all the current is going up only one side of the pair. This is where the name differential comes from, not differential impedance – **difference voltage**. In ECL the difference voltage to achieve proper operation is about 15mV. The smallest signal sent from the driver in Box A is about 1000mV, permitting significant signal loss in the path.

However, the original reason for inserting a differential pair in the signal path is to compensate for ground offsets between Box A and Box B. This is achieved by placing a current source in the emitters of the emitter coupled pair. The collectors of the two transistors are also current sources. As a result of this, the emitter coupled pair is free to float up and down with ground shifts between the two ends of the signal path. For ECL, this shift can be as much as 1.5V.

How does a differential pair detect a logic state change? This is a good question. When the current changes sides between the two transistors in the emitter-coupled pair, a logic state change has taken place. This occurs when the two signals cross each other as they change levels. This means the receiver is a crossing detector. Therefore, the designer's goal is to preserve the crossing. How does one do this? Ensure the two paths are the same electrical length. This is all that is required for successful differential signaling to operate.

From the above discussion it can be seen the differential impedance plays no role in successful operation of the differential pair.

FIGURE 2 is a simplified schematic of a low-voltage differential signaling (LVDS) differential pair. Notice the current switch in the right-hand side, just as there is with the ECL differential pair. Notice current flows into V_{ref} from one side of the pair, and the same magnitude current flows out of V_{ref} into the other side. As a result, during normal operation, the connection to V_{ref} is not necessary and is omitted. This results in two 50Ω terminating resistors in a series. Often, money is saved by replacing them with a single 100Ω resistor. This is likely the reason it is assumed a 100Ω differential impedance is required. Provided the two signals cross exactly in the middle as shown in Figure 1, there is no need for this connection. However, at very high data rates, if this connection is missing and the signals do not cross exactly in the middle, for a moment there will be a need for current to flow into or out of V_{ref}. If the connection is missing, the edges are degraded, sometimes enough to cause failure.

At high data rates, if the V_{ref} connection to the terminating resistors is missing, the signals will be degraded. In all modern high data rate differential signaling protocols, two 50Ω terminations are built into the receiver, and each is connected to "AC" ground in the receiver.

What about application notes that require "guard or ground vias?"

Some application notes require placing the two vias used to change layers for a differential pair close to each other and placing a "ground" via on each side of this pair. The reason given is the return currents have a path to change the planes on which they run. This sounds a bit arbitrary in the face of how a differential pair operates as described above, and it is. This is a solution to an imagined problem.

Recalling that each member of a differential pair is independent of the other, the first thing to note is they do not need to be routed side by side. The second is they are single-ended signals, just like all the other single-ended signals in a design. It is not necessary to put a "ground" via next to the layer-changing vias on single-ended nets. This is a fictitious rule that was made up by someone who did not do a proper job of analyzing the problem.

A Curious Observation

Many manufacturers of ICs that contain very high data rate differential pairs or SERDES (serializers/deserializers) have displays at design shows where the circuits demonstrated are connected with many single-ended 50Ω coaxial cables. These coaxial cables are isolated from each other, so there is no potential for a 100Ω differential impedance, and the circuits perform perfectly. These same manufacturers will publish application notes demanding a 100Ω differential impedance and tight coupling be maintained in a PCB. That the demonstration functions properly with single-ended 50Ω cabling validates the above explanation that differential impedance is not necessary, and designers should not spend time trying to achieve it.

Conclusion

Differential signaling does not rely on a differential impedance. Each of the two sides of the differential pair is a single-ended logic signal, like all other single-ended logic signals in a design. It is not necessary to route them side by side, although it is convenient to do so to keep track of them. In almost all cases, two 50Ω single-ended transmission lines of the same electrical length are all that is needed. If it is necessary to do so, the two members of a differential pair could be routed on different signal layers. □

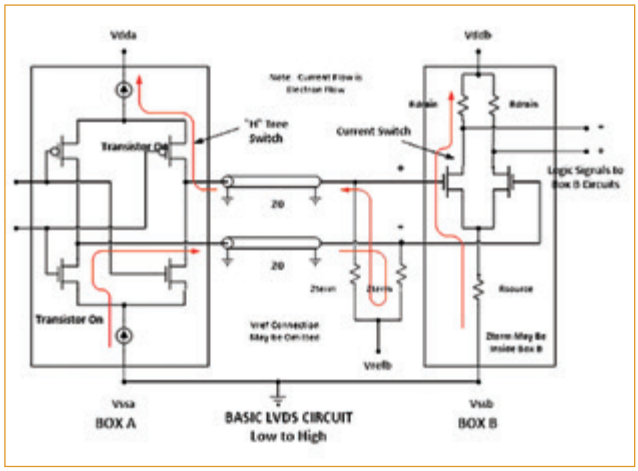

FIGURE 2. LVDS differential pair circuit.

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Is TIGHT OR LOOSE COUPLING Best for Differential Signaling?

Or should we just isolate noisy signals? **by LEE RITCHEY**

There are several theories about whether a differential pair should be routed with tight coupling or loose coupling. There must be some science that can be drawn on to arrive at a rule set that makes best use of layout time, while optimizing the signal integrity of a differential pair. This article explores the advantages of tight and loose coupling.

A known industry speaker says, "Everybody knows tight coupling is best for differential signaling." This is stated in a tone of voice that implies those who don't know this might be lacking. I sometimes say I am from Missouri, which is the "Show-Me State." If the need for tight coupling is true, perhaps there is some proof. I am still waiting to see it. The following discussion will look at a tightly coupled differential pair and the same pair loosely coupled.

The left side of **FIGURE 1** is a 3.25Gb/s differential pair routed with the classic 5-mil line, 5-mil space rule set, and the right side is that same differential pair loosely coupled. Clearly, the tightly coupled differential pair eye diagram is not as good as the loosely coupled differential pair. What happened to the tightly coupled pair is that to achieve 50Ω on each of the two transmission lines (100Ω differential, for those who think this is important), they had to be made narrower than those in the loosely coupled pair and spacing set as 5 mils vs. 10 mils. The primary source of degradation on the left side is skin effect loss due to traces half as wide as the traces on the right.

A good question is why did the traces have to be narrowed in the tightly coupled case? When any metallic object, whether another trace or a plane fill, gets near a transmission line, its impedance is driven down due to the added capacitance to the fill or nearby trace. To get back to 50Ω, the trace must be narrowed to return to the original impedance.

Often, the loss shown in Figure 1 does not concern a designer because the frequency is low enough that loss does

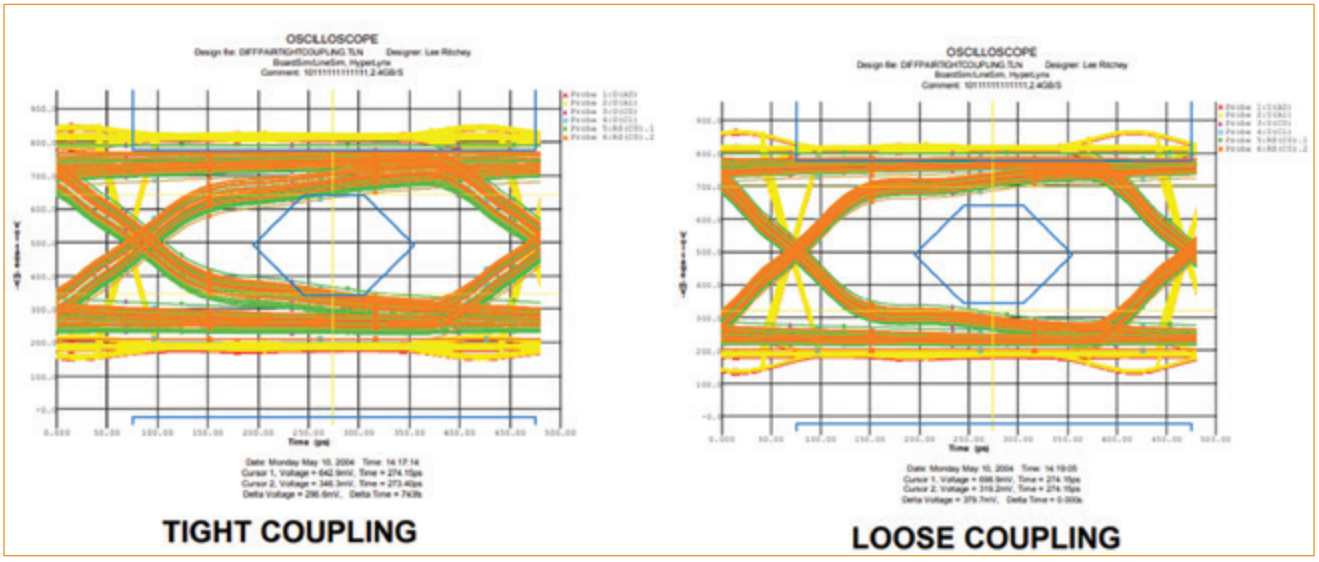

FIGURE 1. Tightly coupled and loosely coupled 3.125Gb/s differential pair.

not matter. Another concern may matter, however. If tight coupling is chosen, a potential problem can arise. Should it be necessary to separate the traces to route the signals through a pin field where they must be separated, after separation the traces no longer interact with each other and their individual impedances jump up to 70Ω. This is an unacceptably large change. Therefore, make sure all the signals can be routed without any separation. This is rarely possible. **FIGURE 3** illustrates the routing cases for the two examples in Figure 1.

Most modern designs have component pin densities that make it difficult, if not impossible, to maintain tight spacing over the entire length of differential pair paths. For this reason, it is advisable to create a routing rule (separation) that ensures the problem shown in Figure 3 does not occur. **FIGURE 4** illustrates how the impedance of a transmission line decreases as another transmission line gets closer.

Across the bottom of Figure 4 is spacing to neighboring trace with 2 mils (51µm) on the left and 28 mils (710µm) on the right. The vertical axis is impedance, with 50Ω at the top and 40Ω at the bottom. This plot is for an off-center stripline with the height above the nearest plane 5 mils (127µm). Notice that at a separation of 10 mils (254µm) the impedance has dropped to 49Ω. If that decrease in impedance is acceptable, the spacing rule for routing has been established analytically, not by some rule of thumb such as the 2H.

FIGURE 2. Tight vs. loose coupled transmission lines.

"Side-by-side routing of a differential pair does not result in common mode noise coupling from an offending signal."

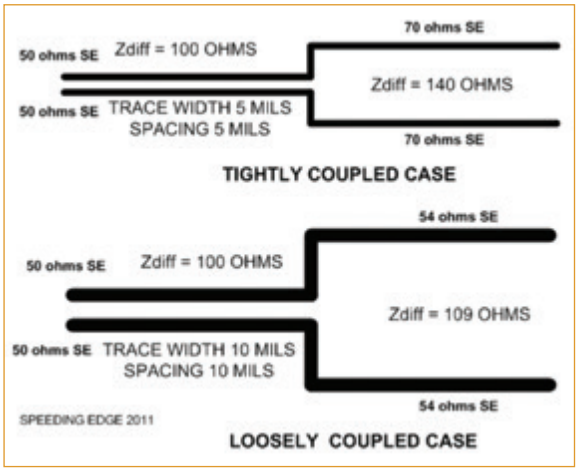

FIGURE 3. Routing tight vs. loose coupled traces.

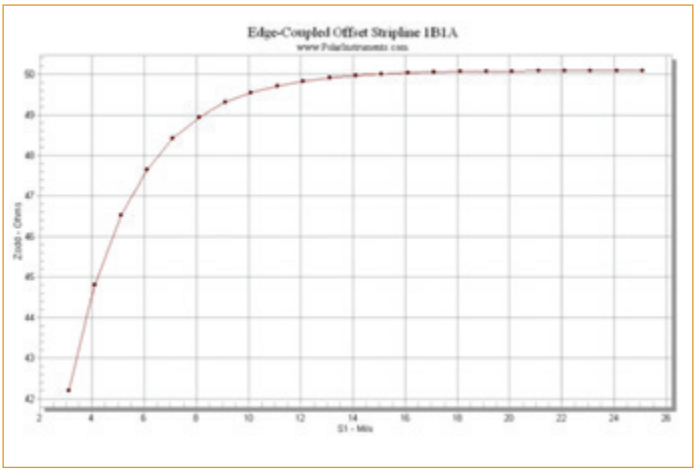

FIGURE 4. Impedance of transmission line as second line gets closer.

Common Mode Noise

Claims have been made that common mode noise coupling is reduced by tightly spacing the members of a differential pair. It would be good to understand what common mode noise coupling is before exploring this topic. To have common mode noise on a differential pair, the noise source (usually a nearby trace) must induce the same amount of noise into each member of the pair. This requires the field strength of the noise from the source be the same for both wires of the pair.

FIGURE 5 is a plot of crosstalk in an off-center stripline layer as a function of height above the nearest plane and edge-to-edge separation. Notice as a victim trace moves away from the inducing trace, the magnitude of the crosstalk gets smaller. FIGURE 6 shows the two possible methods proposed for routing a differential pair: broadside at the top and coplanar at the bottom. In neither case is there common mode noise coupling. The reason is the magnitude of the offending signal diminishes as the location of the victim signal moves farther away, as shown in Figure 5.

The best rule for routing a differential pair is to ensure any offending signal that could cause excessive crosstalk is kept far enough away from either member of the differential pair, so noise targets are met.

Conclusion

Tight coupling of differential pairs has few, if any, benefits. The best routing rule for differential pairs is a "not closer than" rule. This ensures there will never be a situation where needing to separate the members of a pair results in an unacceptable impedance change. This same principal applies to single-ended signals on a design as well. □

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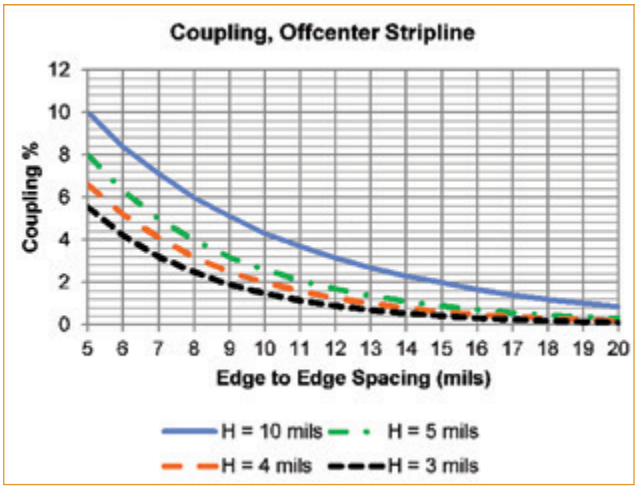


FIGURE 5. Crosstalk vs. height above plane and edge-to-edge separation.

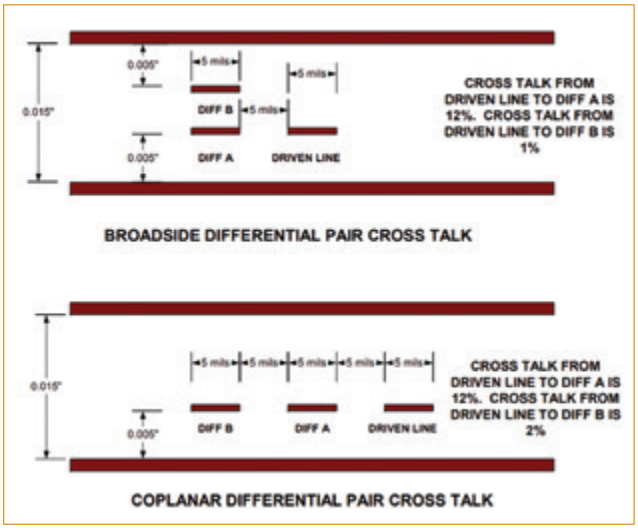


FIGURE 6. Noise coupled into two sides of a stripling differential pair.

The Show Must Go On

In the wake of pandemics and travel bans, visitors still turned out for the annual exhibition. **by MIKE BUETOW**

Heading into IPC Apex Expo the first week of February, I wasn't sure what to expect. The overall market appears to be slowing somewhat. Many EMS companies have reported lower sales for the past quarter. US presidential elections often seem to dampen electronics orders, at least until November, even though a review of the overall GDP disputes any such letup. And fears of the coronavirus in China have clearly spooked the industry, as some firms have reduced or banned employee travel for the time being.

But once the show started, many of those concerns abated. Floor traffic was up and down through the first two days, before grinding to a near halt per usual on the third and final day of the show. Exhibitors took note, reporting mixed reviews of the attendance. But when it was busy, it was really busy. It's hard to say whether the postponement of overseas shows such as Nepcon China and the International Electronic Circuits (Shanghai) Exhibition (better known as the CPCA Show) boosted attendance an ocean away in San Diego, but it probably didn't hurt. (As of this writing, IPC has not released official attendance figures.)

The hallmarks of IPC Apex Expo, which celebrated its 20th anniversary this year (some argued that the show is actually older than that, since it's a combination of Apex, founded in 2000, and Printed Circuits Expo, which launched in 1994), include size and pageantry. The IPC Hall of Fame, keynote addresses and committee luncheons all feature a lot of color and lights and balloons and massive flashy electronic displays. Those are distinct improvements over the shows of yesteryear. And there's a clear emphasis on younger engineers, even though there aren't many of that demographic walking the halls.

On the show floor, chatter over China, the virus and the subsequent factory shutdowns was all the rage. The consensus was the situation is probably worse than has been officially disclosed, that supply-chain disruptions range from mild to severe, and that restarting the lines, especially for fabrication plants that typically run 24/7, might be more complicated than anyone has dared to say aloud.

The beneficiaries, if that's proper to say, are those companies that relocated production in the past year to Mexico, Vietnam or Taiwan. Although generally those moves were made to defeat the onerous tariffs, the timing of the coronavirus only reinforced the wisdom of the decision.

For those who attended Productronica last November, there wasn't much new at Apex Expo in the way of equipment or materials. The German trade show remains the best place outside Asia to see brand-new machines, which are then rolled out regionally, as the other shows follow. This year was no exception. Products previously reviewed in our Productronica recap last December are not covered here.

Industry 4.0 and the coming robotic revolution remain points of focus, but there is the inevitable lag between conception and implementation. We are at the point where, if one wanted, a nearly fully automated assembly plant could be realized, with software dictating component pulls and AGVs moving feeders and trays to lines just in time to maintain peak overall equipment effectiveness (OEE). But the cost and time to implement remain prohibitive, and perhaps unachievable in non-purpose-built plants.

Some of the new product highlights from this year's show:

MacDermid Alpha has a new water-soluble paste, WS-860, and an "ultra" low-temperature solder, ULTS, for PET-based flex circuits and SMT assemblies to be soldered under 150°C. The newly acquired Kester brand is not expected to be merged with Alpha, MacDermid Alpha told us.

Henkel rolled out several new materials for specific applications ranging from high thermal conductivity to high reliability. Bergquist Gap Pad TGP 10000ULM thermal interface material (TIM) has a thermal conductivity of 10.0W/m for 5G telecom infrastructure and consumer mobility devices. The latest generation of the Loctite GC series, GC 18, has been qualified and is going into use. Users are looking at it to lower voiding, especially on QFNs.

Seika Machinery showed a robotic handler that loads and unloads routers. The dual-arm Kawasaki Duaro RS series replaces inline equipment, has a safety stop and can hold panels weighing up to 3kg.

The Sakaya SAM-CT34XJ automatic high-speed router supports panels up to 400mm x 300mm. It has an automatically adjustable cutting position, and the router bit height can be automatically switched for longer tool life. It detects removal, breakage, and floating of the blade, and has an optional automatic bit changer.

Malcom Instruments has a spiral viscometer (PCU002V) for spot-checks of solder paste. It requires just a thimble full of paste from the jar to perform its viscosity readings.

Nordson Asymtek added batch operation capability to its Helios SD-960 dispenser. It comes with dual drawers, allowing continuous processing.

Component handling and storage systems were plentiful. The Juki-Essegi partnership continues to pay off with the latest MIM/EEM modules for its Material Tower. New software links with Oracle, SAP and other ERP systems to verify if a component under review is on the AVL.

Likewise, Yamaha had its YST-15 reel storage tower, which debuted in 2019. New to the show was the YRM20 placement machine, a dual-head, dual-beam system with a new high-speed rotary head capable of placing parts sized metric 0201 to 12mm sq. at speeds up to 115,000cph. The system supports multiple chipshooter heads, or a chipshooter and multifunction setup.

Hanwha is cutting line costs by doing away with the conveyors that link printers and SPI machines to placement machines. Rails from the process machines now link up seamlessly, even in a back-to-back printer configuration.

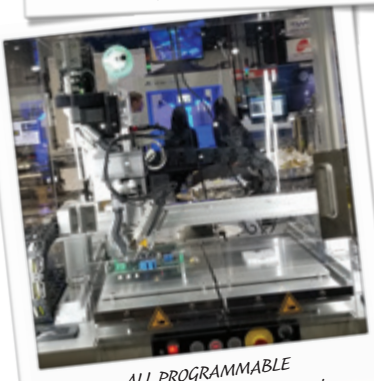
Novacentrix's photonic curing system called PulseForge uses pulses of high-intensity light to heat lead-free alloys to liquidus in milliseconds, much more quickly than forced convection. Check out their video at novacentrix.com.

Vitronics Soltec introduced 3D-Printed Twin-Nozzle for Zeva selective soldering. The patent-pending design has two nozzle diameters combined in one nozzle and makes it possible to solder a board with fine-pitch and multiple-row connectors without stopping for tooling changes.

Thermaltronics' TMT-2200S is a dual-port, single-heater solder station based on Curie Heat Technology said to adjust the power for an individual solder joint on-the-fly.

TWICE AS NICE
The dual-arm Kawasaki Duaro RS robotic handler loads and unloads routers.

JUST A PAT
Malcom Instruments' PCU002V spiral viscometer.



ALL PROGRAMMABLE
Kurtz Ersa's Solder Smart five-axis soldering robot.

Kurtz Ersa had several new tools that were not reviewed in our Productronica coverage. In the Exos 10/26 vacuum reflow soldering system, the vacuum module is situated in the hood, and a long tunnel maintains liquidus temperature to reduce voids. The 26-zone oven features 11 heating and four cooling zones and handles board sizes of 400mm x 630mm in single-lane configuration or 400mm x 280mm in dual-lane. The roller conveyor in the vacuum chamber is the same as used in the firm's selective soldering machines and has no bearings or grease. A medium wave heater is used in place of IR to maintain the temperature profile. The vacuum pump is integrated into the machine on a separate table to prevent vibration and isolate it from the reflow process. The entry-level HR-500 rework system has a medium-wavelength dark IR emitter, for a consistent absorption reflection ratio between dark- and light-bodied components. The HR 550XL is a large board (20" x 20") version. HR 600/3P has 01005 pick-and-place capability and performs pin paste dispensing prior to placement. The Solder Smart five-axis soldering robot has a 150W heater and programmable point-to-point soldering, dwell and feed times.

MEK's PowerSpector GTAz inline AOI series now comes in three longboard models. The nine-camera systems (one top, eight side) handle PCBs from up to 800mm x 550mm, depending on the model. Side cameras now offer a larger field-of-view and 20µm resolution. The systems inspect for component presence, polarity, offset, correctness, soldering and height and can be used for 2-D inspection (pre- and post-reflow, selective or wave soldering) and first-article inspection.

NO SPACE
Hanwha has aligned its printers to other lines to eliminate conveyors.

SPEED DEMON
Yamaha's YRM20 dual-head placement machine.

BACK TO BACK
A pair of Hanwha printers feed a single HM 520 placement machine.

Industry 4.0/smart factory was commonplace, so much so it has become part of the background. There was less this year, however, on the digital twin. One exception: Siemens, which noted virtual models need to be driven by more than IT. Siemens has integrated its Op Center MES with Valor Process CAM; the combined system can share data models such as bills of materials, screen/stencils, SMT, test and inspection. It is extending its ability to monitor the line, with newer options capable of sending pick lists to warehouses. Siemens is tying in Cybord, an Israeli startup that is attempting to prevent counterfeits and malware from entering the field by overlaying a combination of AI and vision capabilities on placement lines.

Mirtec has merged AOI and SPI on a single unit. The camera configuration doesn't change, David Bennett said; the 3-D SPI camera can be used for AOI too.

Novagard and Dow separately introduced UV silicone conformal coatings.

Speaking of conformal coating, Parmi debuted PCI 100, an AOI that uses high-speed scan for conformal coating coverage inspection, contamination/overspray detection and bubble detection. It features a 4M image sensor with telecentric lens camera and uses UV LED lighting for conformal coating inspection and white LED illumination for coating inspection area teaching. The scan speed is 80 sq. cm/sec., at a reported resolution of 16.7 x 16.7µm. Parmi also showed the Axion 3-D AOI, which has a focused two-channel laser for highly specular surfaces (bare die, IPD, die attach, underfill fillet).

Magnalytix has transformed its SIR tester from a multi-unit system with a mass of wires protruding into a beautiful, streamlined design. A steady stream of visitors from defense OEMs observed by this reporter suggested the high-rel sector has noticed.

Each year, the fabrication side of the show seems less busy. Orbotech was unusually reticent. It had a new inkjet solder mask printer called Neos. But finding someone authorized to discuss it was not possible, and booth personnel didn't even allow photos to be taken.

Almost every other machine in the fab section was previously shown, in some cases years ago. Isola did have a pair of new laminates. TerraGreen 400G is a high-speed, low-loss replacement for ceramics in 5G applications. IS550H is a low-CTE, CAF-resistant version for high-power and voltage products. Isola is opening a quickturn manufacturing facility in Chandler, AZ, in the late second quarter.

AGC will have new laminates in a few weeks.

Polar Instruments added a variety of fill types, drill documentation and implemented backdrill capability to its Speedstack PCB stackup design tool.

The technical conference sessions appeared well-attended. Those who attend every conference will note some repeats or updates of previously published work. That said, most engineers lack the budget or time to get to multiple conferences a year, so I'm not certain that covering "old" ground is necessarily a negative. One timely session moderated by Greg Papandrew of Better Board Buying covered best practices for strategic board procurement. A panelist from NI explained the company's process of coupling data from an industry capability index with the specific requirements of a new design to automatically winnow the AVL list to the relevant suppliers. With all the chatter about China and supply chains, that talk couldn't have come at a better time. ▫

MIKE BUETOW is editor-in-chief of PCD&F/CIRCUITS ASSEMBLY; mbuetow@upmediagroup.com.

GOOD LOOKER
Magnalytix has refined the look (and capabilities) of its SIR tester.

Robustness of High Tension, Standard Tension and Mesh Mount SOLDER PASTE STENCILS

An examination of volumetric transfer efficiencies at different aperture locations. **by PRITHVI KOTIAN, JEFF SCHAKE AND MARTIN ANSELM, PH.D.**

The fishbone diagram associated with stencil printing contains a staggering number of variables, the interdependence of which contributes to the high probability of defect origination.[1] Stencil tension is one of the variables and, surprisingly, has not received much attention. This work illustrates the significant influence – particularly with miniaturized, fine-pitch components – that stencil tension has on next-generation PCB assembly results.

This study evaluated the effectiveness of mesh mount, standard clamping tension, and high clamping tension stencils under different parameters, including print quantity and squeegee blades (new/old) by comparing the volumetric efficiencies at the most wear susceptible locations identified on the stencil. The robustness of the stencil is also determined by analyzing the foil for any potential damage at sensitive locations, which includes the components (BGAs and passive devices) within shield enclosure boundaries for printing defects at intervals of 0 ("as received"), 5,000, 10,000, 15,000, and 20,000 print cycles, respectively. Statistical approaches were used to determine how stencil tension influences volumetric efficiencies and which stencil tension provides a more repeatable print. Designing stencil apertures to industry-acceptable area ratios is also of great importance to ensure all the printed solder paste material is deposited on the substrate.[2] These sets of experiments illustrate the effectiveness of stencil tension and provide insight on printing improvements that keep pace with miniaturization of electronic products.

Materials and Test Equipment

Stencil frames. The following stencil frame types were used for analyzing the effectiveness of the stencil tension on the print process:

1. Standard clamping tension master frame, direct foil (mesh-less) attachment to 23" square VectorGuard frame (32N/cm est. tension).
2. High clamping tension master frame, direct foil (mesh-less) attachment to 23" square VectorGuard frame (47N/cm est. tension).
3. Standard mesh mount stencil, permanent glue bonded foil (standard tension) attached to 23" square tubular aluminum frame (35N/cm est. tension).

Types 1 and 2 provide mechanical foil attachment using external air pressure to engage and disengage spring clamps positioned along the frame perimeter. These clamps are designed to secure the foil with uniform tension.[3]

Test vehicle. A single-sided printed circuit containing two different shield perimeter pad designs with BGAs and passive devices both inside and outside their boundaries was used for the study. The dimensions of the board measure 150mm x 100mm x 1mm, as shown in **FIGURE 1**.

The area of interest for print study analysis is indicated by the dashed red line in Figure 1 and **FIGURE 2**. A total of 10 PCB assemblies were used for printing solder paste and analyzing the volumetric efficiencies from a solder paste inspection (SPI) machine.

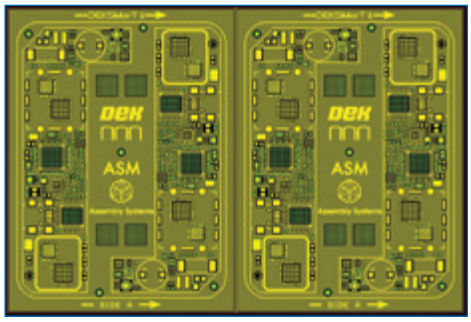


FIGURE 1. Test vehicle PCB with BGAs, passive devices, and shields.

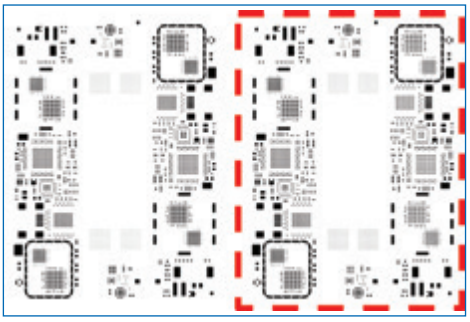


FIGURE 2. Aperture layout of stencil foil.

Solder paste. The solder paste used for this study was a Type 5, lead-free Indium 8.9HFA with an alloy composition of 96.5Sn3Ag0.5Cu and metal content of 88.25%. Type 5 material was selected due to its particle size and print compatibility with miniature components (**TABLE 1**). This particle size solder paste delivers better transfer efficiency and augments printing for miniaturized components such as wafer-scale ultra-fine-pitch array components and sub-01005 passives, which are part of the test board design.

Stencil foil. The stencil foil material was standard stainless steel, with apertures formed via laser cutting. All three stencils were laser-cut in sequence by the same laser tool to ensure minimal differences in quality. Laser-cut technology was chosen due to its broad adoption in the stencil manufacturing process. The stencil foil was 2.4 mils (60µm) thick (Figure 2). The reason for using such a thin stencil foil material was twofold: First, the miniaturized components on the test board design are such that an ultra-thin foil is required to maintain a compatible printing area ratio throughout. Second, the thinner foil degrades more quickly during printing due to coining under repeated stencil wiping, and this acceleration was beneficial for the timeline of this evaluation.

In this study, one stencil foil was used for each frame type, three foils in total. The apertures between the stencils were geometrically identical, created from the same stencil Gerber file and processed on the same laser-cutting tool. A removable coupon with test apertures was produced on the foils to verify stencil aperture size accuracy and repeatability. A size tolerance range of ±0.005mm was given to the stencil manufacturer to ensure aperture uniformity was achieved.

Squeegees. A metal squeegee material, which is the industry norm, was selected for this experiment, as it produces consistent solder volumes and is resistant to scooping the solder paste out of the apertures during printing. The spring metal steel blade was 7.8 mils (0.2mm) thick. This study required a total of eight squeegee blade pairs. The printing of 10 boards required use of both the forward and reverse squeegee on the stencil printer. Hence, the mesh mount frame was the first stencil which required two squeegees to conduct the print test on 10 PCBs, as well as continuous printing until achieving 20,000 cycles. These squeegees were then replaced post-20,000 print cycles with new blades and another 10-print test conducted. This methodology allowed investigation of the print quality of a worn stencil using worn squeegees, as well as comparison to new squeegees on the worn stencil. The new set of squeegees used for the worn mesh mount stencil was then used for printing a new standard clamping tension VectorGuard stencil. This experiment routine was repeated with the high clamping tension VectorGuard stencil.

Test equipment and inspection. The SMT assembly equipment used for this test included an ASM DEK Horizon 01iX stencil printer and a Koh Young 3030VAL SPI. A Keyence VHX-6000 digital microscope was used to visually inspect paste deposits for shield perimeter pads, BGAs, and passive devices. **FIGURES 3A** and **3B** show numbered locations (in blue), which indicate the sites measured by the SPI. Shield 1 BGA aperture designs are squares, while Shield 2 BGAs are circles. The Shield 2 pattern is orientated 180° relative to Shield 1. All other design features of the two shields are the same.

Similarly, all BGAs within Region A (Figure 3b) are square apertures, and BGAs within the Region B are circular apertures. Shields 3 and 4 have a different perimeter pad design compared to Shields 1 and 2, requiring fewer apertures and spaced farther apart (i.e., low aperture density shield aper-

TABLE 1. Component Designations

Notation (ID Label)	Pitch (mm)	Aperture Shape	Aperture Size (mm)	Number of Pads	Description	Shield
1	0.3	Square	0.18	196	BGA	1
2	0.4	Square	0.225	196	BGA	1
3	N/A	Rectangle	0.22 x 0.18	60	01005 Passive	1
4	0.3	Circle	0.18	196	BGA	2
5	0.4	Circle	0.225	196	BGA	2
6	N/A	Rectangle	0.22 x 0.18	60	01005 Passive	2
7	0.3	Square	0.18	196	BGA	3
8	0.4	Square	0.225	196	BGA	3
9	N/A	Rectangle	0.22 x 0.18	60	01005 Passive	3
10	0.3	Circle	0.18	196	BGA	4
11	0.4	Circle	0.225	196	BGA	4
12	N/A	Rectangle	0.22 x 0.18	60	01005 Passive	4
13	0.8	Square	0.37	64	BGA	N/A
14	0.8	Circle	0.37	64	BGA	N/A

tures). Data presented later in this paper illustrate that print results on devices contained inside the two unique shield perimeter design apertures are influenced differently as stencils are worn. Table 1 shows the detailed list of component descriptions and aperture designs used for quantitative and qualitative analysis.

Test Sequence

The test approach for the given PCB assembly was as follows:

- Assess the capability of SPI by conducting a gage repeatability study with and without bare board teach (BBT) option.
- The high flatness quality of PCBs used did not require use of BBT in SPI to produce highly repeatable results.
- A printed reference board was used to verify the accuracy of the SPI and was preserved and maintained throughout the project.
- PCBs were numbered to retain the same run order for all 10-print run quality tests, each one measured by SPI. The tenth board was also manually examined under a digital microscope, and designated locations were photographed.
- New squeegee blades were used for initial 10-print run quality testing on each of the three "as received" condition stencils. Endurance printing to wear stencils was performed until accumulating 5,000 wipes, followed by another 10-print run quality test. Intervals of 5,000 wipe endurance printing and 10-print run quality tests continued (using the same squeegee blades) until endurance printing achieved 20,000 wipes. Note: The print parameter differences between "quality tests" and "endurance printing" are explained in **TABLE 2**. The final print quality test for each print-fatigued stencil was performed after replacing the worn squeegees with new blades.

Stencil Printing Parameters

Key printing machine operating parameters are listed in Table 2 and include squeegee speed, squeegee pressure, separation speed and separation distance. These settings were chosen with consideration to the delicate, thin foil to accommodate SMT production tempo, while suited to the testing purpose.

Observations and Discussion

In the early stages of print cycling, all stencils produced similar quality printing results, but there was a point at which the accumulated cycles from endurance printing started to degrade print quality across the stencils at unequal rates. The mesh mount stencil was first to reveal highly visible indications of surface wear. The regions on the foil surrounding Shield 1 and 2 (the high aperture density shields) were specifically impacted by recurring squeegee contact, becoming marred with prominent witness lines. These two regions also exhibited tension loss occurring within the shield perimeter apertures. Attempts were made to characterize tension over time using a dial indicator to record local foil deflection under a range of controlled applied weights, but the poor measurement repeatability from the crude apparatus proved impossible for proper trend interpretation. However, the print quality results measured by SPI in the Shield 1 and 2 regions correlated well with the perceived deteriorating tension. SPI data showed elevated levels of print volume data scatter, which is reflected in boxplot and standard deviation data graphs referenced later in this article.

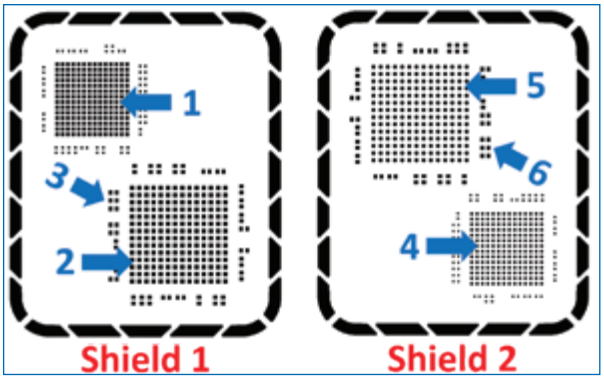


FIGURE 3A. Stencil detail of wear-sensitive apertures in the "high aperture density" shield enclosed areas.

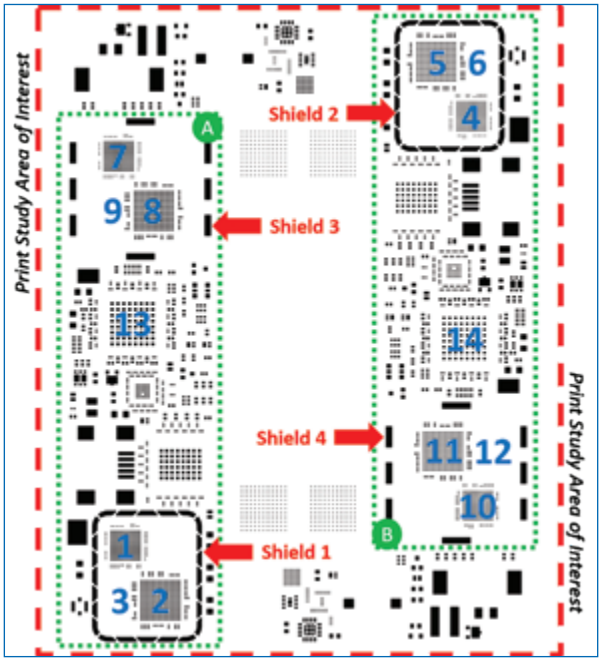


FIGURE 3B. Full stencil detail of solder paste inspection and optical microscopy template.

TABLE 2. Parameters for Experimental Study

Parameters	10-Print "Quality" Test	"Endurance" Printing
Tooling Type	Vacuum	Vacuum
Print Speed	50mm/sec	200mm/sec
Print Pressure	5.0KG	6.0kg
Sep. Speed	20mm/sec	20mm/sec
Sep. Distance	2.0mm	0.0mm

What is believed to have occurred sooner on the mesh mount stencil compared to the other two stencils is the foil tension translating through the narrow web interspaces between the large perimeter shield apertures (for Shields 1 and 2) was not high enough to counteract a natural curling response of the foil. This curling behavior develops from the accumulation of abrasion stress caused by the squeegee, much like a ribbon would behave when slid across a sharp blade. The stencil foil overcomes this tendency to curl, as long as there is enough outward applied tension to maintain its straightness. When the applied tension is insufficient to continue holding the foil level, it may deviate from planarity and succumb to the unremitting curl stress condition. The consequences of this are believed to impact both aperture filling and release processes, setting up unfavorable print control conditions that ultimately degrade the opportunity to produce uniform prints.

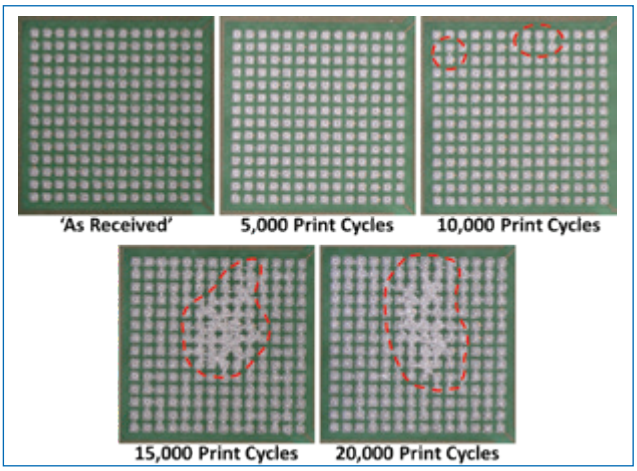


FIGURE 4. Print quality results using mesh mount stencil for BGA component ID 1.

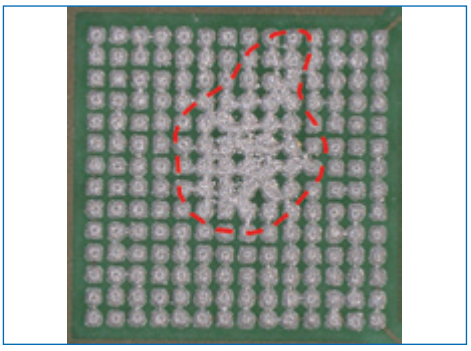


FIGURE 5. Detail of BGA component ID 1 print quality results after 15,000 print cycles.

Shield 1 region analysis. The impact of stencil wear on print quality is illustrated by the progression of print defects observed across the various print quality tests taken at milestone print cycles. Component ID 1 located inside Shield 1 serves as an excellent example for this, as referenced in **FIGURE 4**, where photos of this printed BGA site are shown after the tenth consecutive print using the mesh mount stencil. Neither this stencil nor the two other stencils were cleaned between print strokes (during the "quality" test) in order to witness and compare natural process degradation. Note that all stencils were thoroughly cleaned at endurance printing milestone print cycles. The 10,000-cycle print quality test marked the first occurrence where any visible paste bridging defects were seen, labeled by the red dashed outlines in Figure 4. The 15,000 and 20,000 cycle print quality tests showed expanded regions of paste bridging. **FIGURE 5** shows a detailed view of the 15,000-cycle print quality test, where it is apparent that bridging defects are even more widely occurring. Missing from these images is the 20,000-cycle print quality test result after replacing worn squeegee blades with new blades. It was consistently observed with all stencils tested that the installation of new squeegee blades after 20,000 print cycle "endurance" printing did not typically improve print quality to overcome any previous occurring defects.

Data analysis. Solder paste inspection volumetric data were recorded for each print in the group of ten boards run in the quality test after milestone endurance cycles at time 0 (as received), 5,000, 10,000, 15,000, 20,000, and 20,000 with new squeegee blades for all three stencils under their different tensions. Graphical trend analysis of box and whisker plots means interval and standard deviation distributions provided the essential details for evaluating the print quality behavior over the course of experiments.

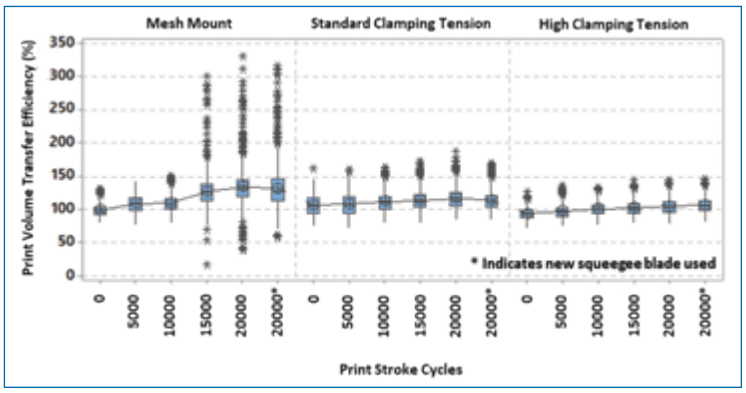


FIGURE 6. Boxplot results of all 10 print run quality tests for all stencil frame types at BGA component ID 1.

Statistical Analysis

Box and whisker plot analysis. The presence of high solder paste volume transfer outliers was the main SPI recorded defect, which correlated to the observations of solder bridging previously shown. The box and whisker plot in **FIGURE 6** offers a clear indication that mesh mount and standard clamping tension stencils have higher variances, whereas the high clamping tension stencil has better stability with printing performance, exhibiting almost constant mean throughout the process. A controlled mean paste transfer efficiency of nearly 100% is an excellent outcome and was achieved by all stencils in early stages of wear testing, but from 10,000 print cycles onward, the stencil types began to show

deviating results. An outlier transfer efficiency percentage of more than 150% indicates an excessive amount of paste volume, signaling the process is escalating out of control, and intervention is required to restore optimal paste transfer efficiencies.

Interval plots. Continuing the discussion focus on BGA component ID 1, the interval plot in **FIGURE 7** provides an overview of the cumulative mean volume paste transfer at different stages of printing the stencils through this course of study. Higher mean paste transfer generally correlated to higher standard deviation (i.e., more print volume scatter), but results of the high clamping tension stencil were the closest to maintaining the ideal 100% paste transfer across all the printing cycles compared to the other frames.

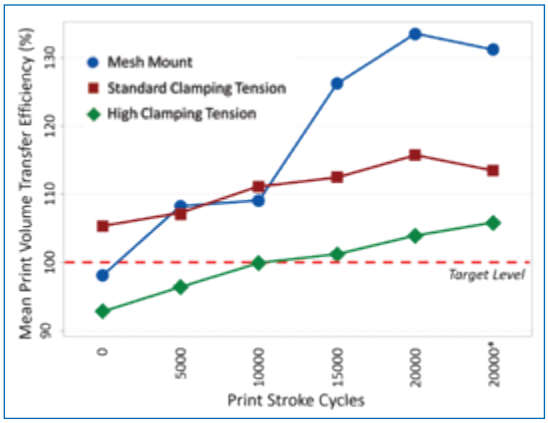


FIGURE 7. Interval plot for BGA component ID 1.

Standard deviations. Surveying the print volume data by computed standard deviations provides a quick and convenient method to perform process control comparisons. The measure of producing highly uniform print deposits is characterized by achieving the lowest standard deviation values. The next several figures compare print results by standard deviation analysis calculated from all print deposits in a device type combined across the 10-print quality test. This grouping of print volume transfer efficiencies is the source data from which a standard deviation is derived. The standard deviations were analyzed and compared for all the components specified in Table 1. **FIGURES 8** to **14** present this series of standard deviation trend graphs, tracking print uniformity results from quality tests for the three stencil types across the full test range of endurance print stroke cycles. The graphs are identically formatted and separately organized for pairwise component-level comparison. It is typically accepted and applied here that a standard deviation value of 10% denotes the pass/fail process control threshold (indicated by the dashed red line in these figures).[4] The strongest observations concerning the influence of the stencil tension variable from a collective viewpoint of all these figures can be summarized as follows:

1. Stencil tension is found to have the largest influence on print uniformity for the components located within the two high aperture density shield areas (i.e., Shields 1 and 2). The print quality benefit of using high foil tension is clear.
2. In the printed regions of the board outside of Shields 1 and 2, the benefit of high tension on print control is either less significant or has no clear impact.

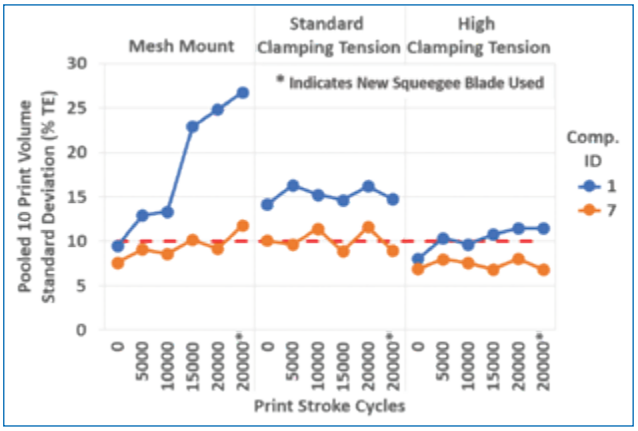


FIGURE 8. Standard deviations of 0.3mm pitch BGAs, square apertures, component ID 1 (Shield 1) vs. component ID 7 (Shield 3).

Conclusions

This robustness study of three different types of stencils provides interesting insight on the role of stencil tension in printing performance and offers a unique opportunity to implement a new strategy for improving process yield. The most important discovery was identifying that not all aperture regions on the stencil respond equally to the application of foil tension.

Specifically, devices positioned inside the borders of high aperture density shields exhibited the greatest disparity of print quality among the stencils tested. The most significant print uniformity improvements attributed to increasing foil tension were witnessed for components at these sensitive locations. In general, the work suggests a distribution of sufficient tension across the stencil foil capable of maintaining suitable coplanarity throughout the print cycle is required to mitigate print defect opportunities.

A high-tension stencil frame can help safeguard printing consistency in volumetric efficiencies for fine-pitch compo-

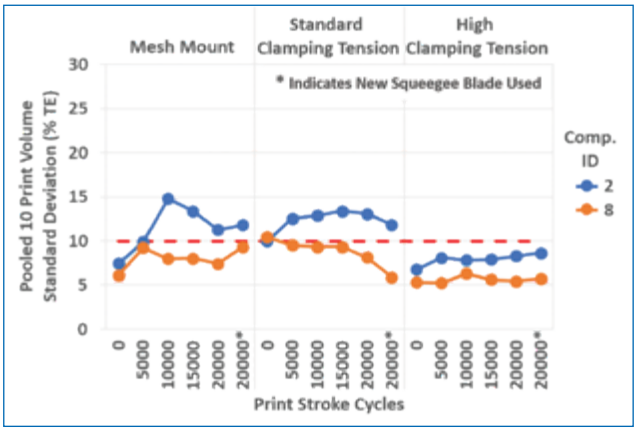


FIGURE 9. Standard deviations of 0.4mm pitch BGAs, square apertures, component ID 2 (Shield 1) vs. component ID 8 (Shield 3).

nents across a variety of positional configurations as demonstrated across 20,000 print cycles. Finally, the durability and survivability of the delicate, thin foil tested under the subjected high clamping tension applied was impressive. Further evaluation and technical reporting on the performance of this apparatus are forthcoming. ▫

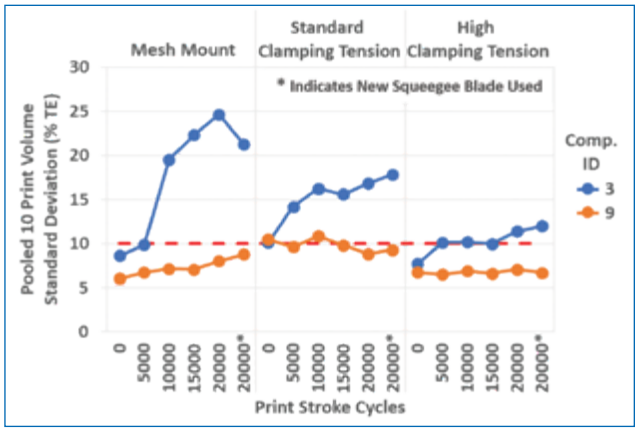


FIGURE 10. Standard deviations of 01005 passive devices, component ID 3 (Shield 1) vs. component ID 9 (Shield 3).

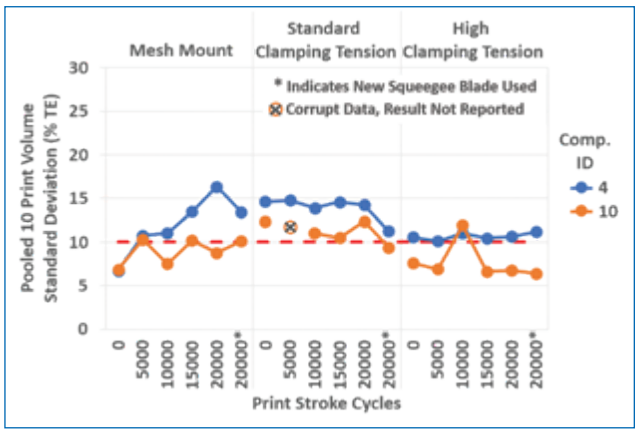


FIGURE 11. Standard deviations of 0.3mm pitch BGAs, circle apertures, component ID 4 (Shield 2) vs. component ID 10 (Shield 4).

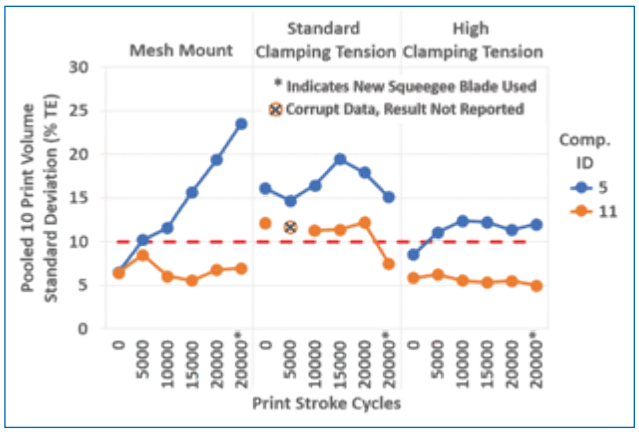


FIGURE 12. Standard deviations of 0.4mm pitch BGAs, circle apertures, component ID 5 (Shield 2) vs. component ID 11 (Shield 4).

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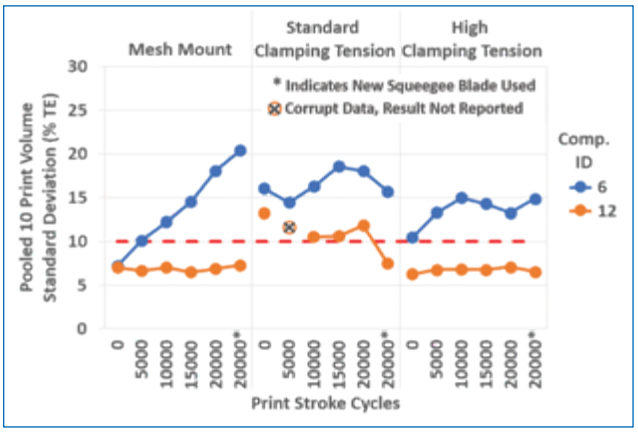


FIGURE 13. Standard deviations of 01005 passive devices, component ID 6 (Shield 2) vs. component ID 12 (Shield 4).

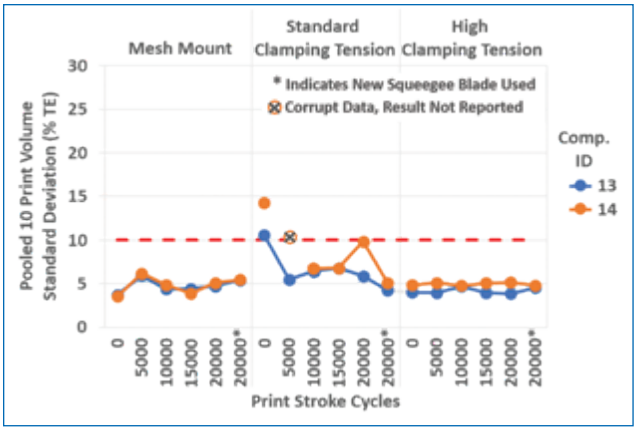


FIGURE 14. Standard deviations of 0.8mm pitch BGAs, component ID 13 (square apertures) vs. component ID 14 (circle apertures).

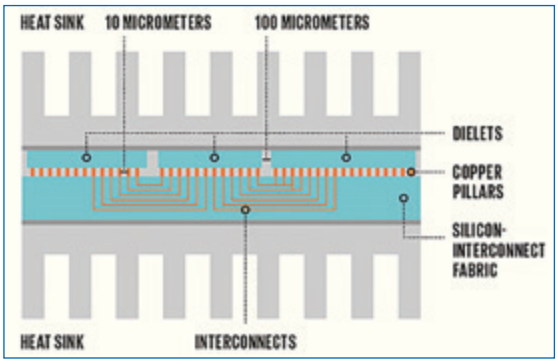
State-of-the-Art Technology Flashes

Updates in silicon and electronics technology.

Ed.: This is a special feature courtesy of Binghamton University.

Transistors can process and store information. Purdue University researchers have created a feasible way to combine transistors and memory on a chip, potentially bringing faster computing. They used a semiconductor that has ferroelectric properties. This way two materials become one material, and without worry about the interface issues. The result is a so-called ferroelectric semiconductor field-effect transistor, built in the same way as transistors currently used on computer chips. The material, alpha indium selenide, not only has ferroelectric properties, but also addresses the issue of a conventional ferroelectric material usually acting as an insulator rather than a semiconductor due to a so-called wide "band gap," which means that electricity cannot pass through and no computing happens. *(IEEC file #11468, Science Daily, 12/9/19)*

Motherboard replacement – Silicon-interconnect fabric. Research shows the printed circuit board (PCB) could be replaced with the same material that makes up the chips that are attached to it. This would lead to smaller, lighter-weight systems for wearables and other



size-constrained gadgets, and to powerful high-performance computers. This all-silicon technology (silicon-interconnect fabric), permits bare chips to be connected directly to wiring on a separate piece of silicon. Unlike connections on a PCB, the wiring between chips on fabric is as small as wiring within a chip. Many more chip-to-chip connections are thus possible, and those connections transmit data faster while using less energy. *(IEEC file #11382, IEEE Spectrum, 10/1/19)*

Tiny organic films could enable new electronics. Researchers at the University of Chicago and Cornell University have discovered an easy, efficient way to grow extremely thin films of organic materials. The findings could be a stepping stone to future electronics or technologies with new abilities. Scientists have known for a long time how to make extremely thin layers – down to a few atoms thick – out of inorganic materials. That's how cellphones have shrunk in size and solar panels have sprung up on roofs around the world. But duplicating that manufacturing process with materials that are organic (something containing carbon) has been tricky. *(IEEC #11443, Printed Electronics World, 10/30/19)*

New photonics breakthrough. A new approach to trapping light in artificial photonic materials by City College of New York researchers could lead to a tremendous boost in the transfer speed of data online. Research into topological photonic metamaterials reveals that long-range interactions in the metamaterial changes the common behavior of light waves forcing them to localize in space. Hence, by controlling the degree of such interactions, one can switch between trapped and extended character of optical waves. The approach to trap light permits the design of new types of optical resonators, which may have a significant impact on devices used daily. These range from antennas in smartphones and Wi-Fi routers, to optical chips in optoelectronics. *(IEEC file #11484, Science Daily, 12/13/19)*

Highly sensitive diode converts microwaves to electricity. The Japan Science and Technology Agency (JST), Fujitsu, and the Tokyo Metropolitan University announced development of a highly sensitive rectifying element in the form of a nano wire backward diode, which can convert low-power microwaves into electricity. It is expected that the newly developed nanowire backward diode will be applied in using plentiful ambient radio wave energy in 5G communications, serving as a stable power source of sensors and contributing to battery-free sensors. *(IEEC file #11380, Science Daily, 9/26/19)*

Artificial intelligence may help scientists make spray-on solar cells. A research team at the University of Central Florida used artificial intelligence to optimize the materials used to make perovskite solar cells (PSC). The organic-inorganic halide perovskites material used in PSC converts photovoltaic power into consumable energy. These perovskites can be processed in solid or liquid state, offering a lot of flexibility. Imagine being able to spray or paint bridges, houses and skyscrapers with the material, which would then capture light, turn it into energy and feed it into the electrical grid. Until now, the solar cell industry has relied on silicon because

BINGHAMTON UNIVERSITY currently has research thrusts in healthcare / medical electronics; 2.5-D/3-D packaging; power electronics; cybersecure hw/sw systems; photonics; MEMS; and next-generation networks, computers and communications. The S3IP Center of Excellence is an umbrella organization comprising five constituent research centers.

INTEGRATED ELECTRONICS ENGINEERING CENTER (IEEC) is a New York Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging. Its mission is to provide research into electronics packaging to enhance our partner's products, improve reliability and understand why parts fail. More information is available at binghamton.edu/ieec.

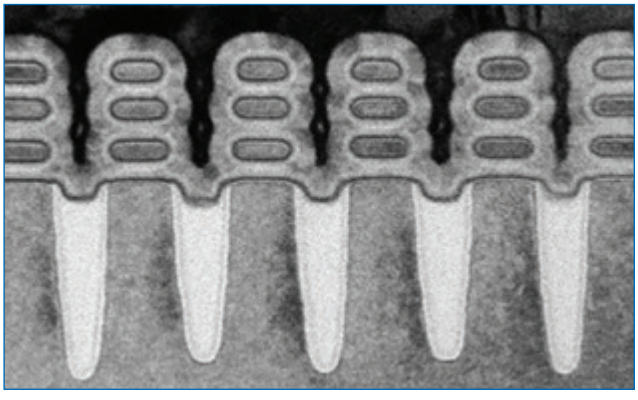
of its efficiency. *(IEEC file #11485, Science Daily, 12/16/19)*

3-D printed bio-compatible battery-free wireless stretch sensors. Georgia Tech has developed 3-D-printed bio-compatible battery-free wireless stretch sensors. A potential application is pressure-sensing inside brain blood vessels damaged by aneurysms. Aerosol jet 3-D printing is a fabrication technique in which a fine mist of droplets is blown onto a substrate through a small nozzle (200-300µm dia.), allowing patterns to be drawn as the nozzle is moved. Two different inks are deposited, one that dries to a layer of polyimide insulator, and one that leaves a layer of silver nanoparticles. Printed onto a thin PMMA layer on a glass substrate, the following layers are deposited: polyimide, silver, polyimide, silver. *(IEEC file #11340, Electronics Weekly, 8/30/19)*

Memory device can be written on and read out optically or electrically. Scientists at TU Dresden have developed a novel storage technology based on the combination of an organic light-emitting diode (OLED) and an insulator. This device allows reading the stored information optically as well as electrically. The information can be added in portions. The storage unit called "pinMOS" is a non-volatile memcapacitor with high repeatability and reproducibility. The special feature is that pinMOS stores several states, since charges can be added or removed in controllable amounts. Another feature is this simple diode-based memory can be both electrically and optically written to and read from. *(IEEC #11452, Science Daily, 11/25/19)*

Printed metal conductors – the next-generation electronic displays. Displays from smartwatches to 4K TVs currently consist of OLEDs which use indium tin oxide (ITO) as a transparent electrode. However, ITO has its limitations: it is expensive; doesn't perform well enough for larger areas; and can crack with repeated touching or swiping. University of Pittsburgh and Electronink researchers are looking to replace ITO with metal "microgrid" conductors to improve OLED performance using metal ink in its circuit drawing kit called Circuit Scribe. The device includes a pen that uses conductive silver ink to allow users to create working lights with circuits drawn on paper. *(IEEC #11449, Printed Electronics World, 11/20/19)*

Nanosheet devices projected to 3-nanometer node by 2021. One of the astounding things about the nanosheet design is it may extend Moore's law. Transistor density is still increasing with every technology node. But the amount of heat an IC can reasonably remove has been stuck at about 100W/sq. cm for a decade. To keep the heat down, clock rates don't exceed 4GHz. One potential solution is to introduce new materials into the channel region, such as germanium or semiconductors composed of elements from columns III and V of the periodic table, such as gallium arsenide. Electrons can move more than 10 times as fast in some of these semiconductors. *(IEEC file #11286, IEEE Times, 7/30/19)*



Market Trends

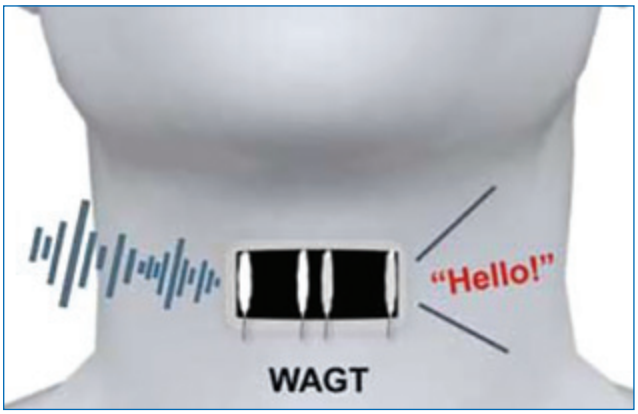
AI device manufacturing to hit 15 million by 2024. The total installed base of artificial intelligence (AI)-enabled devices in industrial manufacturing is forecast to reach 15.4 million within five years, with a CAGR of 64.8% from 2019 to 2024. It's claimed that AI will revolutionize the industrial manufacturing space, and in many respects that transformation has already begun. AI is already delivering generative design in product development, production forecasting in inventory management, and machine vision, defect inspection, production optimization, and predictive maintenance in the production phase. Another commercial use case currently gaining momentum is defect inspection. The total installed base for this use case is expected to grow from 300,000 in 2019 to more than 3.7 million by 2024. *(IEEC file #11393, Global & SMT Packaging, 10/2/19)*

Cybersecurity market to reach $117.9 billion in 2019. A new cyber report indicates the global cyber security market will see $117.9 billion in spending in 2019. One of the biggest trends in trusted-computing is an increase of mainstream awareness among organizations of all sizes when it comes to protecting their information. The second major trend is a massive expansion in the number of devices, and the number of bandwidth enterprises are leveraging, forcing them to seek solutions that are scalable and eliminate the need to backhaul security to the corporate office. By leveraging new node-based architectures, organizations can protect their information in a massively efficient way. *(IEEC file #11436, Military & Aerospace Electronics, 10/31/19)*

6G research gets underway this year. As 5G hits the first year of deployment from the first time initial commercial trials were started in the US by Verizon and AT&T, GSA is reporting that 50 commercial 5G networks have been deployed as China's big three activated 5G networks on Nov 1. Since most of the 3GPP 5G are in-process at this point, so somewhat determined, several research activities have been announced for 6G. Earlier this year, NYU Wireless showed demonstrations of a 140GHz system and is doing several studies with systems in this frequency range. The University of Oulu's Center for Wireless Communications gets funding for the next eight years for project 6Genesis: 6G-Enabled Wireless Smart Society & Ecosystem. Their charter is for the wireless vision for 2030. The low latency of 5G may not be good enough for 6G, and using 100 to 1000GHz signals will be needed to handle data

rates up to terabit/s speeds. *(IEEC #11444, Microwave Journal, 11/14/19)*

Researchers develop a wearable artificial throat. Researchers at ACS Nano have developed a wearable artificial throat that, when attached to the neck like a temporary tattoo, can transform throat movements into sounds. To make their artificial throat, they laser-scribed graphene on a thin sheet of polyvinyl alcohol film. The flexible device measured 0.6 by 1.2". The researchers used water to attach the film to the skin over a volunteer's throat and connected it with electrodes to a small armband that contained a circuit board, microcomputer, power amplifier and decoder. In the future, mute people could be trained to generate signals with their throats that the device would translate into speech. *(IEEC file #11293, Printed Electronics World, 7/29/19)*



Recent Patents

Integrated optical sensor and method of producing an integrated optical sensor (assignee: AMS AG). Patent No. 10,453,972 – An integrated optical sensor comprises a semiconductor substrate, an integrated circuit, a dielectric layer, a wiring, a structured filter layer and a diffuser. The semiconductor substrate has a main surface and the integrated circuit (IC) is arranged in the substrate at or near the main surface. Furthermore, the IC comprises at least one light sensitive component. The dielectric layer comprises at least one compound of the semiconductor material. The dielectric layer is arranged on or above the main surface. The wiring is arranged in the dielectric layer and provides an electrical connection.

Assembly with through-mold cooling channel formed in encapsulant (assignee: Micron Technology). Patent No. 10,424,531 – Semiconductor device assemblies having stacked semiconductor dies and thermal transfer devices that include vapor chambers are disclosed herein. In one embodiment, a semiconductor device assembly includes a first semiconductor die having a base region, at least one second semiconductor die at the base region, and a thermal transfer device attached to the first and second dies. The thermal transfer device includes an encapsulant at least partially surrounding the second die and a via formed in the encapsulant. The encapsulant at least partially defines a cooling channel that is adjacent to a peripheral region of the first die.

Multiple underfills for flip chip packages (assignee: Texas Instruments). Patent No. 15/975167 – A method of assembling a flip chip IC package includes applying core underfill material to a surface of a package substrate in a pattern including an area corresponding to a core region of an IC die thereon that is to be attached, that excludes an area corresponding to corners of the IC die. The IC die is bonded to the package substrate by pushing the IC die with a sufficient force for the core underfill material is displaced laterally by the bumps so the bumps contact the land pads. After the pushing the corners of the IC die are not on the core underfill. Edge underfilling includes dispensing a second underfill material that is curable liquid to fill an area under the corners of the IC die.

Liquid-cooled integrated circuit system (assignee: Hewlett Packard). Patent No. 10,499,488 – A liquid-cooled integrated circuit system includes two printed circuit assemblies having removable heat spreaders and cooling pipes coated with a thermal interface material. The two printed circuit assemblies are placed together in opposition such that the top surfaces of the heat spreaders on each printed circuit assembly contacts, and become thermally coupled with, the thermal interface material on the cooling pipes of the other printed circuit assembly. In this arrangement, each printed circuit assembly is cooled by the other. □

AI Yi-Yi-Yi-Yi! Electronics X-ray Inspection and Artificial Intelligence

What are the questions we should ask before diving in?

TO DELIBERATELY MISQUOTE and mangle Shakespeare once again, I come to praise AI, not to bury it, but does the potential evil it may do live after and the good oft interred in the dataset?

I apologize, but … discussion of the benefits of AI in all manner of applications has been the flavor of the month for much of the last two years, and there seems no end in sight! It has been one of the drivers of processor manufacture and use in recent times. However, two recent articles from BBC News seemed to highlight some pros and cons regarding use of AI for x-ray inspection and test.

The first[1] describes how AI has been trained to best radiologists examining for potential issues in mammograms, based on a dataset of 29,000 images. The second[2] is more nuanced and suggests that after our recent "AI Summer" of heralded successes on what could be considered low-hanging fruit, we might now be entering an AI Autumn or even an AI Winter. In the future, it suggests, successes with more complex problems may be increasingly difficult to achieve, and attempts are made only due to the hype of the technology rather than the realities of the results.

For x-ray inspection and AI, it is important to distinguish between what are, say, 1-D and 2-D AI approaches. 1-D AI, I suggest, is predictive information from huge quantities of data from which patterns can be far more easily discerned than by a human observer. It is based on individual data fields, such as those garnered from shopping and social media sites: for instance, a pop-up advertisement for something under consideration for purchase, or inferences on one's political and societal alignments based on their social media selections and feeds. We may actively or passively choose to provide such information, and its predictive abilities may be construed as for good or ill.

In 2-D AI, identification and pass/fail analysis are based on images, as is required for x-ray inspection. This approach, I believe, raises whole levels of complexity for the AI task. Thus, I have the following questions about how 2-D AI will work with the x-ray images we capture for electronics inspection:

- What is, and should be, the minimum size of the image dataset on which board analysis can be relied? Is there a sufficient quantity of "similar" images from which the AI can build its "ultimately opaque to the user" algorithm on which results will be based? Adding images to the dataset will modify/improve the AI algorithm (more on that in a moment), but how much time is acceptable for human operators to grade the AI results to train/improve the dataset, especially if multiple datasets will be required for different inspection tasks, including analyzing the same component at different board locations?
- How complicated are the individual images in what they show? **FIGURE 1** shows an x-ray image of a BGA on a simple board with little internal board layer structure and no second-side components. Compare this to **FIGURE 2**, a more "real" situation seen in PCB production, yet still relatively simpler than much of what is manufactured today. Finally, compare both images to **FIGURE 3**. Although the fault is clear to the human eye, the additional overlapping information from other parts of the board certainly makes human analysis of this BGA more challenging. If there were only a single, subtle solder ball fault present in Figure 3, then perhaps an AI approach might fare better than a human, given sufficient examples. With this in mind, are there sufficient board quantities to produce an acceptable dataset of images? It is probable applications like those shown in Figure 1 are most appropriate for AI today, as there is likely to be much more simplicity in each image, and the AI can obtain many similar examples from which subtle variations not observable to the human eye may be found. As for Figures 2 and 3, will new image datasets be needed for analysis of the same component when it is used in different locations on the same board or on entirely different boards? How often might an AI algorithm need to be (re) verified?
- What is the quality of the images in the dataset? Will the (potential for) variability in the performance of the x-ray equipment hardware and software over time impact AI algorithm performance? The typical x-ray detector used in x-ray equipment for electronics today is a flat panel detector (FPD). These silicon CMOS array devices already include small quantities of missing (non-working) pixels from their manufacture that are interpolated by software methods so as not be seen in the final image. Can/do the number of missing pixels increase with time and use of the FPD? If so, how often should a missing pixel FPD correction algorithm be run? Once run, does that impact the AI algorithm and question/affect previous and future results? Does x-ray tube output variability,

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if it occurs over time, affect the AI algorithm because the image contrast could vary? Can different x-ray equipment be used with the same AI algorithm? If you add images from multiple x-ray systems into the same algorithm, does this affect it in a positive or negative way? What might be the effects of other wear-and-tear on the AI algorithm, and component replacement (e.g., PC) on the x-ray system taking the images? Repeated system image quality checks should mitigate these issues, but how often?

- Is there a possibility of bias of/in the dataset? Perhaps this is more of an issue for facial recognition than when looking at a quantity of boards, but if you are running the same AI algorithm on multiple x-rays systems and all are adding to the learning dataset, does that necessarily mean the test always gets better, and could the dataset become biased? When bringing a new x-ray system online for the same task, do you need to keep a reference standard set of boards upon which to create a "new"AI algorithm if you cannot "add" to an existing one? Are you able to even keep a set of reference boards in case the algorithm is lost or modified from its previously successful version if conditions change? If there is a new algorithm created on a new, additional x-ray system, either from an existing or a new supplier, are any of these truly comparable to what you have done before?
- What about the fragility of the underlying images themselves, ignoring any equipment hardware changes or variability? It has been shown that deliberately modifying only tens of pixels in a facial image can completely change its predictive success within an AI dataset, modifications that would not be seen by a human operator. For example, at the recent CES 2020, at least one company offered to seek to frustrate facial recognition checks with a program that deliberately makes minor changes to photos to prevent people from being recognized.[3] While deliberately adulterating x-ray images of PCBs is extremely unlikely, could degrading FPD cause sufficient pixels to be changed such that the results are not recognized by an existing AI algorithm, especially if running the same inspection task over months and years? As suggested above, frequent (how often?) quality and consistency checks on the image output should help mitigate these fears, but how often are they needed, and how does that impact inspection throughput?
- Ultimately, do any of my questions matter? If you get, or appear to get, a "good" automated pass/fail result, then does the method used matter? If so, can you be confident this will always be the case for that board analysis in the future?

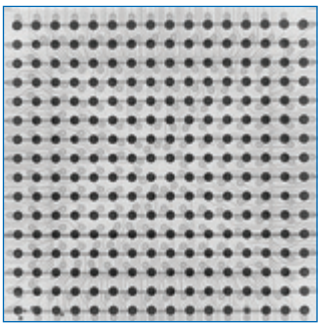

FIGURE 1. Simple image of a BGA?

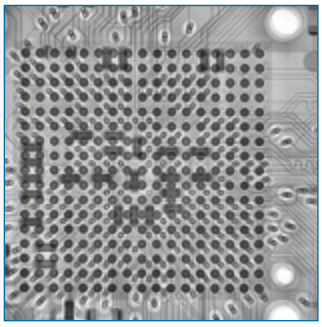

FIGURE 2. Less simple image of a BGA?

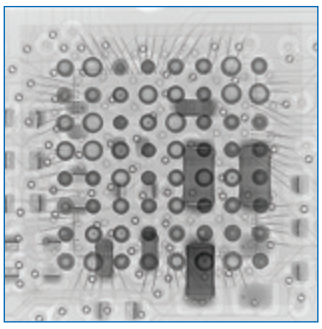

FIGURE 3. An easy image for human and AI identification of the issue? Do the second-side components, wires, movement of components relative to each other during reflow, etc. make it more difficult to analyze if only a single, subtle failure is present?

As a comparison for electronics x-ray inspection today, consider the BBC example of analyzing mammograms.[1] They use a large number of images, I assume of similar image quality, on fields of view that are, I understand, painfully obtained to attempt to achieve more consistency through making a narrower range of tissue thickness across the dataset! In electronics applications, do we have a sufficient quantity of similar images for our board/component analysis AI to produce a reasonable test? Is there more variability in the positional and density variation possible for our electronics under test compared with a mammogram?

What does this mean for x-ray inspection of electronics? Already many equipment suppliers are offering AI capabilities. But what are the questions we should ask about this amazing technology and its suitability and capabilities for the tasks we must complete? We don't know precisely the algorithm used for our tests. We are not certain of having sufficient (and equivalent) images or how many are needed. Adding more over time should give better analysis – a larger dataset – but are they consistent with what went before and, if not, are they materially changing the algorithm in a better way, indicating some escapes may have been made in the past? Sophistry perhaps. But if we do not know what the machine algorithm is using to make its pass/fail criteria, are we satisfied with an "it seems to work" approach?

The more complicated the image, the larger the dataset needed to provide a range of pass/fail examples with an inspection envelope. Variability of the mammograms and the 29,000 images used may well lie within a narrower variation envelope than the BGA in Figures 2 and 3. Perhaps AI for electronics is best suited today for where the image is much simpler and small, as in Figure 1. Automatically identifying variations in the BGA solder balls would naturally be assumed to be better undertaken by the AI approach, but does the variability of the surrounding information affect the pass/fail AI algorithm? Add the potential for movement of com-

ponents during reflow, warpage of boards, etc., and we have more variability in the placement of the features of interest, perhaps requiring a larger image dataset to cover this larger range of possibilities. Then consider adding an oblique view for analysis and these variabilities further enlarge the envelope of possibilities. How many images do you need to get an acceptable test: 100, 1,000, 10,000, 100,000? A bad test is worse than no test, as you are then duplicating effort. Will you get that many images in the test run of the boards you make? And, outside of cellphones, PCs, tablets and automotive (?) applications, is there sufficient product volume to obtain the necessary dataset? If AI tests are applied for automotive applications, is there a complicated equation for quality of test vs. sufficient volume of product vs. complexity/quality of image over time vs. safety critical implications, should an escape occur?

I have asked too many questions and admittedly do not have the answers. I hope the AI experts do and can advise you accordingly. Perhaps the best approach now is to use AI if you are comfortable doing so and consider the images you will be using for your AI test. The simpler the image, the quicker and better the results perhaps, but does that describe the imaging problem you want your AI to solve? Consider the opportunity for using PCT to obtain images at discrete layers within a board's depth to improve the AI analysis by decluttering the images from overlapping information. However, are you at the right level in the board if there is warpage? And are you prepared to take at least 8x as long (and perhaps substantially longer) for the analysis? Because a minimum of eight images will be needed to create the CT model from which the analysis can be made.

There are definitely x-ray inspection tasks in electronics for which AI can be considered and used today. Is it your application? Or is it as Facebook AI research scientist Edward Grefenstette says,[2] "If we want to scale to more complex behavior, we need to do better with less data, and we need to generalize more." Ultimately, does any of this matter if we accept that AI is only an assistant rather than the explicit arbiter of the test? AI as the assistant may well be acceptable if the confidence level of the result matches or is better than human operators. However, can or should AI be used without such oversight today, or even in the future, based on what can be practically achieved? Whatever the decision, I predict this is likely to give metrologists endless sleepless nights! ❑

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2. Sam Shead, "Researchers: Are We on the Cusp of an 'AI Winter'?," BBC News, Jan. 12, 2020, bbc.co.uk/news/technology-51064369.
3. D-ID, deidentification.co.

Au.: Images courtesy Peter Koch, Yxlon International.

DEFECT OF THE **MONTH**

Locating BGA Joint Failures

Why "dye and pry" is a fast, workable solution.

THIS MONTH WE show examples of testing BGAs with a "dye and pry," a simple and cost-effective way of looking at joint failure or their condition after some form of mechanical testing or abnormal assembly practice.

FIGURE 1 shows a sample BGA joint after dye-and-pry testing. Eighty percent of the separated surface is covered by the red dye. This clearly shows separation occurred before the dye was added.

FIGURE 2 shows a solder ball separated from the pad on the PCB. There is no evidence of dye present. This indicates no cracks were present before the two surfaces were separated. The image also shows how the solder has formed around the pad during reflow like an upturned plate.

Some engineers feel "pry" is a bad method, but it's all about the care used when selecting or performing this test. It can take a few minutes to test parts, so quick results can be obtained in production settings, rather than spending hours in a lab. For those who have been trained correctly, it's not as difficult as some suggest.

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at youtube.com/user/mrbobwillis. ❑

BOB WILLIS
is a process engineering consultant; bob@bobwillis.co.uk. His column appears monthly.

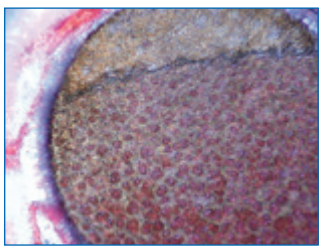

FIGURE 1. Sample BGA joint after dye-and-pry testing.

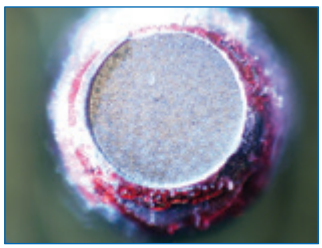

FIGURE 2. A solder ball separated from the pad on a PCB.

Lean Manufacturing and 3-D Printing

Additive processes are an effective tool toward the single-iteration design goal.

IN PAST COLUMNS we've discussed the benefits of strong focus on design for manufacturability (DfM) and assembly (DfA) in the design phase and *poka yoke* or "mistake-proofing" in production. As the cost of 3-D printing technology drops, its usefulness in DfM/DfA and *poka yoke* activities grows. At SigmaTron International, 3-D printers are used in a variety of ways to improve design for assembly and reduce variation. Here we look at ways this technology is used in design, manufacturing and test processes to solve challenges that otherwise add time, cost or defect opportunities.

In SigmaTron's design process, the goal is a single iteration wherever possible. One way that gets accomplished is through peer review of a physical sample of the product. The peer review process usually involves all engineering disciplines, including software development, PCB layout, mechanical, hardware, test engineering and the production team on both the contract manufacturing and customer teams. While 3-D modeling software can provide a representation of the product, 3-D printed parts allow participants in this type of peer review to more easily test assumptions on assembly order of parts and the way parts move in the physical product. SigmaTron's design team frequently uses a 3-D printer to demonstrate how housings and covers will work on new products to help the team visualize the manufacturing and user processes involved.

Another product development benefit is minimalized tooling iterations for designs that aren't fully locked down. In some cases, SigmaTron's design team 3-D prints small quantities of parts for designs that are likely to have engineering changes that will impact hard tooling. When balanced against tooling costs, the 3-D parts are a cheaper option. This path also enables greater flexibility in adjustments to design for assembly or user-friendliness in the early stages of product release when tight deadlines for initial build quantities are involved, since no tooling is involved.

Test fixture design is another area where 3-D printed parts are becoming valuable in solving test challenges. 3-D printing enables custom fixtures for odd-shaped parts and high-mix product families. SigmaTron's design team in Illinois routinely develops unique test fixtures that incorporate 3-D printed parts to solve test challenges in its facilities around the world.

For example, a high-volume control was experiencing high failures in test. The root cause was its odd shape, which made alignment in a test fixture difficult. A redesigned test fixture included a 3-D printed clamp, which had the exact shape of the odd-shaped printed circuit board assembly, along with a rotary knob control that permitted the part to be rotated for a potentiometer test. Printing the clamp was less expensive than fabricating it in plexiglass and accommodated a design that included the rotary control knob. The clamp ensured the unit under test made consistent contact with the test fixture, which eliminated the test failure issue. The redesigned fixture reduced test load and unload time, and the rotating control knob shortened the overall time required to test. The improved throughput met the company goal.

In another example, the team designed a template to support the self-test of a handheld unit. The product had multiple buttons on its faceplate, including one capable of resetting the entire unit. The template covered the reset button to eliminate the possibility of the inspector pressing the wrong sequence of buttons to initiate the self-test.

SigmaTron's team in Tijuana, Mexico, has also been using 3-D printing to *poka yoke* test challenges. In one case, they had a product with 45 variations that utilized a test where voltage was transferred via a connector during test. Six different connector pair variations were among the product types, and confusion about the appropriate connector socket was causing damage and adding time during test. The team designed a 3-D printed six-connector pair exchangeable socket system that enabled 12 units to undergo test at the same time. The socket system had a quick connect/disconnect to the test, making it easy to support different product variations or replace at the end of its usable life. The cost was substantially below the cost to create unique traditional test fixtures.

In another case, product test was accomplished via a tablet app, which scanned a traveler barcode as part of the test process. The team found the time necessary for operators to raise the tablet and align it properly to scan the barcode was impacting throughput. There was also the possibility of tablet damage if the operator dropped it while trying to initiate the test via the app. To address both issues, they designed a 3-D printed fixture that aligned the tablet camera and barcode automatically. The tablet stayed on the fixture, and the travelers could be easily changed.

continued on pg. 43

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VICTOR MENDEZ (below) is manufacturing engineer at SigmaTron in Tijuana; victor.mendez@sigmatronintl.com.

Swag 4.0

Finding our next customer, one trinket at a time.

GREEN IS SEXY. One ignores the wave – in politics, marketing, journalism, social media, commerce – at one's peril. In 2019, *The Economist* published an entire edition raising the alarm about climate change and its implications. Three years ago, Pope Francis wrote an encyclical letter (*Laudato Si*) about the environment, emphasizing care for our neglected "common home." Self-righteous millennials and impressionable younger people march, advocating immediate, drastic control of greenhouse gases and other toxic emissions. A Swedish teenager cuts school and uses her sudden free time to excoriate industrialized nations and big corporations at the UN General Assembly for favoring economic growth over ecological sustainability and contaminating the world, shaming magistrates and captains of industry alike for their perceived callous indifference to the effects of rising temperatures. It is a good time to be a scold.

To be green is to hate waste. Waste is anathema. Angels recycle. Daily. So say those who are woke.

But we are anachronistic, and this is business. We play for keeps.

How do I know? We have swag.

Stuff We All Get. The lovely parting gifts of life. Marketing detritus.

Decades of sales pitches and long-forgotten trade shows have spawned landfills full of useless, incidental stuff, whose avowed aim is to engrave corporate logos and catchphrases into the memory of fleeting visitors, so they'll remember. And buy more stuff, preferably in prodigious amounts. From such numbers are record years made.

That's how it works: GDP fueled by all that stuff-buying. This has been your one-minute economics lesson for today.

Speaking of which, what would the impact be if swag ceased to exist? Where would the resulting impoverishment hit hardest? Would the Third World slide to the Fourth World, or maybe the Fifth? Would some future anthropologist one day stumble upon a great burial mound of unused corporate paraphernalia hidden deep within a primeval forest, a monument to our industry's wasteful self-promotion? Voilà: Swaghenge.

Who started this? Why do we do it?

Long before Bernie Sanders championed free stuff in exchange for votes, there was swag.

Were souvenir party favor pitchforks given out at the Salem witch trials? Did the Dreyfus Affair sport plaintiff and defense team tables hawking pocket watches or *pince-nez*, festooned with the respective barristers' coats of arms? What did a Spanish Inquisition tote bag tote?

Like a birthright, full of contradictions. Like pens, candies, and Post-it notes telling us to recycle, sponsored by ExxonMobil. Or commemorations of the Doolittle Raid on graph paper, courtesy of Sony.

Flash drives. Keychains. Pens (always pens). Memo pads. Tote bags (plastic, paper and cloth). Hand sanitizer. Squeeze toys. Coffee mugs (for driving and for home). Eyeglass cleaner. Letter openers. Mousepads. Lanyards. Penlights. Notebooks. Water bottles. Tool sets. Lab books. Magnetic paper clips. Logo golf balls. Beer koozies. Candy. Endless candy. Even drones with sensors and cameras attached, to give an Industry 4.0 spin. Swag adapts with the times. Swag is forever.

Because when you chomp down on that chocolate, you as chompee will remember indelibly by your indigestion – how's that for big data – where it came from and align your purchasing decisions accordingly.

Repetition is marketing. Marketing, with its generally dim view of human nature, presumes short attention spans. Put the message out there incessantly, and customers will remember your company when the time comes for real requirements.

Put the message out there relentlessly because it's in the ad agencies' best interest you do so. (Translation: It's about money.)

Repeat the message three times, and you seal the deal. So much the better if it's embossed on a beer koozie, and the message brings warm greetings during Happy Hour. You remember.

But will those involuntary recipients remember the right things and think favorable thoughts, induced by our pitch? Remember Peloton? Does ad repetition, in print or on trinkets, really matter in sales, or just inflame prejudices?

Are we stupid or just stupefied?

This puts the "gross" in "gross national product."

Do customers really remember you for that ICBM-shaped athletic water bottle?

I can take a swag at it. As in, "Stupid Wild-Ass Guess."

No.

Personal misgivings aside, our company is far from innocent. At the risk of being annoying, we too fear missing out. We have tote bags and pens. Ours are cool, however; they are worth remembering.

This much remains true: We have yet to secure a new customer who was first attracted to us by our

ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.

innovative pen design. (Maybe someday.)

How do we know? Our company reviews its list of new customers at the end of each year. One big reason is to find out how they found us. Overwhelmingly, new customers seek us out through three media:

1. Sales representative activity
2. Internet searches
3. Personal referrals.

The first source is self-evident. Reps know their territory. It's their job to know who needs what service. They make the initial contact, or get the first call, and relay the request. We take it from there, handling all the technical and administrative details. The rep gets the credit when commissions are released.

Often a rep-referred opportunity comes to us first in the form of a "can you do this" inquiry. Yes or no is the expected answer. Recently, a customer making security systems faced a recall due to a malfunctioning sensor. Our local rep got the first panic call; we got the second from him. Two weeks – and hundreds of x-rays – later, it was my unfortunate duty to report the basis for a recall was justified. Another rep referral went from phone call to NDA to x-raying boards within 36 hours. I came to work on a Monday in total ignorance of this company, their business, their associated products, or their attendant problems. By Wednesday we were x-raying their boards. By Thursday we were sending them results and a bill for services rendered.

Internet searches come via the well-known search engines and optimization algorithms. Specialized online directories such as ThomasNet and others are productive sources as well. A prospective client types in the right keywords, and our name rises to the top of the list. In comes the RFQ.

We get two or three Internet-based inquiries a week, either through our website or direct via phone and email. Last week a customer Googled "flying probe test services" and got us. We are quoting their business now. Another Googled "CT scanning" and up we came. Parts are on the way for inspection as I write this.

Personal referrals happen when Engineer A at Company X changes jobs and goes to Company Y, bringing us with them. Or Engineer B has friend Engineer C working at Company Z; the latter has a problem and asks her friend for help with a referral. We get the call.

We have some specific and unique flying probe test capabilities, a combination of technical wherewithal and long experience. Hard to explain; those in the know simply know we have the requisite skills. So, we get unusual requests. Last month it was a request for programming using an older, nearly obsolete operating system. We have those skills, and the customer had the need. The project and the moment met. Likewise, a colleague was asked recently if they knew of someone who could provide CT scanning services for large objects (not PCBAs). The colleague immediately remembered us and made the referral. We had a new customer within one day of the first contact. A third client wanted high-density wafers to be probed to a very small (sub-70µm) placement size. A friend of a friend referred the customer to us.

Sometimes it boils down to this: Either you can do the job, or provide the service, or you can't. End of discussion. This can be especially true when time is of the essence and alternative solutions are limited or nonexistent. At those moments, tag lines, banners, and slick sales pitches are irrelevant. Can you solve the customer's problem, or can't you? No swag required.

Networks beat trinkets every time. So why do we still hand out logo-ized tchotchkes?

Blame the PR people. Being experts, they assume the least common denominator in humanity and expect a natural propensity among humans to forget those they talked with, whether on the phone, by email, or in person at meetings or trade shows. Hard swag prevents us from declining into obscurity. He or she who shouts the loudest and longest with the mostest, most often, gets the reward. Give 'em something to trip over.

Last week I spoke with a new customer interested in flying probe test engineering. As is my habit, I asked him how he found us. He volunteered that our company first came to his attention through reading these columns. He found resonance in the content and wanted to explore doing business with the author.

Well now.

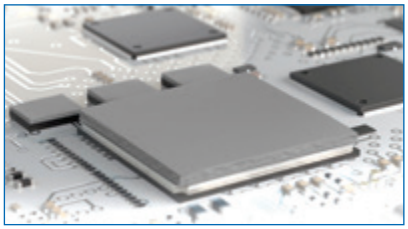
Media swag. What a brilliant idea! We need more sources like this. Glad I thought of it! ▫

Getting Lean, continued from pg. 41

Throughput goals were achieved, and risk of damage to the tablets through excess handling was eliminated.

Production fixturing is a final area where 3-D printing is helping solve challenges. While it isn't an option for high-heat processes, it is a good option for odd-form, nonwettable part masking in conformal coating. Printed masking caps and boots are a less expensive option than third-party tooling and require less lead-time. They are also faster to install and remove than other forms of manual masking.

Using 3-D printed parts to sanity-check design assumptions, increase flexibility in product development timelines or address unique challenges in manufacturing or test is often the simplest, fastest and lowest-cost option. In some cases, the ability to configure unique shapes and interfaces adds levels of functionality not possible with traditional fixturing options. In many cases, the ability to fabricate a one-off solution permits levels of customization that are otherwise not cost-effective. ▫



HIGH-POWER TIM

Bergquist Gap Pad TGP 10000ULM provides thermal conductivity of 10.0W/m-K within ultra-low modulus, low assembly stress formulation. Soft, high-compliance pad conforms to irregular surfaces, fills small gaps to enable interface wet-out and optimal thermal transfer.

Henkel
henkel-adhesives.com

5-D SPI

ProcessLens measures solder paste deposits and controls and optimizes printing process autonomously while learning with each print cycle. Determines matching print parameters and runs virtual prints to check parameters for the stencil design. X/y positioning accuracy is 12.5µm.

ASM
asm-smt.com

HUMIDITY/TEMP. METERS

GNV-720 and GNV-725 are portable, dual-function meters with three environmental sensors. Offer precision capacitance and semiconductor sensors incorporated directly into the remote wand. Thermocouple sensor adds accuracy.

Global Specialties
globalspecialties.com

OTHERS OF NOTE

ADVANCED JITTER ANALYSIS

R&S RTO-/RTP-K133 advanced jitter analysis option for R&S RTO and R&S RTP oscilloscopes separates jitter into random and deterministic components and views results flexibly for debugging. Separates individual components of jitter, such as random jitter, and deterministic jitter components, such as data-dependent and periodic jitter.

Rohde & Schwarz
rohde-schwarz.com

PROGRESSIVE CAVITY PUMPS

797PCP and 797PCP-2K deliver fluid volumes as small as 0.01mL per revolution. Deposit volume tolerances equal to +/-1%. Core components (rotor and stator) form sealed metering chamber. As it rotates, pump allows continuous volumetric dispensing unaffected by external factors such as changes in viscosity, fluctuating fluid pressure, and the full-to-empty effect in syringe barrels.

Nordson EFD
nordsonefd.com

UNIVERSAL FLUXING AGENT

EO-B-011B flux concentrate is low-solids and suitable for wave, selective and manual soldering. Complies with DIN-EN 61190-1-1: L0. Contains organic, halogen-free activation additives with synthetic resin in a combination coordinated to thermal requirements of soldering processes. Can be applied by brushing, spraying, dipping, etc. Solids content is 3%. Corrosion-free.

Emil Otto
emilotto.de

INLINE SOLDERING ROBOT

TMT-9900S inline soldering robot is designed to be incorporated into SMT production line where precision soldering is key. Includes vision/mapping and dynamic laser height control. Incorporates same IP software used on benchtop system.

Thermaltronics
thermaltronics.com

2-PART EPOXY, SEALANT

EP62-1AO has a working life of 12-14 hr. at ambient temp. for a 100gm mass. For bonding and sealing large or intricate parts that may need ample time for mixing and applying. Tensile modulus of 600,000 to 650,000psi and tensile strength of 5,000 to 6,000psi. Service temp. range -60° to +450°F.

Master Bond
masterbond.com

HIGH-SPEED AXI

TR7600F3D SII 3-D AXI reportedly achieves speeds 2x to 3x as fast as previous-generation models. Is equipped with high-res flat panel detector. Can inspect large boards up to 900mm x 460mm.

Test Research
tri.com.tw

IOT/5G ICT

i3070 series 6 supports range of PCBA sizes for applications including IoT and 5G, as well as automotive and energy. Delivers short signal path between measurement circuitry and devices under test to minimize undesired effects from parasitic capacitance, improve immunity to crosstalk, and eliminate stray signal coupling effects. Features improved test efficiency with up to 4x faster boundary scan, silicon nails and dynamic flash programming; minimal downtime for software installation with 100% backwards compatibility.

Keysight Technologies
keysight.com

MICRO MATERIALS TESTER

Prospector enables full characterization of any device by combining mechanical testing with electrical, thermal, acoustic and optical. Tests across coatings and thin films, medical devices, microelectronics, and more. Gains failure mode insights. New applications include hardness and scratch testing.

Nordson Dage
nordson.com/en/divisions/dage

98K CPH CHIPSHOOTER

YRM20 chipshooter uses two head types: a high-speed, multi-purpose rotary head that, when combined with the high-speed feeder, delivers performance under optimal conditions of 115,000cph, as well as a one-head solution via inline (HM) head. Mounting accuracy of ±25µm (Cpk ≧ 1.0); supports 0201 (0.25mm x 0.125mm) sized component packages. 98,000cph.

Yamaha Surface Mount Technology
yamaha-motor-im.eu

OTHERS OF NOTE

SMEMA-COMPATIBLE MES

FactoryLogix 2019.1 has more than 100 enhancements: improved screen layout; enhanced attachment capabilities; ability to transfer assemblies and all product device history, including all trace and quality data; automated replenishment and reordering, delta kitting, and automated quality inspection switching rules. inForce 2.0 interacts with SMEMA-compliant equipment for production line control.

Aegis Software
aiscorp.com

PORTABLE OPERATOR INTERFACE

TTC Go! is redesigned for Android 7+ supported mobile devices. Simplifies production tasks. Has intuitive navigation features. Context-driven interface guides user to achieve simple tasks with as little clicks, data entry or scanning steps as possible. Runs over Windows and Android platforms.

Cogiscan
cogiscan.com

AUTOMATIC PISTON SOLDERING

MPC KL integrates collaborative robot and soldering irons from JBC or Hakko. Comes with automatic tip changer and optional kinematic system. Soldering iron is fixed to arm of robot, including sensitive wire feeder, to create single unit. Optional rotary indexing table for manual component assembly and safety cell surrounding soldering process.

Eutect
eutect.de

LASER-CUT STENCILS

Alpha Cut HR2 retains shape, positional accuracy and wall quality associated with standard Alpha Cut material; has improved print definition and reduced variation in solder deposits. Made from hardened stainless steel that enables improved resistance to stretching under high tension. Drop-in compatibility.

MacDermid Alpha
MacDermidAlpha.com

ULTRASONIC SPRAY COATING

FlexiCoat EMI is designed for conformal spraying of EMI shielding material onto semiconductor packages. Is an automated x-y-z coating engineered to spray copper and silver-filled shielding materials with control of coating characteristics and little overspray. Integrated nozzle provides targeted spray area.

Sono-Tek
sono-tek.com

LARGE-AREA AOI

LX-1000 offers 630mm x 630mm inspection area with single-or dual-sided imaging. Has full travel imaging sensors. Offers high-speed PCB inspection with exceptional defect coverage. Inline.

YesTech
nordson.com/en/divisions/yestech

In Case You Missed It

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

Low-Power Transistors

"Uniform and Ultrathin High-κ Gate Dielectrics for Two-Dimensional Electronic Devices"

Authors: Weisheng Li, *et al.*

Abstract: Two-dimensional semiconductors could be used as a channel material in low-power transistors, but the deposition of high-quality, ultrathin high-κ dielectrics on such materials has proved challenging. In particular, atomic layer deposition typically leads to nonuniform nucleation and island formation, creating a porous dielectric layer that suffers from current leakage, particularly when the equivalent oxide thickness is small. Here, the authors report the atomic layer deposition of high-κ gate dielectrics on two-dimensional semiconductors using a monolayer molecular crystal as a seeding layer. The approach can be used to grow dielectrics with an equivalent oxide thickness of 1nm on graphene, molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2). Compared with dielectrics created using established methods, these dielectrics exhibit a reduced roughness, density of interface states and leakage current, as well as an improved breakdown field. With the technique, the authors fabricate graphene radio-frequency transistors that operate at 60GHz, and MoS_2 and WSe_2 complementary metal-oxide-semiconductor transistors with a supply voltage of 0.8V and subthreshold swing down to $60 mV\,dec^{-1}$. They also create MoS_2 transistors with a channel length of 20 nm, which exhibit an on/off ratio of over 10^7. (*Nature Electronics*, December 2019, nature.com/articles/s41928-019-0334-y)

PCB Recycling

"Debromination and Decomposition Mechanisms of Phenolic Resin Molecules in Ball Milling with Nano-Zerovalent Iron"

Authors: Xi Chen, Jie Zhu, Jujun Ruan, Ye-tao Tang and Rong-liang Qiu

Abstract: Nonmetallic particles from waste printed circuit boards are toxic pollutants due to their brominated flame-retardant content. Developing green technology for the disposal of nonmetallic particles is a significant task. To the authors' knowledge, this paper might be the first to report the ball milling of nonmetallic particles with nano-zerovalent iron. The results indicate the content of bromine on the surface of nonmetallic particles ball-milled with nano-zerovalent iron was reduced by 50%. Phenolic resin macromolecules were decomposed to methylbenzene, phenol, etc., and graphitic carbon and amorphous carbon appeared. The reason for the decomposition of phenolic resin molecules was presented. Nano-zerovalent iron, as an electron donor, transferred electrons to pentabromodiphenyl ether molecules during ball milling. The C-Br bond was stretched, and the bond length increased, which promoted the debromination process. The authors also found that in the pentabromodiphenyl ether molecule, the C-Br bond in the para position on the benzene ring with more Br atoms and the C-O bonds were broken first. Additionally, the reaction pathway from resin macromolecules to methylbenzene and phenol etc. was presented and discussed. This paper provides a detailed mechanism by which ball milling achieves the decomposition of brominated flame-retardant molecules.

(*ACS Sustainable Chemical Engineering*, December 2019, https://pubs.acs.org/doi/full/10.1021/acssuschemeng.9b05071)

Underfill

"Filling Efficiency of Flip-Chip Underfill Encapsulation Process"

Authors: Fei Chong Ng, Mohamad Aizat Abas and Mohd Zulkifly Abdullah

Abstract: The authors aim to introduce an indicative parameter of filling efficiency to quantify the performance and productivity of the flip-chip underfill encapsulation process. Additionally, the variation effect of the bump pitch of flip-chip on the filling efficiency was demonstrated to provide insight for flip-chip design optimization. Filling efficiency was formulated analytically based on the conceptual, spatial and temporal perspectives. Subsequently, the effect of bump pitch on filling efficiency was studied based on the past actual-scaled and current scaled-up underfill experiments. The latter scaled-up experiment was validated with both the finite volume method-based numerical simulation and analytical filling time model. Moreover, the scaling validity of scaled-up experiment was justified based on the similarity analysis of dimensionless number. Through the scaling analysis, the current scaled-up experimental system is justified to be valid since the adopted scaling factor 40 is less than the theoretical scaling limit of 270. Furthermore, the current experiment was qualitatively well validated with the numerical simulation and analytical filling time model. It is found that the filling efficiency increases with the bump pitch, such that doubling the bump pitch would triple the efficiency. (*Soldering & Surface Mount Technology*, January 2020, emerald.com/insight/content/doi/10.1108/SSMT-07-2019-0026/full/html).

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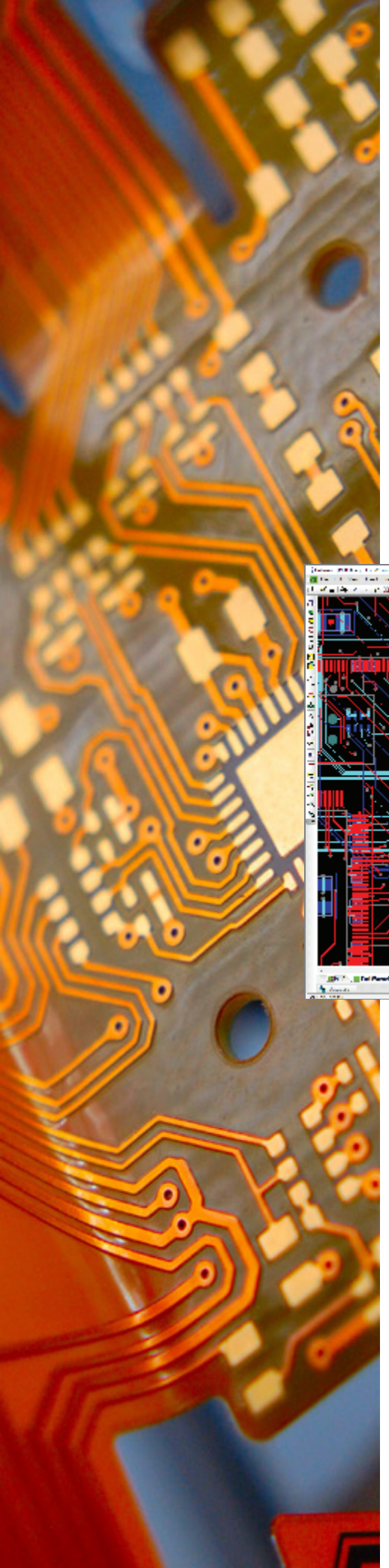

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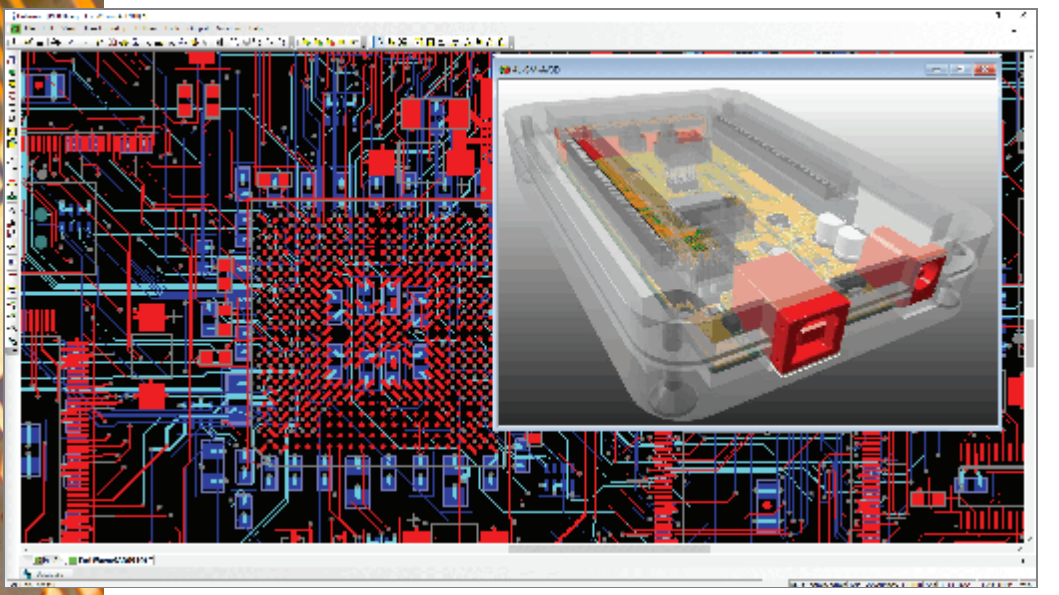

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