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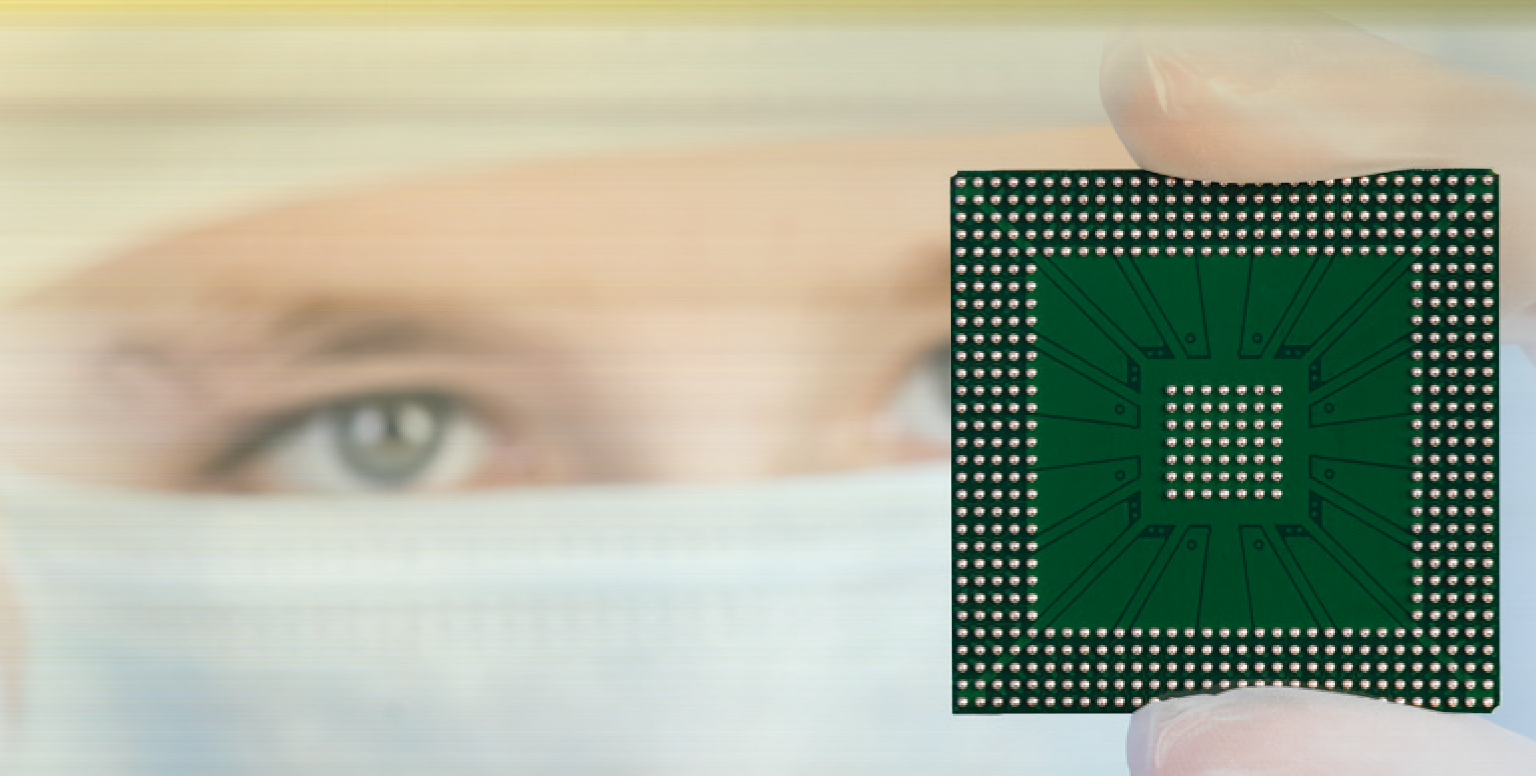
APRIL 2020

NPI Awards
SEA Awards

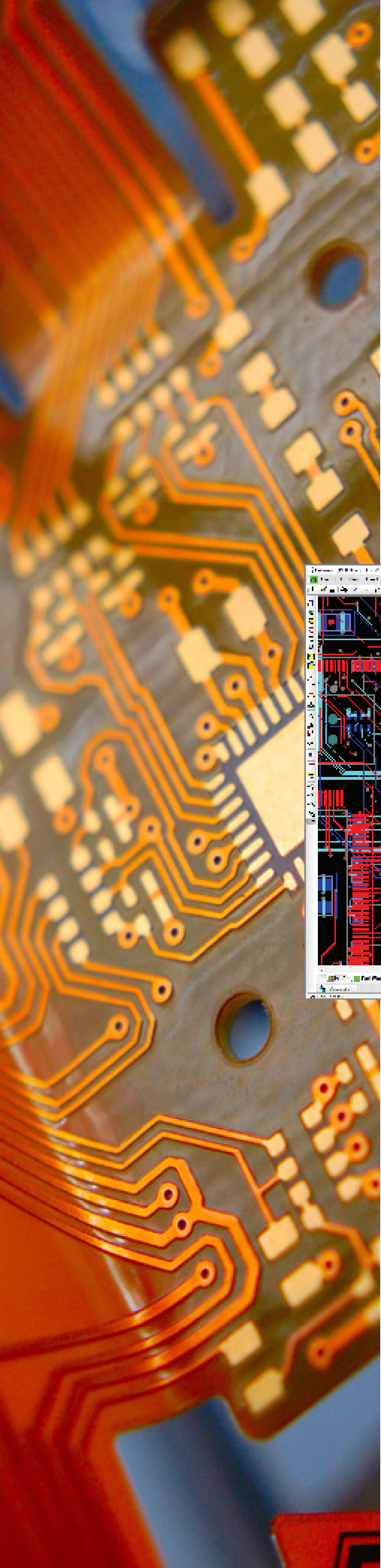


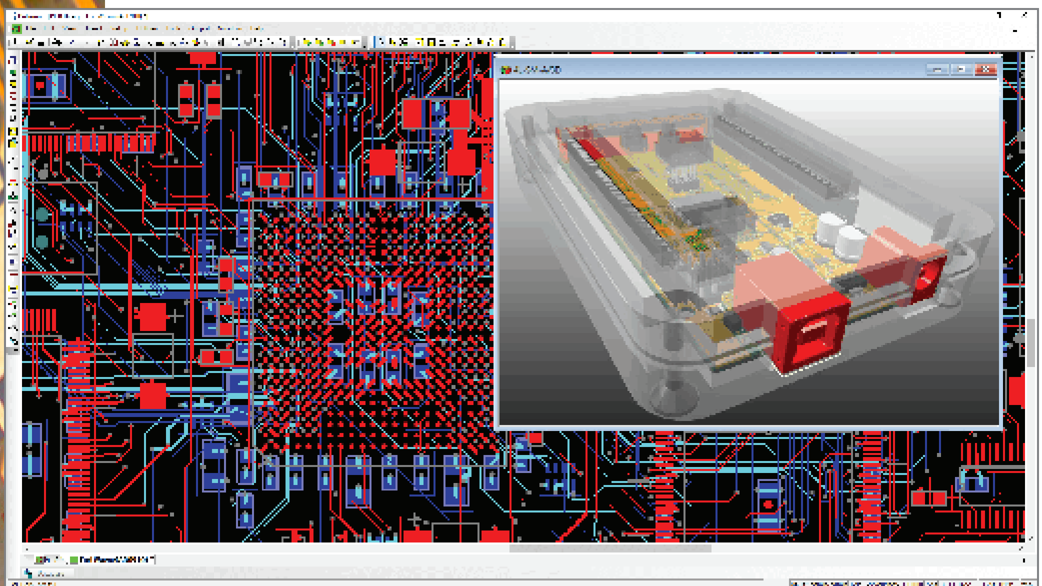
What **Fine-Pitch BGAs** Mean for **Fabrication**

Time and Frequency Domain

Making Flex Stiffer

Vapor Degreasing





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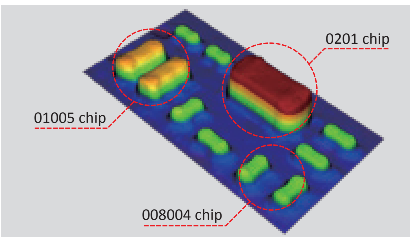
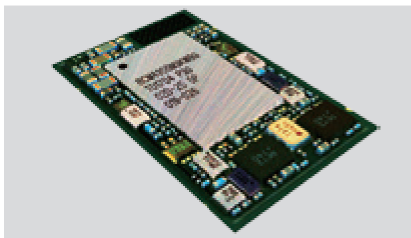
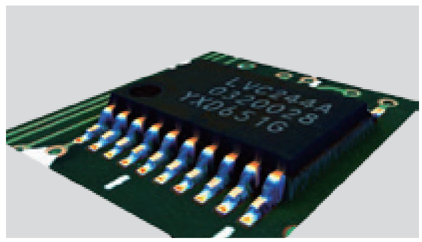


008004 Chip



Specular Die



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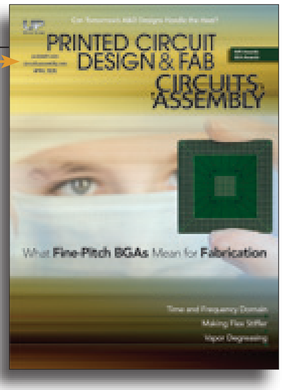

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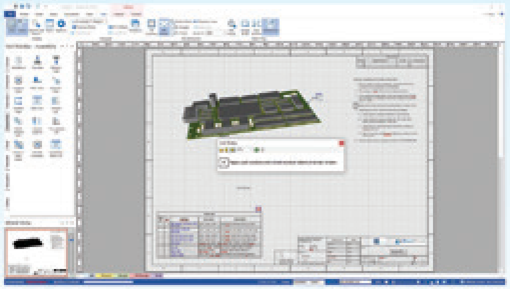

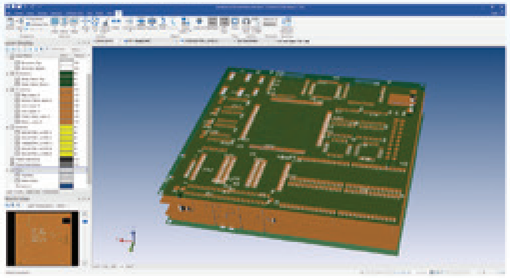

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MIKE BUETOW
EDITOR-IN-CHIEF

Will Mass Shutdowns Spur More Action?

REMEMBER 2010? That year, a massive earthquake in the Pacific Ocean led to a tsunami of biblical proportions. Much of Japan's semiconductor and electronics manufacturing industry was taken offline for nearly two months.

About 12 months later, it was Thailand's turn in the wringer. The so-called 100-year floods swamped most of the country, causing nearly $50 billion in damage. In doing so, they took out key assembly operations at Fabrinet, Benchmark Electronics, Kimball and SVI, among others, upsetting a key link in the auto electronics and optical component supply chains.

Covid-19 has hit the electronics supply chain with all the force of those two natural disasters. The industry response will be fascinating.

This is the ultimate stress test. Coming on the heels of the Chinese New Year, where employees had not yet returned to work, the shutdown lasted four to six weeks in China. It's a double whammy.

Not to diminish the very real and devastating aspects of Covid-19, but the industry has been building or attempting to build in preventative and protective measures for years, and I am eager to see how these plans play out.

I expect wild swings. Not on the level of what happened following the natural disasters in Thailand and Japan, of course. In those instances, auto production in Japan alone jumped 20% the first year after the earthquake, as consumers replaced their destroyed vehicles, then plunged to 1.3% growth the following year. In this case, some inventories will be depleted, but replacement of end-products won't be a driver. Most national economies have been puttering along for the past several years. This won't help. The loss of wealth due to crashes in most of the world stock exchanges, coupled with the loss of income due to worker furloughs or layoffs, will stifle some of the demand that will be needed to revive factories to full capacity. In crisis situations, consumers buy staples. Just look at your local Wal-Mart: Plenty of TVs and PCs can be found, but the food and paper goods aisles are cleaned out.

Going back to my start in the industry in 1991, just-in-time inventory management was in vogue, at least among consulting circles. (The actual shop floor was another matter.) Software capable of tracking and traceability was just starting to appear. Most inventory controls were primitive, however. Visibility outside the factory was limited.

Fast forward to 2000. I recall a long talk with the head of Viasystems' supply chain, whose stated goal – besides becoming the dominant player in electronics manufacturing – was to be able to see five layers in either direction, basically from the mines all the way to the landfill. Neither vision was met.

Likewise, we've heard for years about the promise of concurrent engineering. Yet, due to various governmental, networking and patent constraints, distributed engineering is far less common than it could be.

And I've been through at least three major component inventory crises, in one case where parts were in such short supply major assemblers were openly searching for available spares on social media. Yikes.

I've often felt our industry has the best finance managers around. How else can they stay alive on miniscule margins in a cash-intensive industry known for slow payments? Still, the Electronic Components Industry Association (ECIA) says 70% of the component manufacturing sites in China were affected by Covid-19. Most have only two to three months of cash in reserve, ECIA added. Their financial acumen – and resolve – will be supremely tested.

I have many questions over what might happen in the coming months:

- Will this spur the industry to lessen its dependence on China?
- If so, where will production migrate?
- What will be the impact on inventory levels? Will this cue a new trend toward higher inventories?
- Can companies whose balance sheets have been disrupted by unplanned shutdowns afford to take on higher stock levels?
- Will nations and companies be inclined to ease controls over digital data transfer and bring networking capabilities up to par? And what are the IP implications of doing so?

Inventory decisions are cyclical. Historically, when the industry has been faced with supply issues, it responds by raising stocks. We've been better at it of late. Two years ago we stared down a worldwide undercapacity situation and didn't lose our minds.

Surely we will study and learn from this shutdown. For a change, I think we are well-positioned to weather the initial storm. My gut tells me supply chains are unlikely to up and move due to Covid-19, because unlike earthquakes and typhoons, when it comes to pandemics there is nowhere to hide.

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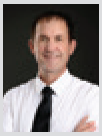
PCDF People

Dyconex named **Dr. Selcuk Mentese** head of quality management.

IPC presented **Mike Carano**, **Bhanu Sood** and **Udo Welzel** with the Dieter Bergman Fellowship award.

Susy Webb in June will lead Design Essentials for PCB Engineers, a two-day workshop covering parts placement, routing, fine-pitch BGAs, fanout, controlling impedance and high-frequency energy, and stack-up and power issues, in Austin, TX.

Taiyo America announced **Frank-Ralf Mayer** as European sales manager. He was a logistics and sourcing consultant with Cronos for 18 years prior to joining Taiyo.



Uyemura named **Troy McNulty** Midwest technical sales manager in Minnesota, Wisconsin, Illinois and Michigan. He has held technical sales positions with OMG/ MacDermid and was business development manager for Paradigm. He has more than two decades' experience in research/formulation, sales, and technical service related to electrochemicals.

PCDF Briefs

Celus (formerly Contunity) has announced a €1.7 million seed round that will fuel the company's ambition to turn simple plans into complex PCB designs in 90% less time.

DSBJ will invest $42 million to expand flexible PCB production for 5G applications.

IPC bestowed its highest corporate honors on two IPC member companies: **TTM Technologies** and **Continental Automotive**.

Kyocera and **AVX** have entered into a definitive merger agreement under which Kyocera will acquire all outstanding common shares of AVX.

Leading-edge chipmakers, foundries and EDA companies are pushing into 3nm and beyond, and are encountering a long list of challenges that raise questions about whether the entire system needs to be shrunk onto a chip or into a package.

Mitsubishi says it developed a <3cm-thick high-bandwidth aircraft antenna by incorporating the antenna elements, the RF combiner and the RF-ICs into a single circuit board.

Multicircuits is among the fabricators embracing automation and other Industry

TTM Opens New Manufacturing Facility in WI

CHIPPEWA FALLS, WI – TTM Technologies in January opened a state-of-the-art PCB manufacturing facility here, its second in this Midwestern US state.

The world's second largest fabricator invested $15 million in the new plant. It spent seven months converting the site from a warehouse.

"We took a 20-year-old, 40,000 sq. ft. building that was being used as a warehouse, and we turned it into the most technology advanced PCB building in the United States," said TTM Technologies president and CEO Tom Edman, in a statement.

The plant was outfitted in part with equipment and assets from TTM's acquisition of Endicott, NY-based i3. The company told local media it wanted to keep the acquired technology in the US.

About 40 staff members now work in the advanced technology center, along with some 600 employees at the 240,000 sq. ft. site nearby, which TTM acquired from Honeywell in 2002. That site was expanded in 2004.

Production began at the new plant Jan. 4. – *CD*

PCB West 2020 Exhibition Floor Sold Out for 9th Year in a Row

ATLANTA, GA – The exhibition floor for PCB West is sold out for the ninth straight year, UP Media Group announced. The annual show, the largest conference and exhibition for printed circuit design, fabrication and assembly in the Silicon Valley, returns to the Santa Clara (CA) Exhibition Center on Sept. 8-11.

PCB WEST
Conference & Exhibition

The event includes a four-day technical conference and one-day exhibition. The September 2019 event attracted more than 2,500 registrants.

"We are pleased to announce the exhibition floor for PCB West is sold out for the ninth straight year," said Frances Stewart, vice president of sales and marketing, UPMG. "Our exhibitors continue to count on us every year to deliver an outstanding event and targeted audience."

Now in its 29th year, this year's show will feature 110 booths showcasing the leading companies in the PCB industry, including the top CAD and CAM vendors and top names in printed circuit fabrication and electronics assembly.

For information about attending, visit pcbwest.com. – *MB*

Report: Large-Area FO Remains 'Hot Topic'

AUSTIN, TX – Large-area fan-out remains a hot topic in the industry, according to TechSearch International.

The main driver for large-area FO panel development is cost-reduction because more parts can be processed in a batch, according to the firm's recent report, which divides the panel market into high-density RDL (≤2µm L/S with multiple RDLs) versus low-density (>5µm L/S with ≤3 RDLs).

The report discusses FO-WLP panel activities at major companies and reports on consortia progress and future plans. Applications for large-area panels are discussed. A market forecast is provided for low-density panels, and panel capacity is included.

The report examines the packages inside Huawei's Mate 30 5G to see how Huawei has been able to use fewer US components. Recent announcements of high-performance package offerings from TSMC are described. Trade-offs in high-performance packaging are discussed.

Quarterly and annual OSAT financial trends are presented. One section examines EMI shielding offerings and applications. – *CD*

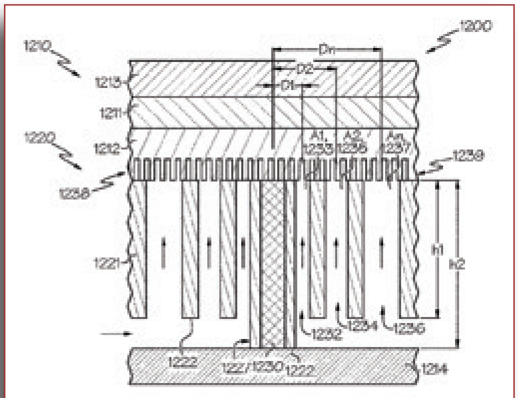
Toyota Devises Novel Power Electronics Cooling Method

ERLANGER, KY – A pair of Toyota Motor Engineering & Manufacturing engineers have been issued a US patent for a novel method for cooling power electronics inside printed circuit boards.

In the filing, Yuji Fukuoka and Ercan Dede describe an electronics assembly that includes a cooling chip structure with a target layer and a jet impingement layer coupled to the target layer. The jet impingement layer has one or more jet channels disposed within the jet impingement layer. Further, one or more through substrate vias are disposed within the jet impingement layer, where the substrate vias are electrically conductive and electrically coupled to the target layer.

A fluid inlet port and a fluid outlet port are fluidly coupled to the one or more jet channels of the jet impingement layer.

The engineers wrote in their application that higher power electronic devices overwhelm conventional heat sinks. The placement and integration of conventional heat sink and cooling structures also present a challenge, they add, and require additional bonding layers and thermal matching materials such as bond layers, substrates and thermal interface materials, which add "substantial thermal resistance" to the assembly. "Accordingly," they wrote, "a need exists for alternative power electronic assemblies and power electronics devices having cooling structures that also provide electrical interfaces."



The Toyota engineers conceived a pair of alternatives. "In one embodiment, an electronics assembly includes a cooling chip structure having a target layer, a jet impingement layer coupled to the target layer, the jet impingement layer having one or more jet channels disposed within the jet impingement layer, and one or more through substrate vias disposed within the jet impingement layer. The one or more substrate vias are electrically conductive and are electrically coupled to the target layer. The electronics assembly includes a fluid inlet port and a fluid outlet port that are fluidly coupled to the one or more jet channels of the jet impingement layer.

"In another embodiment, an electronics assembly includes a cooling chip structure having a target layer with a plurality of fins defining a plurality of microchannels. Further, the electronics assembly includes a jet impingement layer coupled to the plurality of fins of the target layer, the jet impingement layer having a plurality of jet channels disposed within the jet impingement layer and a plurality of through substrate vias disposed within the jet impingement layer. The plurality of through substrate vias is electrically conductive and is electrically coupled to the target layer. A first jet channel of the plurality of jet channels is closer to a first through substrate via of the plurality of through substrate vias than a second jet channel of the plurality of jet channels. The first jet channel has a first cross-sectional fluid area that is smaller than a second cross-sectional fluid area of the second jet channel. The electronics assembly includes a fluid inlet port and a fluid outlet port that are fluidly coupled to the plurality of jet channels of the jet impingement layer."

The US patent number is 10566265, and it was issued Feb. 18, 2020. – *MB*

4.0 technologies, having installed three drills that require only a single operator to run simultaneously.

Nano Dimension moved its headquarters for the Americas to Boca Raton, Florida.

Shennan Circuits expects to complete its second-phase development of its Nantong production base in Jiangsu province by the end of March, which will increase annual PCB capacity by 580,000 sq. m.

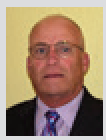
Trackwise Designs received its first production order for its flexible printed circuit technology, worth about £600,000.

Transistor count trends continue to track with Moore's law, a new report from **IC Insights** finds.

Wus now operates three production bases with one each in Kunshan, Shanghai and Huangshi. Its Kunshan plant has an annual capacity of 2.2 million sq. m., and PCBs with over 16-layer counts account for over 50% of the output, mainly for telecommunication equipment applications.

CA People

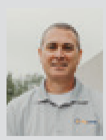
Asscon named **Tobias Tuffentsammer** head of sales in Germany.



Inovar named **Joe Barber** chief engineer, Logan Aerospace & Defense division. He held senior technical and leadership roles in electrical systems engineering and manufacturing for 40 years at Raytheon.

IPC presented four volunteers with its annual President's Award: **Michael Ford**, Aegis Software; **Dale Lee**, Plexus; **Joe O'Neil**, Green Circuits; and **S. Manian Ramkumar**, Ph.D., Rochester Institute of Technology.

IPC presented **Gaston Hidalgo**, **Kate Stees**, **Stephanie Rodgers**, and **Zhiman Chen** with its Rising Star Award.



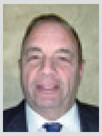
KeyTronic promoted **Duane Mackleit** to vice president of operations. He has been with the EMS company since 2008.

MicroCare promoted **Jerald Chan** to managing director, MicroCare Asia.

Prism Electronics named **Mary Wells** customer account manager.

Sanmina promoted **Richard Henrick** to senior quality engineer.

SMTA named **Greg Vance** interim president after the current president resigned due to a job change.



Takaya appointed **Mike Casper** group applications engineer. He spent 15 years in customer support for flying probe and functional test applications at Seica, and 20 years developing functional test hardware and software for a number of companies and product types.

TopLine CEO **Martin Hart** has been awarded a US patent for a fixture designed to deliver 1752 solder columns onto a substrate as part of the Ceramic Column Grid Array (CCGA) assembly process.

Weller Tools promoted **Dyan Reagan** to West Regional Manager.

CA Briefs

A provision that allows the use of standard datasheets for electronic components when reporting to the automotive industry's material declaration system, IMDS, will be removed on Jul. 1.

Absolute EMS purchased a **Sayaka** SAM-CT23S tabletop router from **Seika Machinery** and a **Nordson Dage** Quadra 3 x-ray inspection machine.

AIM Solder expanded its research and development laboratory in Montreal.

Asymtek expanded distributor **Neutec Electronic's** territory to the French-speaking areas of Switzerland.

AW installed a **Yamaha** YSP screen printer.

Celestica will lay off some 450 people at its Romanian subsidiary, according to reports.

CheckSum is partnering with the **Adaptsys Group** to sell its in-circuit test solutions in Europe.

Computrol purchased an **Asys** Serio 4000 solder paste printer.

Critical Manufacturing appointed **Process Automation & Tool** representative in Kentucky, Tennessee, Alabama, Mississippi and Georgia.

Cyient opened a wire harness lab in Peoria, IL.

India's Department for Promotion of Industry and Internal Trade said foreign retailers can now meet local sourcing requirements by buying goods produced in units in Special Economic Zones, a decision that should benefit ODMs like **Wistron** and **Foxconn**.

EnviroLeach Technologies completed preliminary lab-scale testing on the recovery of tin metal from PCB material.

U of I Researchers Demonstrate New Capability for Electronics Cooling Using Additive Manufacturing

URBANA, IL – For decades, researchers have considered the potential for cooling hot electronic devices by blowing on them with high-speed air jets.

However, air jet cooling systems are not widely used today. Two of the biggest obstacles that prevent the use of these systems is their complexity and weight. Air jet systems must be made of metal to be able to handle the pressure associated with air jets whose speed can exceed 200 miles per hour. And the air handling system can be complex with many discrete components that manage the air flow and direct the air onto the hot spots where cooling is required.

Now, researchers at the University of Illinois at Urbana-Champaign have demonstrated a new type of air jet cooler that overcomes previous barriers to jet cooling systems. Using additive manufacturing, the researchers created an air jet cooling system in a single component that can direct high-speed air onto multiple electronics hot spots. The researchers manufactured the cooling system from strong polymer materials that can withstand the harsh conditions associated with high-speed air jets.

"The design freedom of additive manufacturing allows us to create cooling solutions that have sizes and shapes not previously possible," said William King, Andersen Chair and Professor of Mechanical Science and Engineering. "This really opens up a new world of opportunities for thermal management."

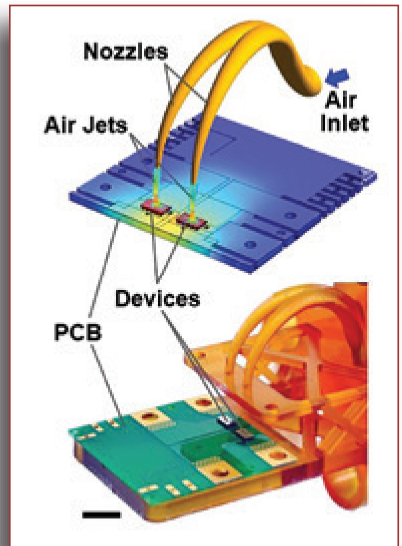


FIGURE 1. Schematic (top) and a photograph (bottom) of additively manufactured nozzles showing how the impinging jet cools working GaN devices on a PCB. The scale bar represents 10mm.

The research focused on heat removal from high-power electronic devices. "The acute thermal management problems of high-power electronic devices appear in a host of applications, especially in modern data centers, as well as electric vehicles including aircraft, automotive, and off-road vehicles," said Nenad Miljkovic, Associate Professor of Mechanical Science and Engineering at Illinois and coauthor on the published research.

The applications of high-power electronic devices are growing rapidly – in electric cars, solar power systems, 5G communications, and high-power computing utilizing graphics processing units (GPU), to name a few. The electronic devices in these systems generate heat that must be removed for effective and reliable operation. In general, higher power results in higher performance. Unfortunately, higher power also makes it more difficult to remove the heat. New cooling technologies are required to support the growth of electric systems.

The paper, "Air Jet Impingement Cooling of Electronic Devices Using Additively Manufactured Nozzles," was published in the journal *IEEE Transactions on Components, Packaging, and Manufacturing Technology*. Authors include Beomjin Kwon (now an assistant professor at Arizona State University, graduate students Thomas Foulkes and Tianyu Yang, and Professors Miljkovic and King. – *MB*

EMS Companies Stifled by Pandemic

TAIPEI – Foxconn founder Terry Gou said return to production at the company's factories in China has "exceeded our expectations" after the coronavirus outbreak temporarily shut down manufacturing, according to reports. But other major ODMs and EMS companies are reporting weaker near-term results.

Gou said supplies to factories in China and Vietnam have returned to normal levels. However, weak consumer demand has resulted from Covid-19, which the World Health Organization has declared a pandemic. Gou said the US market is now particularly concerning.

The Foxconn founder said he's concerned about the electronics supply chain in Japan and South Korea and cited rising prices for DRAM memory and supply issues with display panels.

"When Foxconn communicated that they would have their factories back to 100% capacity by the end of March, that was very encouraging as it relates to Q2 output," Christopher Stansbury, chief financial officer, Arrow Electronics, said on an investor call. "But for Q1, we're still monitoring it daily and it's too early to call."

In March Foxconn reported revenue would fall 15% in the first quarter. Taiwan-based competitors Compal and Wistron reported February sales were down 27 and 21%, respectively, from a year ago. The latter firms added that concerns remain over component supply and lower demand in their key consumer end-markets.

Most ODM factories in China were running at about 60% capacity as of mid March, DigiTimes reported.

Meanwhile, Sanmina does not expect to meet its second quarter fiscal 2020 financial outlook due to the impact of Covid-19, and Jabil announced its affected factories were operating at five to 10% below optimal level. Likewise, SigmaTron said its factory headcount was at 60% as of the end of February and "steadily increasing," but warned supplier decommits could swing up in the coming weeks, putting pressure on deliveries.

Not all companies were playing catchup, however. Note said its plant in Tangxia, China, which reopened Feb. 10, was running at full capacity by the end of February. *– CD + MB*

IPC Releases 5 Standards Revisions

BANNOCKBURN, IL – IPC released five revised standards covering several areas of the supply chain: IPC/WHMA-A-620D, "Requirements and Acceptance for Cable and Wire Harness Assemblies"; IPC-2223E, "Sectional Design Standard for Flexible/Rigid-Flexible Printed Boards"; IPC-2591-Version 1.1, "Connected Factory Exchange (CfX)"; IPC-1791A, "Trusted Electronic Designer, Fabricator and Assembler Requirements"; and IPC-6012E, "Qualification and Performance Specification for Rigid Printed Boards."

For printed boards, IPC-2223E will provide designers of flexible/rigid-flexible designs with updated figures, new sections and comments on microvia stacking, back-drilled holes and dual-row zero insertion force connectors.

IPC-6102E provides new acceptance criteria for back-drilled holes, discussion on reliability issues for microvia structures in Class 3 products and establishes new requirements for copper wrap plating of holes in new designs.

IPC/WHMA-A-620D provides some new acceptability criteria, figures and graphics on target conditions, solderless wrap section revisions, and a new section added on overmolding of flexible flat ribbon.

The connected factory exchange (CfX) standard provides changes made to message sections and message structure sections. Appendix A was added with a short description of all changes from V1.0, and Appendix B provides acronyms and abbreviations.

IPC-1791A provides a new Appendix D covering requirements for trust certification of non-US electronic design, fabrication and assembly organizations. Several sections have been updated as well. *– CD*

Fluidra acquired Australian EMS **Fabtronics** for AU$15 million.

Hanwha Techwin named **Torenko & Associates**, **Kurt Whitlock Associates** and **Murray Percival Co.** as its three top performing reps in the US.

Intervala signed a manufacturing agreement with **Noregon Systems**.

KIC expanded **BarTron's** sales territory to include Ohio, Kentucky and Western Pennsylvania.

Koh Young America recognized its top performing sales partners: Jim Rittman, **Aligned Solutions**; David Dogget, **FHP**; Mario Pouza, **Fuji do Brazil**; and Ray Neal, **Process Automation & Tool.**

Kurtz Ersa presented **GMG Industrial** with two Representative of the Year awards.

MacroFab purchased an **Austin American Technology** Aqua Rose PCB cleaner.

Nexvoo will outsource manufacturing to **Foxconn**.

nScrypt announced successful 3-D printing of Type IX solder and silicone adhesive dots in the 50-micron range.

Omron's foundation provided cash and robotics equipment to **California State University, Chico** (Chico State) for a new and expanded mechatronics laboratory.

Prime Technological Services has acquired **I Technical Services** for an undisclosed sum.

Productronica China and **Electronica China** have been rescheduled for July 3-5.

Quik-Pak announced a new substrate design, fabrication and assembly service.

Saki opened a plant in Yamato Koriyama City, Nara Prefecture, Japan to build electronics x-ray inspection equipment.

Smart Made Simple purchased a **CyberOptics** SQ3000 3-D AOI.

Scienscope named **Repstronics** representative in Mexico.

Yamaha Motor Europe opened a customer service and support function at its headquarters in Neuss, Germany.

South African courts have suspended the liquidation process of **Yekani Manufacturing's** R1 billion (US$66.7 million) EMS factory, according to reports.

STORING UP

Trends in the US electronics equipment market (shipments only).	% CHANGE NOV.	DEC.	JAN.	YTD%
Computers and electronics products	0.3	-0.1	0.3	0.5
Computers	1.3	0.2	3.3	-13.5
Storage devices	22.0	-17.0	10.3	49.1
Other peripheral equipment	5.6	-5.3	4.0	11.3
Nondefense communications equipment	-0.4	2.9	-0.7	5.6
Defense communications equipment	3.8	27.1	-17.5	-20.4
A/V equipment	-14.8	3.5	-8.9	-26.3
Components[1]	3.9	0.8	2.3	9.4
Nondefense search and navigation equipment	-0.3	0.3	1.0	-3.9
Defense search and navigation equipment	2.5	-2.0	-0.4	2.9
Medical, measurement and control	-2.5	-0.2	1.2	-4.2

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, Mar. 5, 2020

METALS INDEX

US MANUFACTURING INDICES

	OCT.	NOV.	DEC.	JAN.	FEB.
PMI	48.3	48.1	47.8	50.9	50.1
New orders	49.1	47.2	47.6	52.0	49.8
Production	46.2	49.1	44.8	54.3	50.3
Inventories	48.9	45.5	49.2	48.8	46.5
Customer inventories	47.8	45.0	41.1	43.8	41.8
Backlogs	44.1	43.0	43.3	45.7	50.3

Source: Institute for Supply Management, Mar. 2, 2020

KEY COMPONENTS

	SEPT.	OCT.	NOV.	DEC.	JAN.
Semiconductor equipment billings[1]	-5.7%	2.5%	9.1%	17.8%[r]	22.9%[p]
Semiconductors[2]	-14.6%	-12.7%	-10.7%	-5.4%[r]	-0.3%[p]
PCBs[3] (North America)	1.04	1.11	1.08	1.09	1.05
Computers/electronic products[4]	5.52	5.49	5.50	5.47[r]	5.43[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

Hot Takes

- **Tablet demand** in China is picking up as companies affected by the coronavirus are pushing remote work, but ODM production is impacted by shortages of raw materials and components. (DigiTimes)
- Worldwide spending on **information and communications technology** is expected to be $4.3 trillion in 2020, an increase of 3.6% over 2019. (IDC)
- **Electronics manufacturers** anticipate at least a five-week product shipment delay from suppliers due to the coronavirus epidemic. (IPC)
- The coronavirus outbreak is expected to drive **higher prices for components** throughout 2020, especially MLCC and chip resistors. (DigiTimes)
- Annual **semiconductor unit shipments** are forecast to rise 7% in 2020 and surpass one trillion units for the second time in history. (IC Insights)
- **IT spending** could grow 1% compared to the original forecast of more than 4% growth, due to coronavirus effects. (IDC)
- The global **automotive electronics market** accounted for $228 billion in 2019, and is estimated to reach $382 billion by 2026, a CAGR of 7.3%. (Grandview Research)
- The worldwide **smartphone market** is expected to decline 2.3% in 2020, with shipment volume over 1.3 billion. (IDC)
- **PC device shipments** will decline 9% in 2020, to 374 million units. Shipments are forecast to grow to 377 million in 2024, a five-year CAGR of 0.2%. (IDC)

EMS M&A Fell in 2019, Market Watcher Says

CHICAGO – M&A activity in the electronics manufacturing services sector slipped slightly in 2019, falling two to a total of 29. The market for such deals remained strong through the year, said Lincoln International, an investment bank advisory group that tracks the market.

There were 14 consolidations, four vertical/horizontal convergences, 10 private equity investments, and one "diversification" into EMS, Lincoln said. No OEM divestitures took place last year.

Stranded by Covid-19? Let's Talk

Will the latest pandemic spur mass change in communications?

GLOBAL EVENTS SOMETIMES become the catalyst for widespread change. In the world of technology, Covid-19, also known as the coronavirus, may be such an event.

Over the decades our industry has been an integral part of developing, refining and establishing many cost-effective and reliable technologies, perhaps best illustrated by improvements in communications. These improvements have not just been about broadcasting voice with higher fidelity in smaller packages, or integrating photography into word processing software, with easier user interfaces. Thanks to technology, the world of communications has been developing into much more: real-time, interactive, and transportable.

The combination of higher capacity data storage in smaller and far less expensive packages and fast and reliable wireless bandwidth, available virtually anywhere, matched with camera and microphone technology that makes the smallest device sound crystal clear and picks up the smallest sound or sight from incredibly long distances, is just part of the dramatic evolution of communications technologies.

Apps have proven equally amazing, in some ways perhaps a bigger game-changer. The ability to type a short message, add a picture and reach literally millions of "followers" has enabled real-time reporting, sharing of the most personal trivia, and widespread influence, all for virtually free. The combination of compact and high-resolution video feed via the internet and apps that take that video feed and put it on a handheld device has transformed communication. This transformation has evolved. Not long ago, we experienced either "live," a person on location or listening/viewing as an event occurs, or "recorded," when a listener hears/sees an event that has already taken place hours or days before. Today, an individual anywhere in the world can be a part of a live event via their smart device or computer, regardless of where it takes place.

And that's just what countless people now do: harness the copious communications technologies to get their message out 24/7 on everything from political musings to updates on the trip to the mall. Interestingly, business has been far slower to harness the latest communications technologies for internal purposes. Yes, they mine their customer base and lure tech-savvy folk to tell their product or service story, but for the majority of internal intra-company and customer-to-vendor or vendor-to-customer communications, the default remains tried-and-true: person-to-person via meetings, email or telephone communication.

Then a pandemic emerges and some of the tried-and-true communication methods aren't cutting it.

The coronavirus has made many rethink how best to communicate. Companies are asking employees to work from home. While this might not work in a manufacturing environment, for many other job functions and industries it does. In fact, working from home in many ways can be far more productive, eliminating distractions such as the proverbial water cooler chats or cubicle caucuses that can suck time out of a productive day.

Schools of all kinds are in position to rethink their educational processes in response to the coronavirus. Many are finding ways to teach remotely via online platforms so students can enjoy the academic curriculum and teacher-student interaction as if they were physically in the classroom. The technology is in place. Most have the hardware: a tablet, smartphone or computer.

Likewise, the medical profession is leveraging technology in ways that may have not seemed potentially mainstream just a short time back. The virtual doctor appointment, where a doctor communicates via the internet with patients, has to date primarily enabled those in remote locations to seek advice and treatment. The technology is now being harnessed so those with symptoms of coronavirus need not go out in public to be diagnosed and treated.

And finally, the road warrior – the person who feels they must see their customer in person to make the pitch and close the sale – is forced to rethink their tactics. When travel is deemed riskier, possibly a different interaction needs to be employed toward the same goal: communication when and as needed.

These situations may not have surfaced had a pandemic such as coronavirus not gripped the world. We have been slow to fully harness available technology to reduce personal risk. With fear of exposure to rampant viruses, even the most interactive activities – teaching, medicine, sales – are embracing the latest communications technologies as never before to reduce that risk.

Which brings me back to how sometimes events occur that are the catalyst for change. Forced to stop and rethink how we do something because of

continued on pg. 17

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Communications Lessons to Learn from Covid-19

Or how not to make a (potential) problem bigger than it is.

ONE OF THE challenges of writing a column a month before it gets published is material based around breaking news can become dated. As I write this (Feb. 28), the spread of Covid-19 within the US is still very limited in terms of numbers of confirmed cases. That said, it is already creating a large body of communications lessons to be learned that will remain relevant a month from now. The stock market has tanked, and people are fearful of what's next because there is a lot of speculation on worst-case scenarios. Cases are growing worldwide, and the media is uttering the words "will have an impact on the supply chain" every other sentence.

The basic problem with this or any other evolving crisis (be it pandemic, material allocation or natural disaster) is, at the beginning, it can be difficult to assess what will happen. Will this be an H1N1-type event, where business continues with heightened attention to employee health in impacted areas, or will it require the draconian quarantine measures already seen in China that created significant supply-chain disruption? The answers may be unclear for weeks. The natural impulse is to say as little as possible. The problem is when only the media is talking, people imagine worst-case scenarios. Hence the huge selloffs in the stock market.

Most electronics manufacturing services (EMS) companies have four or five primary audiences that need regular communications. In the case of publicly traded companies governed by SEC regulations related to disclosure of material events, creating a coordinated communications campaign that includes shareholders is critical, because if it becomes widely known within a company that Covid-19 issues are going to impact quarterly results significantly, these companies are required to disclose that information to shareholders. That is why companies, including Apple, Jabil and others, have issued statements. Privately held companies simply need to focus on customers, employees, prospects and their supply chains.

What does one say when there are significant unknowns? Focus messaging on what is known. Internal questions to ask in developing this messaging include:

- Are we experiencing supply-chain disruption? What steps is our company taking to address this? How is it impacting our operations?
- Are any of our facilities impacted by Covid-19 infections or travel restrictions related to those infections? What is the impact on our operations?
- Do we have a protocol in place for minimizing disease transmission among our workers? Should we tell customers and prospects what steps we are taking?
- Do our systems support work-at-home strategies? Should we discuss this with employees and provide clear guidelines?
- What workplace education needs to be done with our employees to help them better understand their responsibilities in self-quarantining and maintaining good health practices to minimize virus spread?
- What contingency plans do we have in place should a large outbreak reduce staff for an extended period?
- Are we communicating effectively with suppliers to understand real-time changes in the status of inbound shipments? Is there a way to organize that communication process to ensure all stakeholders are notified if there is significant change in any organization's situation? Do we need to push back on some material due to other shortages in any projects? Are there any border crossing or transportation bottlenecks in our area that need to be communicated to suppliers so shipments can be routed differently?
- Have we educated employees on their communications duties, so messaging to customers and suppliers is always cohesive versus changing based on who is asked?
- Do we have a media communications policy in place? This last question is very important because the media is randomly contacting members of the supply chain to get updates and will take the answer of anyone who answers the phone and has an opinion.

If your company is large enough to have a communications department, most of this is likely already done. However, if your company doesn't have a communications department or specialist, these are the key steps:

Create a committee that includes senior management, supply chain management, HR and production management. That group should discuss what is known, likely issues that will occur as the situation evolves, and what is being done to mitigate those likely risks. This team should determine what should be shared with each group of stakeholders.

Decide on messages to be communicated, messaging formats, communication channels and frequency of messaging. At the customer level, coordinating communication through program managers can be highly effective, provided the program managers have clear direction on the messages. Simi-

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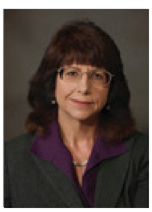

larly, employee "all-hands" meetings are an excellent way to communicate with staff, provided supervisors have been briefed and have a detailed sheet with responses to the most likely post-meeting employee questions. From a marketing standpoint, periodic email bulletin updates and social media posts work well with prospects. Providing information via your website is also an option. The supply-chain communications activities may be coordinated through buyers or commodity managers, and once again, answers to likely questions should be brainstormed in advance so those communicating have clear guidelines on what they can say.

Transparency matters. The goal shouldn't be to paint a rosier picture than the situation dictates. The goal is to fill the communications void and establish trust that your company will provide news as the situation evolves. Be careful of overstating good news and share bad news candidly.

> "Be careful of overstating good news and share bad news candidly."

Situations like Covid-19 present one of the most difficult corporate communications challenges because what is true today may not be true tomorrow. While we can't predict the outcome, lack of communication ensures stakeholders will form opinions about what is happening with your company based on what they hear from friends, other companies or the media. That may drive companies to plan stealth supply-chain moves, make employees fearful of self-reporting flu-like symptoms, or discourage prospects evaluating new suppliers from choosing your company. A comprehensive crisis communication strategy that creates unified messaging, ensures employees understand their roles and responsibilities, and keeps other stakeholders aware of your current situational assessments is the best way to build trust in a time of fear and misinformation. ❑

Ed.: Listen to Mucha's advice on crisis communications on the PCB Chat podcast (pcbchat.com).

Nepcon Japan Highlights AI, 5G, and Packaging and Assembly Trends

ADAS auto electronics require zero-defect components.

With construction of a new venue for the 2020 Olympics in Tokyo, the annual Nepcon show was split into two parts this year. There were 67,169 visitors to see more than 2,100 exhibitors. A reported 24,323 people attended the conference presentations. Exhibits included automotive and electronics. The electronics R&D and manufacturing exhibits included IC and sensor packaging, LED and laser diode technology, PCB, SMT, test and measurement, components, devices, and materials. Many highly attended conference sessions focused on 5G, AI, and automotive electronics (**FIGURE 1**).

Automotive electronics. Automotive electronics, autonomous driving and electric vehicles (EVs) were the main focuses of the presentations in Automotive World. Nissan described the evolution of advanced automotive technology and described how the need to reduce CO_2 emissions is driving the movement toward electrification. Evolving technologies such as the electric vehicle battery, including cell-energy density and volume, have improved cruising range and charging.

Urbanization and optimum mobility coupled with geriatric drivers create the need for autonomous vehicles. Speakers described breakthroughs in advanced driver assistance systems and autonomous driving (ADAS/AD), especially 360° viewing. Toyota presented its approach to autonomous driving, and Nvidia promoted its GPUs. Xilinx indicated 170 million of its devices have been shipped for automotive use. The Xilinx FPGA technology as an AI solution was presented, and challenges in object recognition were discussed. A design concept for automated parking assist using deep learning was presented. Nissan described its driver assistance technology. Volkswagen presented its adaptive Autosar. Robert Bosch talked about its safe power net solution for autonomous driving, and Continental described its views on AD. Honda and others introduced the concept of Mobility as a Service (MaaS), where connected autonomous electric cars can be shared. Technologies such as 5G and Cellular V2X were discussed by the 5G Automotive Association and Continental. Hitachi talked about design for safety with high-reliability systems. Autosar discussed the safety and security of autonomous driving, highlighting its software framework for autonomous vehicles. Infineon described trends in component packaging, including radar modules packaged in fan-out wafer-level packages and lidar systems using MEMS mirrors. Velodyne Lidar proposed standardization of range detection and targets, as well as lidar mounting and analysis methodology. After listening to many presentations, the drive for automotive electronic components with zero defects is clearer. No room for error in this application!

Advanced packaging. High-performance packaging trends, including chiplet developments, were presented by several consulting firms. Chiplet solutions from AMD, Intel and TSMC were mentioned. The high-performance packaging discussion was not limited to chiplets. Fujitsu's booth featured its server processors packaged in flip-chip ball grid array packages. Fujitsu's supercomputer application features its logic device plus Samsung's HBM, assembled on a silicon interposer using TSMC's chip-on-wafer-on-substrate (CoWoS) process.

TSMC introduced an organic RDL interposer with copper traces in low-k dielectric that permits a finer-power mesh, reducing power delivery network (PDN) impedance and noise. This will become especially important for packaging logic plus HBM3, which is expected to reach 3.2Gbs. TSMC also reported good electrical performance and reliability test results.

Embedded die presentations from TDK and Shinko Electric included applications for mobile and networking systems. SBR Technology discussed trends in application processors for smartphones, including the continuation of package-on-package (PoP) in various formats, including TSMC's InFO and future die last fan-out options. Samsung presented its panel FO technology based on the SEMCO panel FO production line purchase in 2019. Already in production for a power management IC (PMIC) plus application processor for the Galaxy smartwatch, Samsung indicated

FIGURE 1. Full house for talks at Nepcon Japan.

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the technology has also been qualified for its flagship application processor. The data presented looked promising, but no timeline for adoption was provided. Samsung is also working on an RDL technology for 2µm line and space features.

PowerTech Technology (PTI) described a variety of FO activities. While the small volume production line is used for PMICs, the new factory will focus on heterogeneous integration and developing 2µm line and space features that could be used for logic plus HBM, and the line is targeted for GPUs, CPUs and FPGAs.

Several new equipment developments were introduced on the show floor. Toray Engineering introduced a bonder for Micro LED mass transfer. Shibuya displayed its latest flip-chip bonder for optical devices. PMT Corp. displayed its "Minimal Fab" for processing WLP and FO-WLP on a small-scale wafer (**FIGURE 2**). Specialized equipment for molding from Yamada was highlighted in the process.

FIGURE 2. PMT's Minimal Fab line.

Power devices. Several companies focused on trends in power device and packaging. Rohm discussed SiC for power devices, and Japan's National Institute of Advanced Industrial Science and Technology (AIST) described the development of SiC super junction Mosfet with extremely low on-resistance. STMicroelectronics also presented power device developments. Senju Metal and Heraeus described materials targeted for power semiconductors.

AI IoT smart homes. AIoT Cloud and Daiwa Connect described how AI and IoT are increasingly combined. AIoT Cloud is a new company developing AIoT conversion of Sharp's appliances. Areas of focus include making data usable for cooking, washing clothes, air-conditioning, and air purification. Daiwa provided examples, including smart homes with special emphasis on the elderly, intelligent toilets (providing a lot of health information!), and industrial applications.

Toshiba's keynote described how big data are used to improve yield in the factory. While data collection is important, the key is using systems instead of humans for analysis and decision-making. Examples of machine learning to identify the types and causes of defects were presented. The automation of yield analysis requires input from many sensors such as flow rate, pressure, measurements. Capturing the data with machines is possible for 90% of the information needed today, but humans are still required.

Pervasive 5G theme. Many presentations discussed 5G, including use conditions that can help monetize investment in the infrastructure. Qualcomm discussed material innovations required for 5G packages. The discussion focused on the need for low Dk/Df substrate dielectrics, low Dk/D mold compounds, and the need for conformal shielding overmold and substrate sidewalls, as well as the use of electrically conductive paste. Qualcomm highlighted its AiP module, digital module for the application processor and modem, and its radio frequency (RF) front-end (FE) module.

One session discussed the requirements for substrate materials as the industry moves to 6G, with presentations from AGC and Oki. Semi Consult discussed flex circuits for 5G mobile phones, highlighting Apple's iPhone.

PCB materials. Hitachi Chemical and Zhen Ding Technology (ZDT) discussed new materials and processes for PCBs. A presentation from Robert Bosch described the impact of autonomous driving and electrification on the PCB and its reliability requirements. Challenges of miniaturization, higher frequencies, and new high-speed materials with high temperatures are creating manufacturing, reliability, and testing challenges. Meiko Electronics described 5G material trends and challenges, such as transmission loss by the PCB material and copper foil surface, and RF material.

Next year's conference will take place from Jan. 20-21 at Tokyo Big Sight. The conference will be combined again with Robotics, Wearables, and SmartFactory. □

ROI, continued from pg. 13

an unforeseeable event can make us realize a more efficient, better option is available. For businesses and institutions that may have avoided investment in the technology, the alternative may suddenly seem far costlier. For those reluctant to break from their comfort zone and try something new, the challenge of doing so becomes far less risky than continuing along the same path. The urgency is there to embrace and try the new.

These virtual communications options may not permanently replace all conventional methods, but their adoption will most certainly accelerate. Time will reveal whether changes in how we communicate are a temporary reaction to an immediate pressing need, or if the technology proves an opportunity for all. □

Common Design for Assembly 'Gotchas'

DfM means design for money. If it can't be built, that's a waste.

GREAT IDEAS COME together with great timing; what's left is great execution. Flipping the switch that sets the factory in motion causes a few pain points. These "opportunities for improvement" will dictate your agenda down to the minute with all the little things that go wrong. Let's say there is a factory downstairs from you. Further, the factory is doing slow and laborious rework on old printed circuit boards, aka PCBs. There is a solution! New PCBs. We're going from P0 (zero) to P1 (one). That's where we, the designers, come in.

At new PCB time, the first order of business is improving the electronics in some way. The fix could be better performance, lower cost, higher reliability and, in some cases, all the above. Venturing into wireless technology and gaining FCC approval to play in its allocated spectrum is no slam dunk. Beefing up the power grid is a typical step. A good power distribution network has been known to cover for otherwise iffy routing. Every engineer will have some considerations carried forward.

Remember those last-minute patches to fool the design rule check (DRC) into giving a pass to the intentional short from one ground domain to another? No? Now would be an appropriate time to address that. Test access, anyone? More hooks to keep tabs on current density are always a welcome addition.

The second order of business is getting the fab shop to build to the print. The P1 version is when the final form factor is in play. That only matters to the extent that it sets the size limit. For your information, the limit shrinks constantly. Having collected data from the P0 build, there is some confidence in the all-important stack-up data, along with impedance calculations. Capturing all that for posterity is a big deal.

A perspective I like is to think of DfM as design for money. Manufacturing is where money changes hands. Product goes in one direction, and money flows back toward the source of goods. If you're any kind of capitalist, keep that machine running. Do not turn it off or even slow it down.

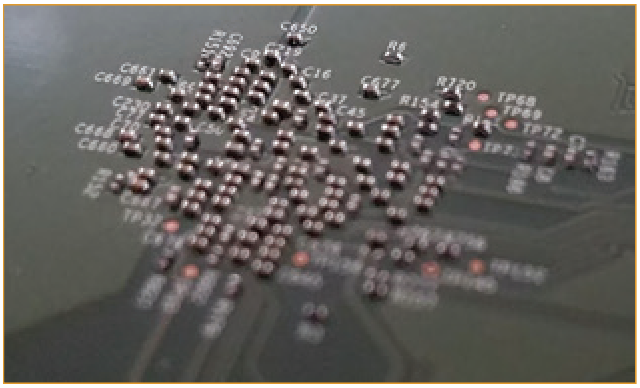

FIGURE 1. A cap-hungry MCU lives on the other side.

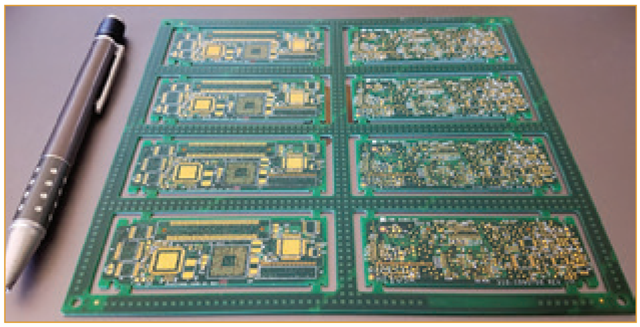

FIGURE 2. How many tooling holes do you prefer?

Some assembly required. Finally, handing a set of clear plans to the assembler is way more important than building a flatpack shelving unit. Numbers of holes on the drill chart need updating. X-y machine data. Critical dimensions and other mechanical relationships are added for clarity. Anything that bubbles up out of the original design gets squared up on the second revision. In some cases, retrofitting new data can take more effort than the original creation.

FIGURE 3. Semiautomated assembly.

The simple things. Some smart aleck said a

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man with two watches never knows what time it is. Producing data in two popular formats is tantamount to giving your vendor an extra watch. Once and only once. That is to say, all data must be congruent in terms of part numbers and revisions and properly put to bed. One complete set of information without overlap/repetition of the data.

An assembly drawing is just that. The soldering profile, stencil thickness, paste composition and so on are relevant, but they ought to belong to a process document. This advice is more about passing ISO audits than helping the assembly line worker do their job with a one-pager on a particular PCB assembly. Separate “what is” from “how to.”

If you choose the other path, circle back to your assembly line to see if any alterations were made to the stencil artwork. Any number of global micro-edits are at their disposal when it comes to dialing in a stencil. I try to avoid getting the assembly drawing involved with the churn of process methodology on the assembly floor.

If there’s a conflict between the information on the PCB silkscreen marking and the information on the assembly drawing, it can disturb the people involved with making those products. Your only defense against this type of transgression is to pour over the details of file names to make sure nothing is ambiguous.

I don’t know who said it, but a little gem someone gave me is this: “If something can be misunderstood, then it already has been.” The automotive industry borrows a word from the Japanese: *poka-yoke* (ポカヨケ). The essence of this concept is something will fit together if and only if it is being assembled correctly. It could be the reason three tooling holes are preferred to four on the assembly subpanel. In English slang, “idiot proofing” works as a harsh translation.

So, first electrical debug, then mechanical fit, and finally placement, as it relates to assembly concerns, are solved. The reason for this hierarchy, I think, is the immediacy of the team members. Inevitably, PCB designers are first linked to electrical engineers, even (or especially!) when their background is mechanical engineering. Our world is a blend of three things that are occasionally (read: always) at odds with one another.

Because assembly takes place at some distance in both space and time, it is easier for that facet to fall off the radar. The board designer is their champion, from the smallest component placement decision up to the final design review. We’re at our best when we can integrate all these, so the line keeps moving. ❑

The Foundation of the PCEA is Laid

The Orange County chapter joins up, and a new PCEA chairman is named.

IN THIS MONTH'S column, I highlight the Orange County Chapter's recent meeting and its transition from IPC to Printed Circuit Engineers Association affiliation, recent PCEA activities, and the evolution of this column, including introducing Kelly Dack, CID+, PCEA's new communications officer.

Orange County Chapter

Scott McCurdy, president

The Orange County Chapter is doing very well in Southern California and has been active for 18-plus years. We are proudly the largest active chapter in existence, based on attendance at our quarterly meetings. We average 50 to 65 attendees at our meetings, and occasionally have 80 or more in attendance. In our most recent meeting, held Jan. 21 at the Harvard Athletic Park multipurpose room, we had an outstanding crowd of 80 people in attendance to hear the educational presentation by Gerry Partida, a senior field application engineer for Summit Interconnect.

The main topic for this meeting was Microvias: Have You Designed for Reliability? How to Detect Weak Microvias and Avoid Costly Assembly Defects and Customer Field Failures. As component pin densities get tighter with each passing year, designers have been pushed to use HDI with more microvias and blind/buried via structures. As a result, tighter via densities and signal integrity requirements in printed boards have revealed reliability concerns with microvia structures in high-performance products. Avoiding post-fabrication microvia failures is critical to the success of your products, and there are details designers need to know.

Gerry's presentation reviewed concerns and reliability testing relating to microvias. He provided an overview of the HDI processes and presented the use of current test methods and the superiority of testing with the IPC-D-coupon and IPC-TM-650 test methods 2.6.7.2 and 2.6.27. Gerry also discussed the warning statement in the forthcoming IPC-6012E": "Qualification and Performance Specification for Rigid Printed Boards."

If you're interested in learning from an industry subject-matter expert like Gerry Partida, attend and become a member of a local PCEA chapter in your area.

Also, Mike Creeden, Insulectro's technical director of design education, provided an overview of the new PCEA that included its inception details, the PCEA purpose/mission, and the advantages of membership. Mike's presentation was received extremely well with much interest and engagement by all in attendance.

At the end of the meeting, we opened the floor for discussion, as we always do. The main discussion this time was on the PCEA topic and the Orange County Chapter's future. Leading up to the chapter meeting, our chapter officers unanimously voted to become a PCEA chapter. In the chapter meeting, chapter leadership (and Mike Creeden) let members know our new direction going forward and the decision to leave the umbrella of IPC. The chapter's leadership decision and the new direction for the chapter were widely accepted with great enthusiasm and eagerness to move forward as part of the collective of PCEA.

I hope to see you at our next lunch 'n learn event under our new chapter name: Printed Circuit Engineering Association – Orange County Chapter (PCEA-OCC).

PCEA Activities

Much activity continues as PCEA's foundation is laid. Several legacy IPC chapters have made the decision to affiliate with PCEA, like the Orange County Chapter did. In early February, we held an executive board meeting. The overall structure of PCEA is forming nicely, with executive board member elections wrapping up. The newly elected executive board members will be introduced next month.

Also, PCEA's website (pce-a.org) is up and running, but is still in its infancy. It is our hope to have our official website released later in March. I encourage everyone to check out the website and sign up to receive more details of PCEA as we unfold in the industry.

In the coming months, we will expand the number of chapters, while realizing a steady growth of our membership. If you're interested in joining or starting a chapter in your area, feel free to participate and join the many professionals who are the backbone of our industry. Again, visit our website and contact us for more information.

The Evolution of 'The Digital Route'

I have been writing this column for over a year now. It has been a huge success so far, because it has been a team effort putting it together from month to month. My main objective for this column remains to promote continued globalization of knowledge sharing and education for any and all involved in the design, fabrication, assembly, and test of printed circuit boards. Getting people to communicate more often

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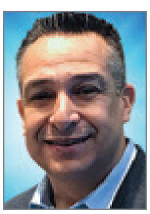

and outside of their box is important. That is why I decided to be a contributor: for the betterment of our industry.

I will be taking on a leadership role within PCEA as chairman. In doing so, I will pass oversight of this column to a renowned colleague and dear friend of mine, Kelly Dack, CID+. I will still share my thoughts through a "message from the chairman" section within the column, but Kelly will serve as the PCEA's communications officer and assume oversight of this column. I wish Kelly well and encourage everyone to contribute to the ongoing success of this column. We very much appreciate your readership.

Professional Development and Events

Here are some upcoming industry events to look out for in 2020. I hope you have the opportunity to attend one or more.

- April 27-30: Zuken Innovation World Americas 2020 (Coronado, California)
- **Jun. 9-10: PCB2Day – SMT Assembly Boot Camp (Austin, Texas)**
- **Jun. 11-12: PCB2Day – Design Essentials for PCB Engineers (Austin, Texas)**
- Jun. 14-20: IPC SummerCom 2020 (Raleigh, North Carolina)
- Jun. 22-25: Realize LIVE 2020 (Las Vegas, Nevada)
- July 7-8: Cadence Live 2020 (Silicon Valley, California)
- **Sept. 8-11: PCB West (Santa Clara, California)**
- Oct. 7-9: AltiumLive 2020 (San Diego, California)
- Nov. 11: PCB Carolina (Raleigh, North Carolina)

As always, if you have a local or regional industry event in your area and would like to announce it, please feel free to submit the details to be listed in an upcoming column. For 2020 CID and CID+ certification schedules and locations, contact EPTAC to check current dates and availability. (Dates and locations are subject to change.) □

New IPC Standards Emphasize Performance over Composition

Changes in standards and supply chain are making high-performance materials more accessible.

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5G IS EXPECTED to revolutionize many aspects of work and life, as a critical enabler for connected cars and self-driving vehicles, autonomous factories, remote medical surgery and the diffusion of smart "things" throughout cities, infrastructures and our homes.

Within the automotive sector alone, its influence will be huge thanks to attributes like ultra-low latency that will enable time-critical use cases such as V2X. The 5G Automotive Association (5GAA) is excited about the prospects for cellular V2X (C-V2X) to consolidate vehicle-to-vehicle, vehicle-to-infrastructure, vehicle-to-pedestrian, and vehicle-to-network modes, combining direct communication, communication with cell towers, and links to cloud services.

For a country to delay 5G rollout risks compromising standards of living and economic competitiveness. On the other hand, US concerns about foreign involvement in such a pervasive infrastructure are widely reported. While the UK has decided to grant Huawei access to noncritical parts of the network – against the counsel of the Trump administration – it has been proposed the US consider the outright purchase of equipment companies such as Nokia as a way of keeping pace while also staying in control.

We all understand what's at stake. The fear of falling behind is driving the search for solutions. Moreover, in the race to unleash the benefits of 5G for life, work and everything else, we can expect increasing pressure on the pace of intellectual-property development, as well as demand for the high-performance components and materials needed to make it real.

The PCB substrate materials capable of satisfying 5G technical specifications are esoteric, high-performance formulations characterized by very low losses. Tightly controlled dielectric constant (Dk) and low dissipation factor (Df) are needed to ensure signal integrity and minimize power demand and heat dissipation. Low passive intermodulation and good thermal stability are also required. The materials are technically specialized; few companies can produce them, and supply can be limited. 5G infrastructure rollouts have barely hit their stride and already there is talk of shortages that could delay and disrupt projects ongoing around the world. Applications like 77GHz automotive radar are also set for explosive growth and will compete for a share of the supply.

Part of the problem is manufacturers of substrate materials are managing complex, globalized supply chains that are difficult to control. There are many variables, and some companies in these chains may have conflicting business interests. I have explained before how a wholly owned supply chain provides protection against some of these hazards. Such arrangements can keep lines of communication short and untethered to supply-chain management skills of third-party companies.

No company has unlimited resources or flexibility to ignore the effects of global supply shortages that coincide with surging customer demand. However, complete control over the means of production and distribution makes it easier to make relatively small but influential adjustments to handle the situation. Production capability and capacity can be raised in targeted locations, increasing inventories of the most affected products, which in turn can be distributed in strategic locations globally. On the other hand, the understanding and cooperation of customers is vital to be completely confident of delivering the required products to the right place, at the time they are needed. Ideally, this should extend to automated electronic cooperation between the supplier's and customer's enterprise resource-planning software tools. Letting the machines share the information they need automatically is the most effective and efficient way to ensure customers' needs are communicated properly to be fulfilled at the right time.

On the other hand, human interaction is very much needed at the cutting edge of product development. The technical demands in cellular infrastructure are always ahead of the standards-making processes, so equipment designers need to work extremely closely with their material suppliers to leverage the newest and best materials and make their products as good as they can be.

An important change in the standards landscape, however, concerns the latest IPC-4103 specification covering low-loss materials for use in printed circuits for microstrip, stripline, and high-speed digital circuits. Unlike IPC-4101 and IPC-4921, which were derived from NEMA specifications first published in the 1960s, IPC-4103 characterizes materials based on their Dk and Df at different frequencies, without concern for chemical composition. Materials covered by this specification typically have Df less than 0.005 and include state-of-the-art styles as low as 0.002.

As the performance of modern PCBs has advanced significantly since the 1960s, it makes sense to bypass the constraints of 1960s' thinking when it comes to material grades. Emphasizing performance over composition enables a pragmatic approach to material selection that should make all our lives easier. □

An Ode to Pi

Understanding key differences between time and frequency domains.

AS MARCH APPROACHES each year, I can count on the bullfrogs around our neighbor's pond to be out in force, memories of days coaching baseball and softball, my wife's birthday, and on March 14, "Pi Day," which has been celebrated by geeks around the globe since 1988. I take the day seriously due to pi's prevalence in almost every field of science, ranging from astronomy, electromagnetics, physics, to probably several other fields I'm not even thinking about. How did pi find its way into so much science, and what are the implications for electromagnetics?

Before we go into details regarding the time and frequency domains, it's beneficial to discuss the "unit circle" and radians. A unit circle is simply a circle with a radius of 1 (regardless of units). The circumference of a unit circle is 2π, meaning that one cycle would be 2π, and there would be 2 x 3.14 radians required to complete the circle. This is illustrated in FIGURE 1.

2π is the period or circumference of the unit circle. Without the mathematical relationships tied to the circle and pi, it would be very difficult for signal-integrity simulation software to model the behavior of signals without building circuit boards and making physical measurements. In other words, we'd only know what was going to happen after it already happened.

Angular frequency's connection to electromagnetics is discussed below. For now, just realize the number of times we sweep through the period per unit time is the angular frequency, typically represented in radians per second.

The time domain. We're naturally more familiar with the time domain, which we deal with in everyday life, but the frequency domain can provide valuable insight into signal-integrity effects, impedance and loss. To understand this connection, we need to discuss both the time and frequency domains. Dr. Eric Bogatin[1] does an excellent job of describing the differences and distinctions, so I'll leverage that information with his permission.

Using relationships well-known in the time domain, the clock frequency shown in FIGURE 2, F_{clock}, represents the number of cycles per second the clock goes through, which is the inverse of the clock period, T_{clock}.

$$F_{clock}\,(\text{GHz}) = \frac{1}{T_{clock}\,(\text{ns})}$$

The math is easy if we represent frequency in gigahertz and the clock period in nanoseconds. The signal in Figure 2 has a frequency of 1GHz. Similarly, a 10GHz signal has a period of 0.1ns.

It's important to note the time domain is the *only* domain that's *real*. What we describe as the "frequency domain" below connects the time domain to the title of this article.

The frequency domain. As mentioned, the frequency domain provides valuable insight into signal-integrity effects, impedance and loss. If you've been around hardware design for long, you've no doubt heard about the "frequency domain," which is where pi really starts to appear. Bogatin[1] points out, "The most important quality of the frequency domain is that *it is not real*. It is a mathematical construct. The only reality is the time domain. The frequency domain is a mathematical world where very specific rules are followed." (Emphasis mine.) This is the part of the world where you can use "imaginary numbers" and people won't think you're crazy.

In the frequency domain, everything's a sine wave, and sine waves are everything. Any waveform in the time domain can be completely characterized by a combination of sine waves. And mathematically, we know all about sine waves.

Sine waves typically provide a straighter path to an answer because of the types of electrical problems we often encounter in signal integrity. Transmission lines, in a simplified sense, can be represented as networks of resistors (R), inductors (L), and capacitors (C). As Bogatin[1] notes, if we "send any arbitrary waveform in, more often than not, we get waveforms out that look like sine waves and can more simply be described by a combination of a few sine waves."

No new information is added when switching from the time domain to the frequency domain, but

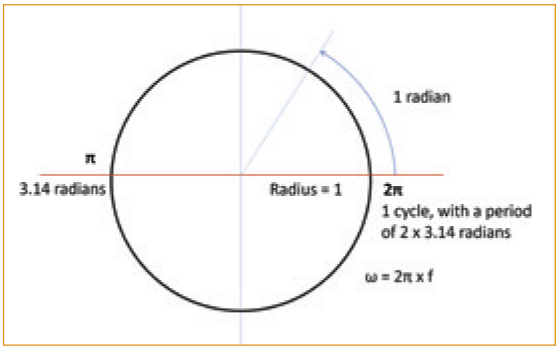

FIGURE 1. The unit circle has a radius of 1 and a circumference or period of 2ω.

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AUSTIN, TX
June 9-10, 2020

SMT Assembly Boot Camp, PHIL ZARROW

This SMT electronics assembly class is a practical overview of the many different processes and materials used in through-hole and surface mount technologies (SMT). It is a focused, two-day long class, which provides students with the opportunity to learn and understand the processes, tools, and materials used in today's manufacture of electronic assemblies.

The course combines lecture, videos and discussion and is intended for those that are new to electronics assembly and want to come up to speed on the processes, materials, equipment and procedures.

AUSTIN, TX
June 11-12, 2020

Design Essentials for PCB Engineers, SUSY WEBB

Engineers designing their own boards will need to understand and use the same science that seasoned PCB designers have built up over many years. For example, the way parts are built, or a board is designed can make a huge impact on the ease of fabrication and assembly, just by the practices put into place while working. Those practices can increase yields and lower the cost for all, and this two-day workshop starts with thoughts about that. There are many ways to place parts on a board, but some work much better than others for the physics, electrical and mechanical purposes. We will discuss the order of placing parts, setting up routing, and placement ideas that will lead to better flow.

On Day 2, fine-pitch BGAs will be examined. Their size and pitch make them increasingly challenging to work with, as do the signal integrity and EMI issues that come along with them. We will look at through-hole and HDI examples for fanout, grid and routing information, and their specific manufacturing needs. In the last section we will delve more into the science of how everything works together by discussing the electronics and physics, controlling impedance and high-frequency energy, and stack-up and power issues. There will be examples of how a signal's field energy actually flows through layers of the board, and steps to take when routing signals through the board. The workshop will conclude with a brief discussion of autorouting vs. hand routing.

certain things, including but not limited to scattering parameters (S-parameters, a topic for a future column) live quite happily in the frequency domain. Results from an SI simulator can be viewed in either the frequency or time domain. To illustrate the simplicity of the frequency domain, compare the plots in **FIGURE 3**.

The figure is an excellent illustration of how much easier it is to describe things in the frequency domain. If the time-domain plot represents hundreds or thousands of data points, the same sine wave in the frequency domain can simply be described with a frequency (f) and amplitude (A).

"But what about pi?" you might ask. Well, sine waves have amplitudes, frequency (and periods), as well as phase. The frequency (f, measured in hertz) is the number of complete cycles per second made by the sine wave. Angular frequency is measured in radians per second. As shown in Figure 1, radians describe fractions of a cycle. Figure 1 shows there are $2 \times \pi$ radians in one complete cycle. As a physicist-friend recently said, "We humans can devise other angular systems to our taste, like say 360°, because, hey, the number divides really well; but they are arbitrary. When we finally meet up with the guys from Zeta Reticuli, they are unlikely to have 360° circles, but they will agree that a circle or cycle is 2π." That's because the ratio between the circumference of a circle to its radius will be the same in Euclidean spaces.

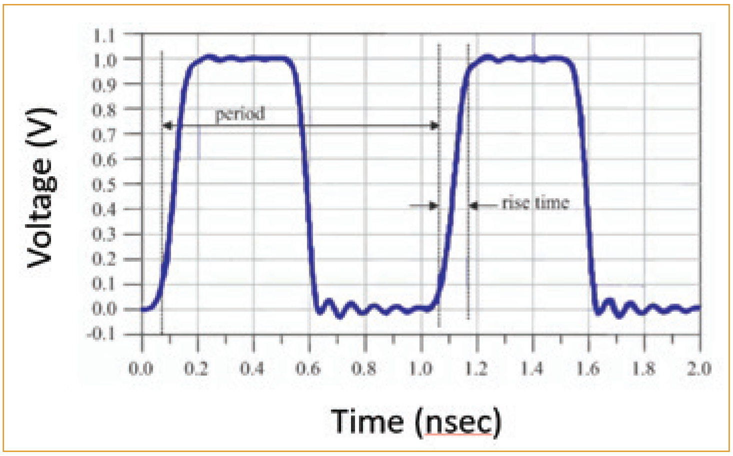

FIGURE 2. A clock signal, shown in the time domain, with a period of 1.0ns (Bogatin[1]).

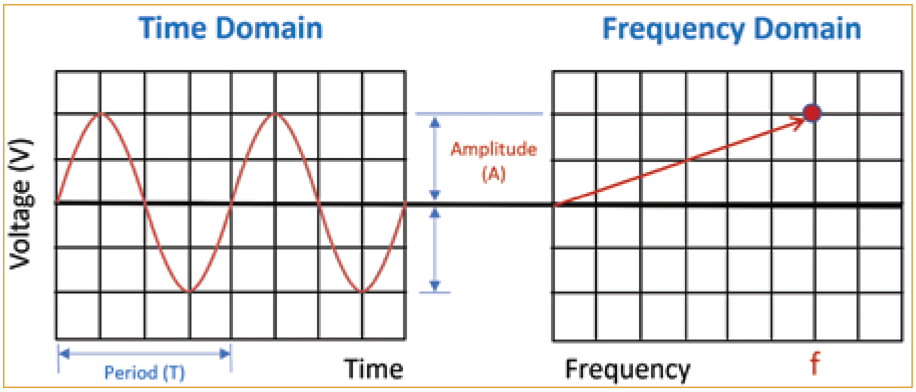

FIGURE 3. A sine wave, shown in the time domain, with hundreds of data points in the time domain, contrasted to representing the same sine wave in the frequency domain with just one data point, described as frequency (f) and amplitude (A) (adapted from Bogatin[1]).

The Greek letter omega ω is typically used to refer to the angular frequency, measured in radians per second. The sine-wave frequency and the angular frequency are related by $\omega = 2\pi \times f$ where ω is the angular frequency in radians/second, and f is the sine-wave frequency in Hz. Once we've transformed the frequency into radians/second, the mathematical relationships of complex systems become much easier, as we will discuss further below. But rather than blowing past the relationship between angular frequency and your time-domain frequency, make sure you understand and memorize the relationship between angular frequency and time-domain frequency above, as ω is extremely prevalent in the frequency domain.

Impedance and reactance. As mentioned, transmission lines can be represented by a network of parasitic resistance (R), conductance (G), inductance (L), and capacitance (C). Each of these *impedes* current flow. We characterize these factors that impede current flow as follows:

- Resistance (R) is the impedance to current flow, represented by an ideal resistor, in ohms. Resistance has no relationship to frequency.
- Reactance (designated by X), also represented in ohms, is the impedance to current flow from an ideal inductor (L) or capacitor (C). Reactance depends on signal frequency, as noted in the relationships below.
- Impedance (designated by Z) is represented by the combination of resistance and reactance, making it a function of frequency through the reactance elements.

The impedance relationship is $Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$ where G is conductance, and R and G represent the "real" part of impedance, while jωL and jωC represent the "imaginary" part of impedance – inductive and capacitive reactance in the frequency domain. Without going deep into what's called "imaginary math," the value of j is the square root of (-1). Obviously, the square root of (-1) doesn't exist, hence the term "imaginary."

Jenny, I've got your number. I memorize pi as either 22/7 (simple enough) or 3.14159-ee-ine, rhyming with the Tommy

Tutone song, "867-5309/Jenny." If you don't know the tune, I recommend getting out more and Googling it. It's a cool song!

We could go much further here to discuss conductor loss and dielectric loss in the frequency domain as well. Again, angular frequency, pi, and imaginary arithmetic are involved. I'm running long here, so I'll save that discussion for another day, and will simply close by wishing everyone a happy Pi Day! ▫

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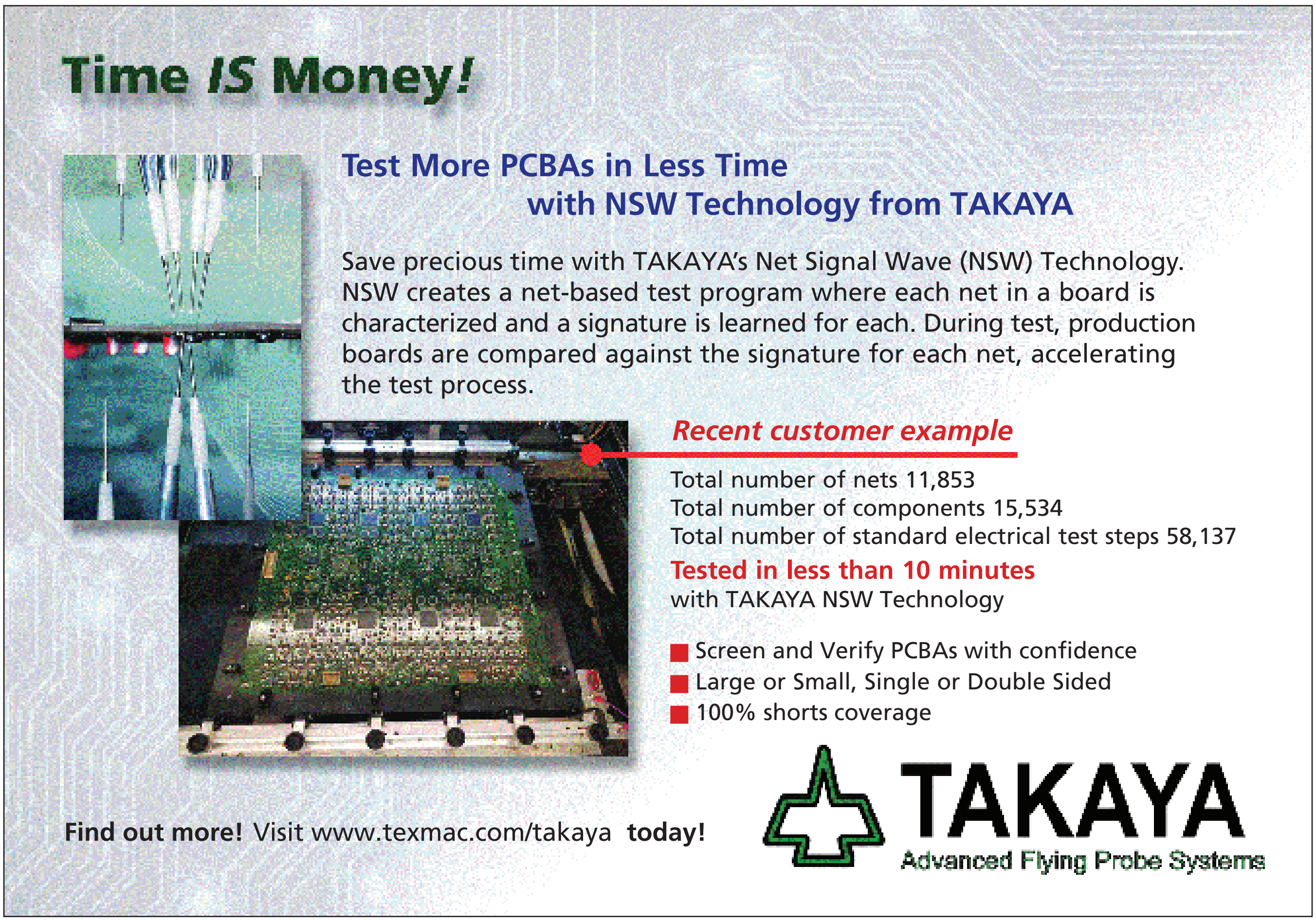

I Need a Stiffer Flex Circuit. What Do I Do?

Material choices are often based on the planned assembly.

MANY DIFFERENT MATERIALS are used to rigidize flexible circuits. Likewise, the reasons for stiffening an area on a flex board are many. The "best" stiffener material is tied to exactly why you are stiffening your flex circuit.

Rigidized SMT or through-hole component areas. Providing a rigid, stable surface for mounting components is probably the most common reason for stiffening an area on a flexible circuit. If components are mounted on a flex, which is then bent in that area, there is a very good chance the solder joints or solder pads will be damaged. The industry standard is to rigidize any area on a flex that has soldered components. If components are all SMT, install the stiffener on the side opposite the components. If through-hole components or connectors are used, mount the stiffener on the same side as the components. If components are on both sides, rigid-flex construction is probably needed, but that is a topic for a future column. By far the most common (and least expensive) stiffener material is epoxy-glass laminate (FR-4). This inexpensive sheet material comes in a range of thicknesses and is machined to size and shape by the flex circuit manufacturer. The machined stiffeners are then applied with either a pressure-sensitive or thermosetting adhesive (see below). Another material for stiffening a component area is 0.003" to 0.005" polyimide film. This material is common and cost-effective, since these stiffeners can often be added in panel form. This option is typically specified when overall thickness is a concern. The material is a bit more expensive than FR-4 but offers significant time savings during stiffener mounting. This material will not provide the same level of stiffness as a thicker FR-4 stiffener, so operators must exercise care in handing and forming during installation.

ZIF (zero-insertion force) connector applications. ZIF connectors are an easy, reliable and inexpensive termination option. But these connectors have very specific thickness requirements for the flex to ensure it will seat securely in the connector. The typical thickness requirement for the insertion zone of the flex is ~0.011" to 0.013". Since most single- and double-sided flex circuits fall short of the ZIF thickness requirements (especially since the top cover is removed over the fingers), a stiffener is added to increase the thickness of the area inserted into the ZIF connector. ZIF stiffeners are usually less than 0.005" in thickness, so polyimide is the preferred material choice for these applications. Virtually all thickness options of polyimide film are supplied to the fabricator with pre-clad thermosetting adhesive, making it the typical bonding adhesive choice.

Heat sink stiffeners. It is more and more common to see high-power LEDs mounted on flex. Due to the heat generated by the LEDs during operation, it is sometimes necessary to provide a heat sink stiffener. Aluminum is the most common heat sink material due to its low thermal resistance and relatively low cost. Aluminum stiffeners are typically punched out of sheets, then bonded with either pressure-sensitive or thermosetting adhesive. Stainless steel is occasionally used as a heat sink material but is typically more expensive than aluminum.

Mechanical rigidity of specific non-component area. Mechanical stiffeners are often necessary for a variety of reasons, including:

- To provide abrasion protection.
- To force a natural bend into a specific area.
- To add mounting holes that can accept screws or other hardware.

The material type used for these applications is

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FIGURE 1. Aluminum stiffeners can be a great way to both stiffen the flex and dissipate heat from LEDs.

driven by which of the aforementioned items is desired. Usually FR-4 is the first choice to evaluate due to its low cost and ease of installation. It can be machined to virtually any size and shape, and can also be drilled and tapped to accept hardware such as screws, small bolts, and press-fit hardware. Polyimide stiffeners are widely used for abrasion protection, and to force a bend into a specific area. Its thinness makes polyimide film typically a poor choice to use in conjunction with screws and other metallic mounting hardware.

While stiffeners could technically be bonded with virtually any type of adhesive, only three are used regularly: thermosetting epoxy film, thermosetting acrylic film, and pressure-sensitive adhesive. Thermosetting epoxy and acrylic are virtually identical in most respects regarding processing and finished properties. Both types require high-pressure and high-temperature lamination for adhesion and curing. This results in a superior bond between the flex and any mechanical stiffener added, but is also more expensive due to the added lamination step. Pressure-sensitive adhesive (PSA), as the name implies, only requires some pressure between the flex and stiffener in order to bond. A *lot* of PSA options are available; it is imperative to choose one that will bond well to both the flex and stiffener material. Most PSAs are applied by hand and require only finger pressure to create an acceptable bond. A very quick low-temp "kiss" press operation can reduce some of the bubbles and provide increased bond strength.

This brings up another important point. Per IPC-6013, stiffeners are for mechanical support only, and void-free lamination is *not* required. Bubbles and small voids are almost always evident with PSA-bonded stiffeners, and bubbles are also common to a lesser degree with thermoset adhesive bonded stiffeners. ▫

FIGURE 2. FR-4 (left) and polyimide (right) make up the lion's share of stiffener used today.

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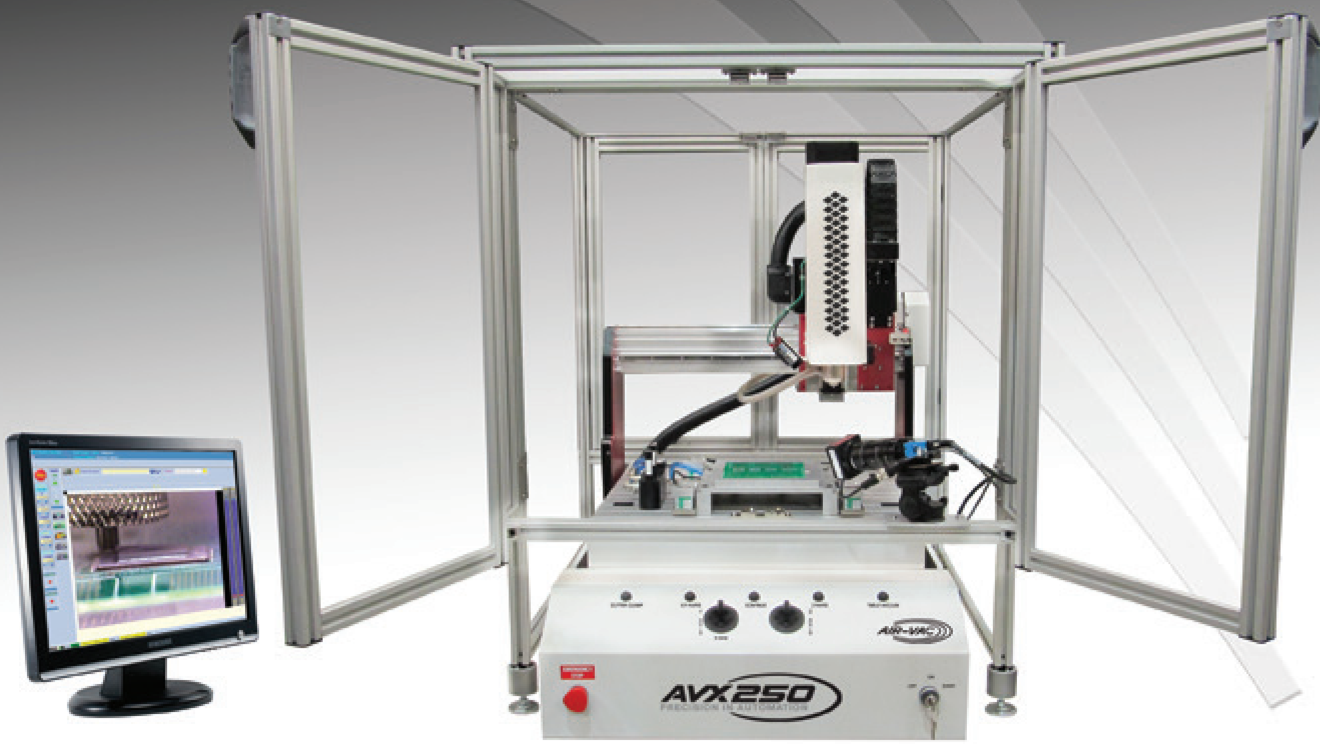

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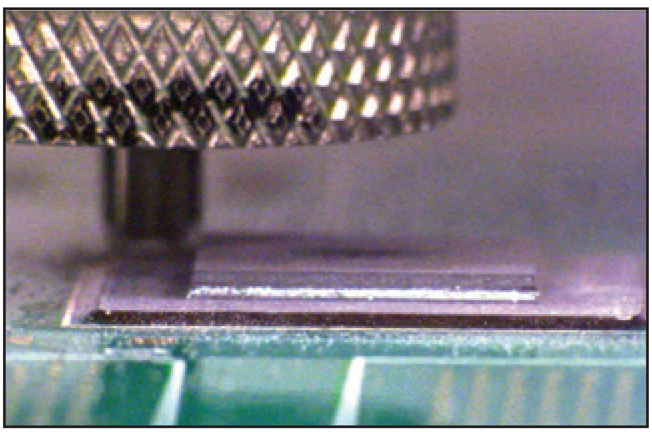

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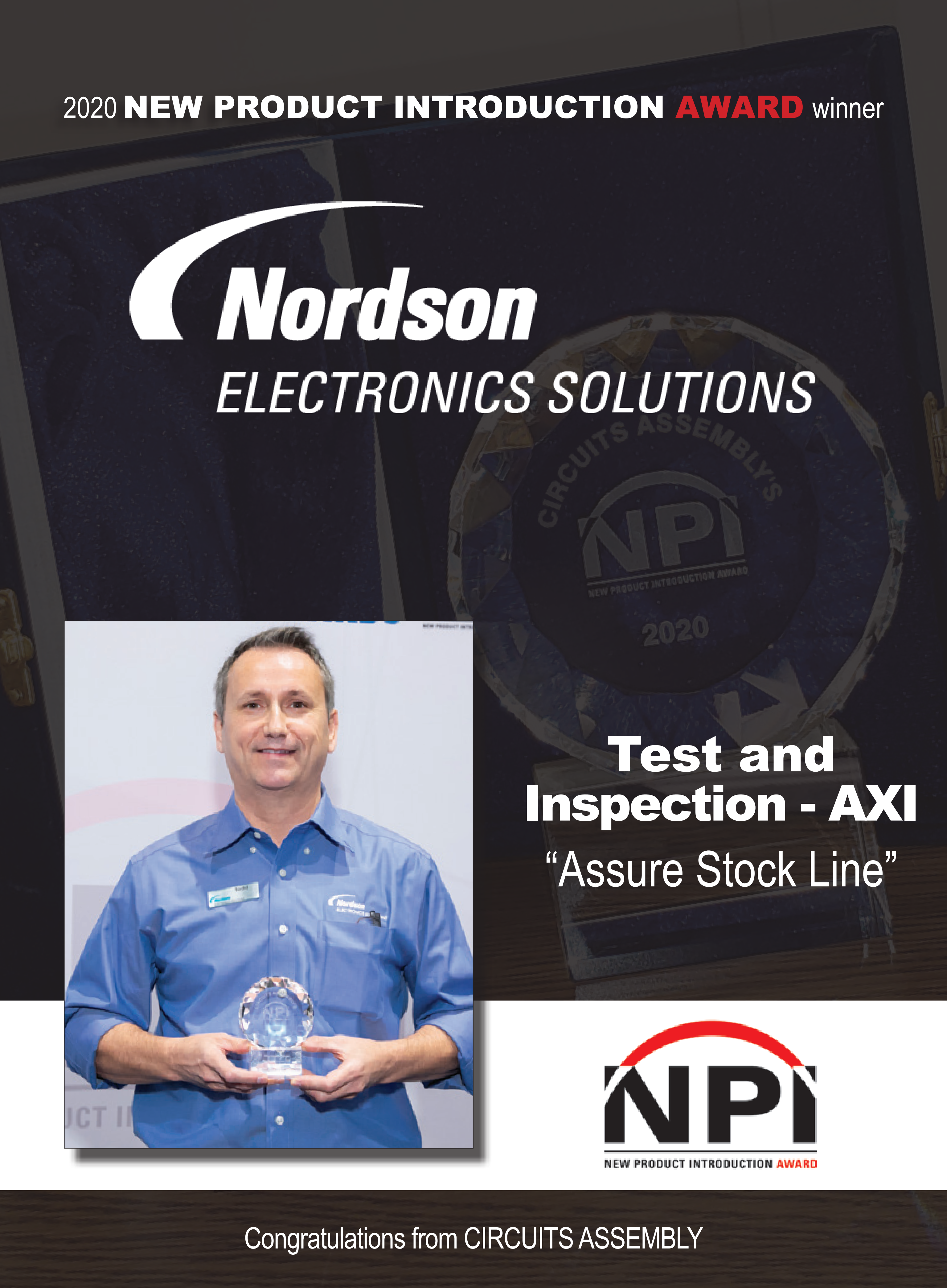

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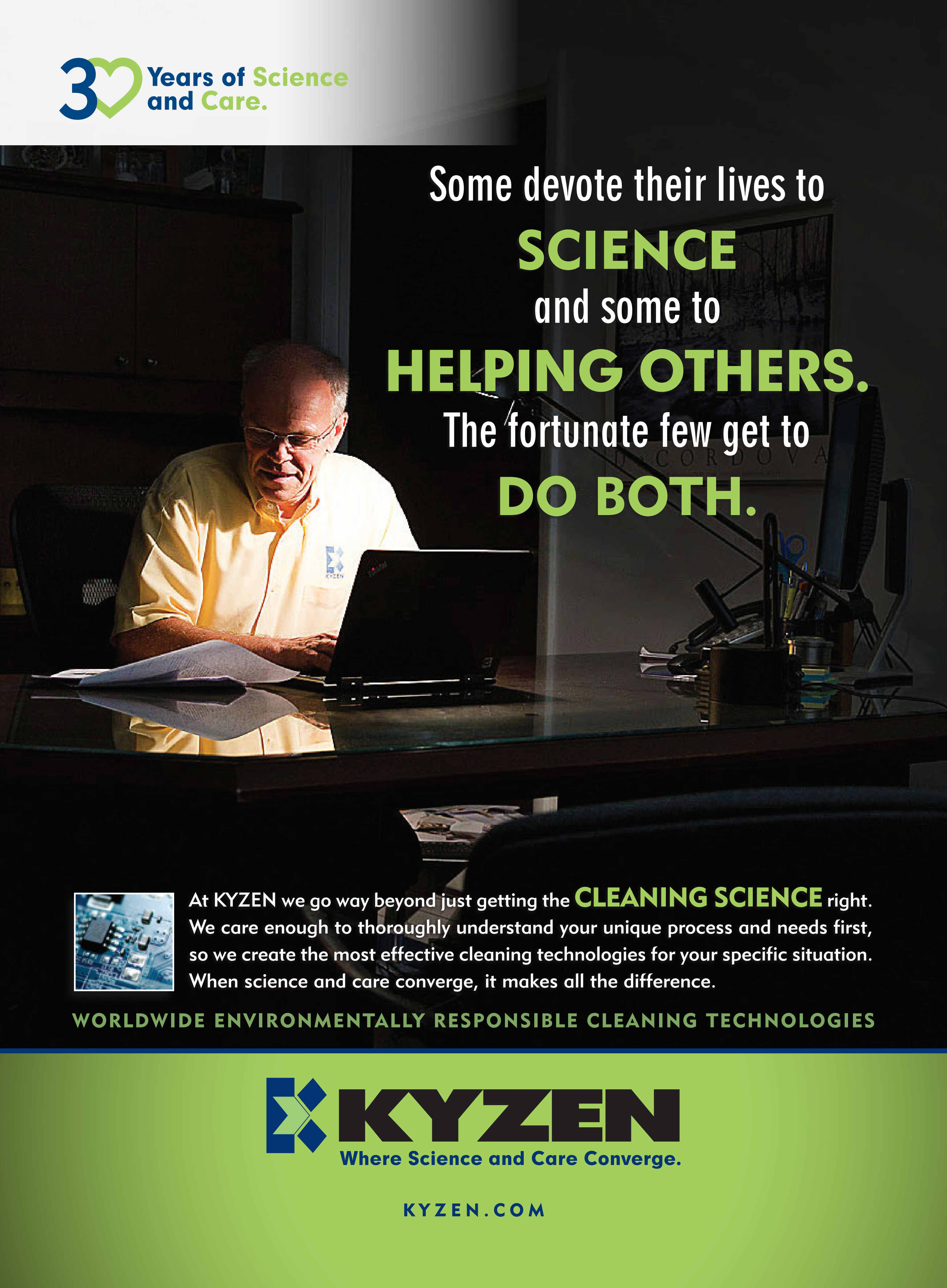
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BGA PITCH Impacts on Bare Board Fabrication

A look at how array technology influences processes from board routing to drill to test. **by TODD MACFADDEN**

"Miniaturization has made it possible for electronics to penetrate society more widely and deeply than ever before."[1] That sentence is as relevant today as when it was written in 1984. It embodies the core tenets of Moore's law, and the associated manufacturing technologies that have enabled performance improvements in electronics at a predictable cadence for 55 years: 1) decreasing feature sizes, 2) increasing functionality, 3) decreasing cost. One of the most important innovations to accommodate increasing densification of chip technology has been the ball grid array, introduced in the early 1990s, which permits high pin counts per area relative to peripheral lead and no-lead packages such as QFNs and DFNs. The evolution of array packaging has moved from BGA to chip-scale package, to wafer-level CSP to flip-chips, defined by a steady march toward smaller balls and finer-pitch arrays (**FIGURE 1**).

Array pitch has profound implications for the printed circuit board industry, which must continually develop newer methods to route dense, high-I/O packages with increasingly finer pitch. In fact, it is arguable that the pitch of array packages has been *the* most important driver of most PCB technology developments, and will continue for the foreseeable future. As BGA pitch* continues to shrink to accommodate chip density, the number of PCB suppliers with the capability to fabricate PCBs to support these finer pitches decreases (**FIGURE 2**).

This article highlights some of the ways fine-pitch BGAs – those with pitches less than 0.4mm – affect six crucial aspects of printed circuit board fabrication: laser drill, laminate type, stackup, patterning (etch), solder mask and test (**FIGURE 3**). The ability and willingness of PCB suppliers to invest in the technology and equipment to support ever-finer BGA pitch designs can become a key differentiator in terms of their capability within the industry.

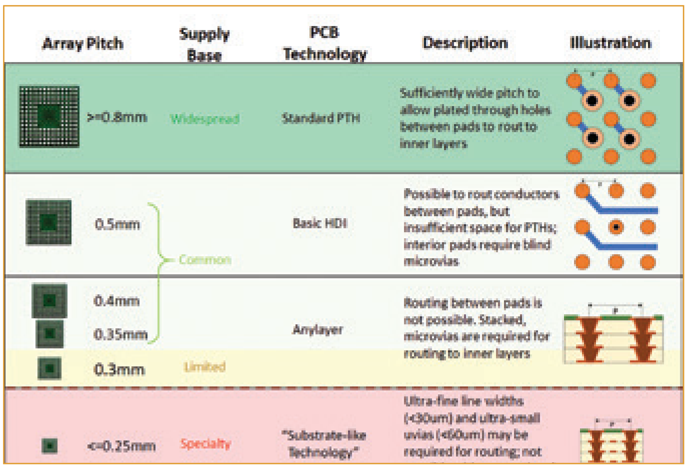


FIGURE 2. As BGA pitch gets finer, the PCB technology required to support it becomes more complicated, and the supply base becomes smaller.

FIGURE 1. Typical pitch ranges and structures of common grid array packages.

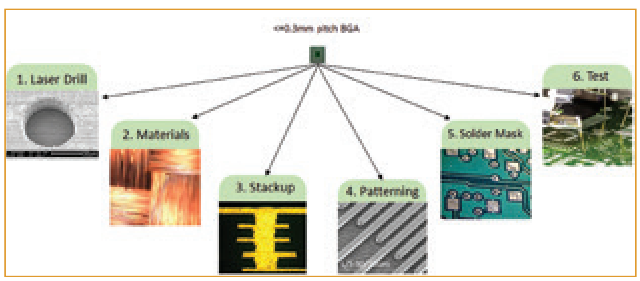


FIGURE 3. Fine-pitch BGAs, those with pitch ≤0.3mm, present challenges to PCB suppliers in six key areas of fabrication.

*For simplicity, the term BGA will be used generically in this paper to refer to any grid array package.

Laser drill. With BGA pitch of less than or equal to 0.4mm, it is generally not possible to route between pads. Therefore, via-in-pad is required to escape inner array pins to innerlayers; the finer the pitch, the smaller the pads, and therefore the smaller the required drill. A 0.3mm pitch array typically requires a 0.075mm drill size, which is often the lower limit of most conventional CO_2 lasers. Below 0.3mm pitch, smaller holes are needed, which generally require UV lasers. These types of lasers are more accurate and produce cleaner holes but are slower and thus more costly (FIGURE 4).

There are reliability concerns with stacked µvias 75µm and smaller, with evidence that stacked µvias, particularly when stacked four or more high, are susceptible to pad lifting during reflow processing and suffer premature failure.[2,3] FIGURE 5 illustrates a

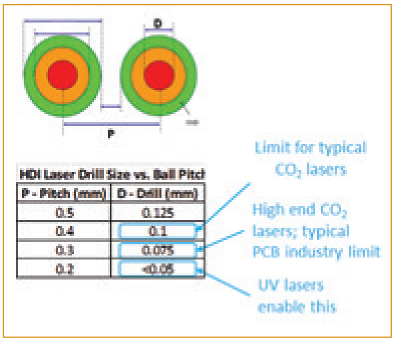


FIGURE 4. As array pitch decreases, the size of laser-drilled holes must decrease, but the laser drilling and plating process for µvias <75um is more challenging and the costs higher.

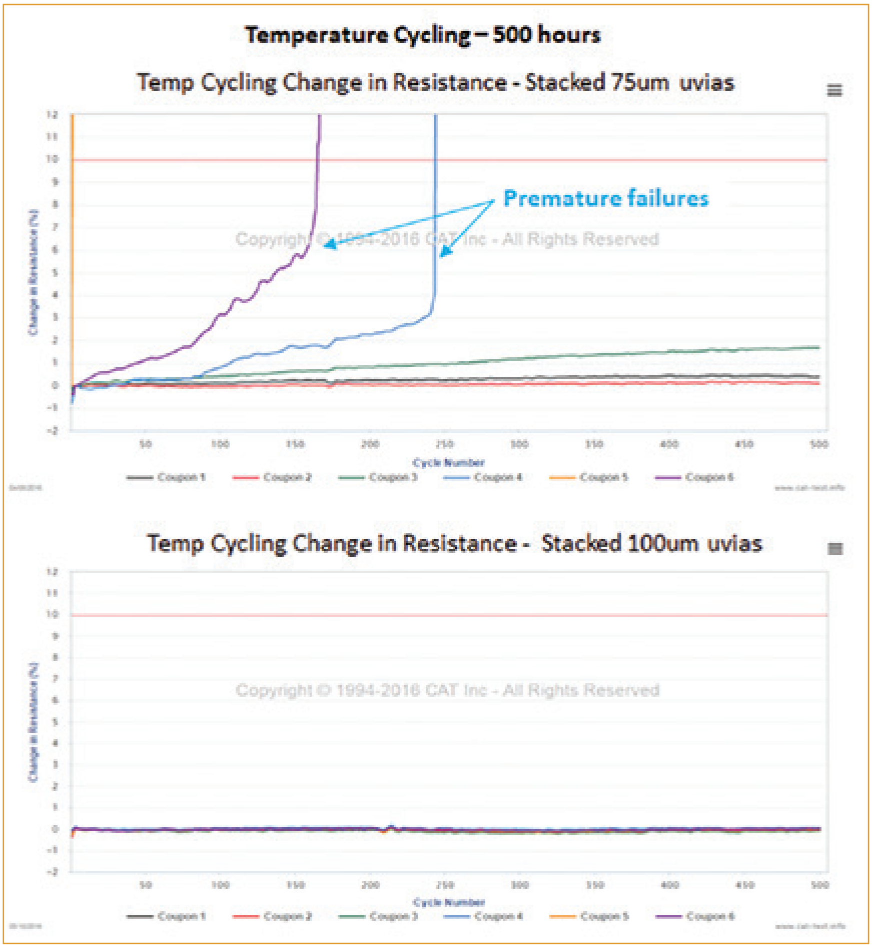


FIGURE 6. Stacked microvias 75µm in diameter experienced premature failures during temperature cycling after 6x reflow simulation, whereas stacked microvias 100µm in diameter similarly preconditioned exhibited good reliability.

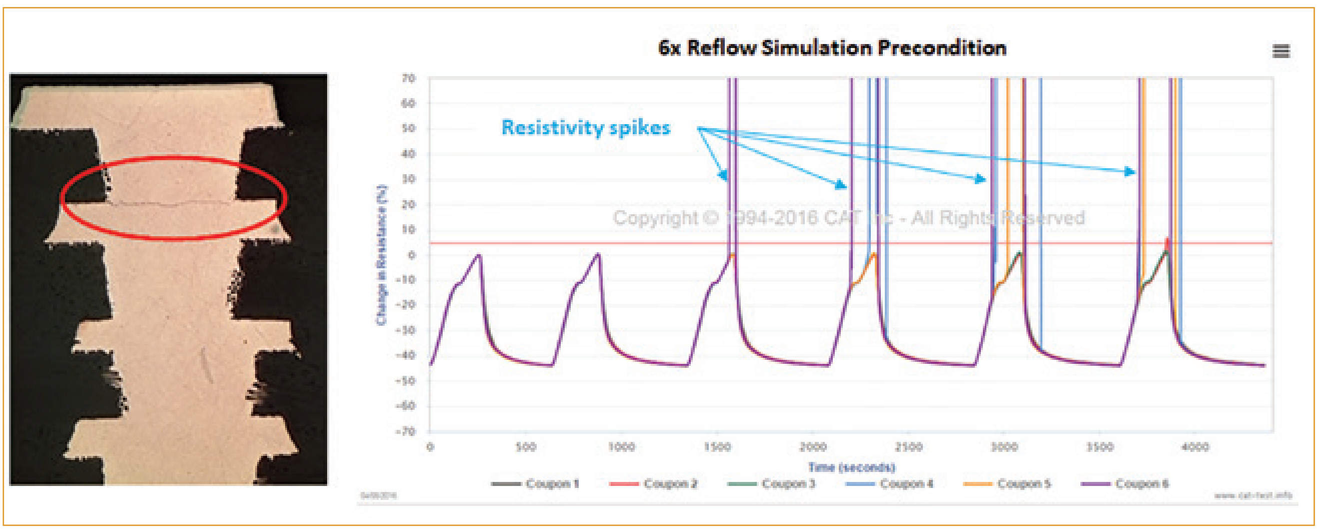


FIGURE 5. Stacked microvias 75µm and smaller are susceptible to pad lift during reflow and can pose long-term reliability risk as a result.

representative stacked µvia that lifted from the pad during reflow; this unit actually passed electrical test after reflow, indicating the via sat back down on the pad upon cooling. A shown in **FIGURE 6**, however, long-term reliability of the 75µm µvias was compromised, compared with 100µm µvias, which showed no failures during reflow or temperature cycling.

One solution when µvias 75µm and smaller are required is to stagger them wherever possible. When that is not possible, the second choice is to stack only two layers deep, as shown in **FIGURE 7**. Glickman, *et al*, have shown good reliability with 50µm stacked µvias when used with high-T_g laminate (T_g ~270°C) material in hybrid construction with standard laminate, as shown in **FIGURE 8**.[4]

Materials. Standard fiberglass weave patterns in conventional prepreg materials are characterized by tight glass fiber bundles alternating with open spaces that are filled in with resin, as illustrated in **FIGURE 9**. The laser ablation rate of resin is faster than that of glass. Therefore, the non-homogenous structure of standard prepreg materials can yield rough, inconsistent holes with poor size and location accuracy. These inconsistencies were especially pronounced with early generations of laser drills and had a significant impact on quality. Resin-coated copper materials, which do not use fiberglass cloth, were developed to solve this problem. RCC materials dramatically improved laser drill quality and offered ancillary benefits such as good dielectric performance. However, RCC materials are expensive, difficult to handle and have poor dimensional stability, so they are no longer common.

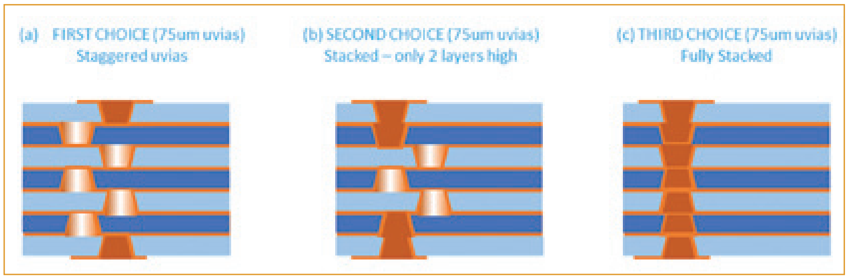


FIGURE 7. When microvias 75µm and smaller are required, it is advisable to avoid full stacked columns where possible to minimize the risk of lifted pad.

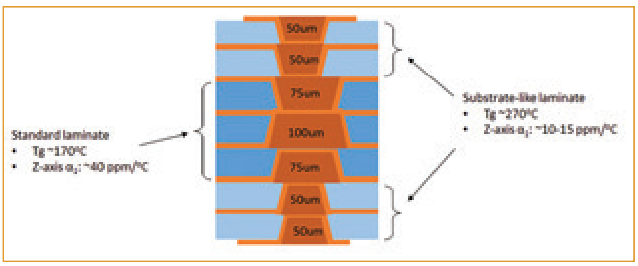


FIGURE 8. There is evidence stacked microvias as small as 50µm have good reliability when used with high-T_g laminate material in hybrid construction with standard materials.

Property	PrePreg Type		
	Conventional	Resin-Coated	Laser Drillable
Laser speed	red	red	yellow
Hole smoothness	red	yellow	green
Resin cracking	green	red	green
Image transfer	yellow	red	green
Dimensional stability	yellow	red	green
Thermal expansion	yellow	red	green
Thickness control	yellow	red	green
Surface smoothness	red	green	yellow
Handling	green	red	green

FIGURE 10. Tradeoff comparison table of conventional fiberglass, resin-coated copper and low-profile, laser drillable prepreg.

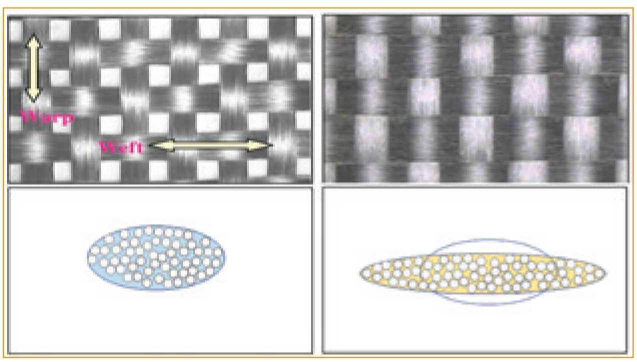


FIGURE 9. Standard square weave fiberglass (left) is characterized by distinct glass-rich vs. resin rich areas, which can negatively affect laser-drill quality; spread weave fiberglass (right) reduces this variation, thereby improving laser-drill performance, and provides a lower-profile glass bundle without changing the resin-glass ratio.

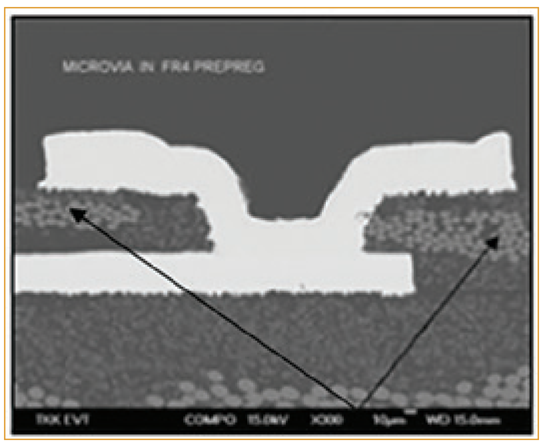


FIGURE 11. Lower-profile glass weave is required for small microvias to ensure adequate resin coverage, so the glass bundles do not contact adjacent copper.

Alternate fiberglass materials flatten the weave pattern to provide more even distribution of glass content across the panel, thereby facilitating consistent hole shape and accuracy during laser drill, without changing the resin-glass ratio. The spread weave can also improve signal integrity for high-speed lines because the resin-glass ratio is less variable, thus providing a more consistent dielectric constant. The lower glass profile of these laser-drillable prepregs offers another important advantage for small (<75µm) µvias: layer-to-layer spacing of small holes must be reduced to maintain acceptable aspect ratios for electroplating; the thickness of the glass bundle can start to approach the layer spacing, which can lead to insufficient resin coverage above and below the glass for bonding. Lower profile glass weaves help ensure adequate resin coverage to prevent glass bundles from contacting adjacent copper.

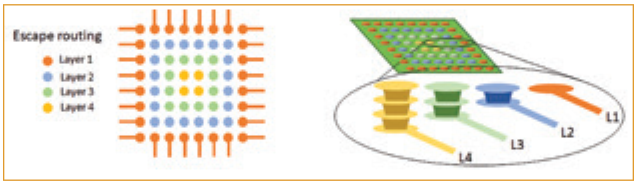


FIGURE 12. For fine-pitch arrays where routing between pads is not possible, microvias must be used to route interior rows to adjacent innerlayers. This requires "anylayer" construction.

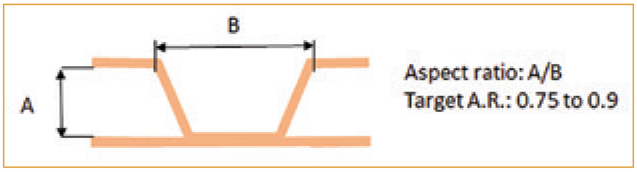


FIGURE 13. As microvia size shrinks to accommodate finer-pitch arrays, layer thickness must also decrease to maintain acceptable aspect ratios.

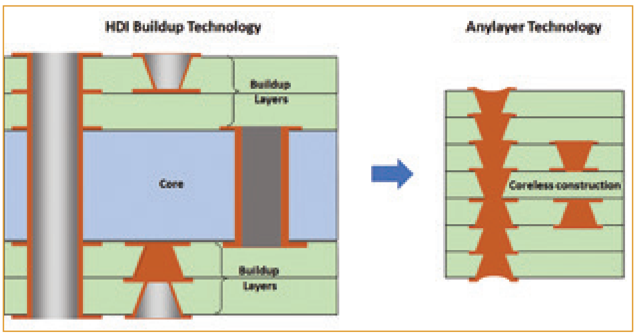


FIGURE 14. High-density arrays typically require anylayer construction to route.

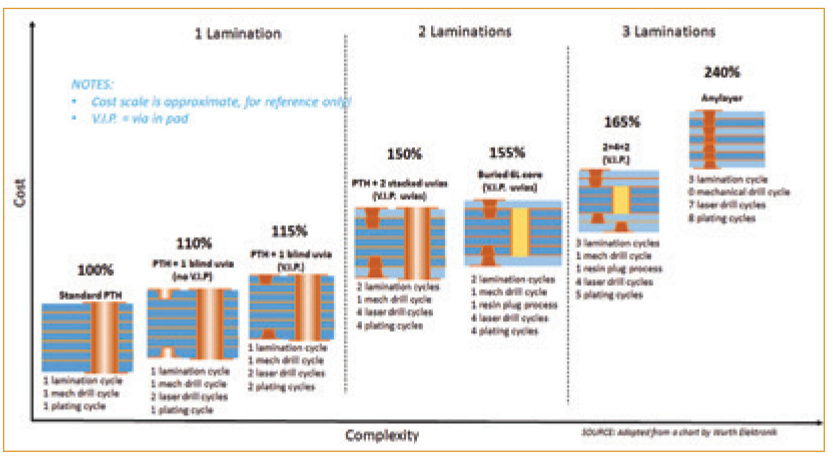


FIGURE 15. Blind microvias and sequential buildup technology, necessary for fine-pitch arrays, add complexity to the PCB fabrication process and have significant implications on cost.

Stackup. Because there is insufficient space to route conductors between interior pads of fine-pitch arrays, microvias must be used for routing these rows to innerlayers, as illustrated in **FIGURE 12**. For full arrays, this usually requires anylayer construction, in which blind microvias can be used on any layer, thereby providing full routing freedom. The larger the array, the more layers are required for routing.

This has direct implications on the stackup, not only driving layer count but also the overall thickness of the PCB. One of the critical design parameters of a microvia is the aspect ratio – calculated as hole depth divided by hole diameter – which governs the ability of the fabricator to plate the hole. Generally, the ratio must be less than 1:1, with a typical target of 0.75:1 (**FIGURE 13**). Thus, as ever-decreasing array pitches require smaller µvias, layer-to-layer thickness must also decrease to maintain acceptable aspect ratios.

With traditional HDI construction, the core layer is usually a C-stage (fully cured), rigid copper-clad laminate, and forms a structural backbone of the buildup, providing support during fabrication. But with anylayer technology, there is no traditional "core" layer for support, and the thin starting layers are fragile and not compatible with conventional processes (**FIGURE 14**). Anylayer technology, therefore, requires suppliers invest in specialized processes and equipment to fabricate coreless stackups and thin buildup layers, such as horizontal etching, vertical continuous plating, automated loading/unloading robots and other techniques to minimize processing and handling damage. It may also be necessary to process the center layer using a release backer that provides support throughout the initial processing steps and is then discarded upon the first lamination cycle.

Buildup technology used in HDI, especially anylayer construction, requires sequential processing, whereby each buildup layer must be processed through all of 10 to 15 steps sequentially. Each buildup sequence is thus nearly equivalent in terms of process time and resources as a single standard technology PCB. Fabricators that support high-volume anylayer technology require tremendous capital investment, particularly in bottleneck processes such as drilling and lamination where redundant equipment is essential to maintain volume capacity. **FIGURE 15** highlights the cost implications for anylayer designs.

Patterning. Ultra-fine pitch devices, those with pitch <0.3mm, may require routing between innerlayer pads. The typical line widths necessary to route between pads of fine-pitch arrays are summarized in **FIGURE 16**. Conventional imaging and etching techniques are insufficient to support these requirements. Line widths below 60 to 75µm generally require laser direct imaging (LDI) because standard phototools introduce too much variation due to alignment and resolution imperfections. Conventional etching, or subtractive technology, uses liquid etchant to remove unwanted copper. This technique produces undercut, since the etchant is in contact with the top of the trace longer than the bottom. With standard line widths, undercut has a negligible effect on signal performance at normal frequencies, but with line widths ≤40µm, undercutting the normal variation of the etching process can overetch lines and even remove them entirely (Figure 16).

Additive processes must be used for ultra-fine lines. The most common type is modified semi-additive patterning (mSAP). In this process, dry film is used to mask non-pattern areas, and the desired conductor pattern is exposed to electroplating. Thus, the pattern is built up rather than etched down. Figure 13 provides a graphical comparison on typical conductor shapes using subtractive vs. additive patterning.

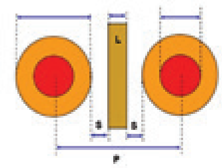
Solder mask. Liquid photoimagable solder mask, by far the most common solder mask process, has inherent process imaging, registration and thickness variations that can become significant when used with fine-pitch arrays. **FIGURE 18** shows an example of mis-registered solder mask on a BGA array exposed an adjacent conductor. Standard solder mask registration, which uses dry film and optical exposure for patterning, is ±75µm. This is acceptable for BGAs down to 0.5mm. For finer-pitch arrays, direct imaging is required, in which light energy exposes the desired pattern, which then resists the developer material. In addition to improving the imaging accuracy compared with photo-imaged dry film, many DI processes can expose isolated regions of a working panel and make real-time adjustments to compensate for alignment inaccuracies across the panel before exposing the subsequent region, as illustrated in **FIGURE 19**.

Inspection and test. Finer feature sizes present various challenges for conventional inspection and test processes, including the obvious difficulty of detecting and repairing small or minor defects that would otherwise be acceptable with conventional feature sizes, but which can be significant on fine-pitch designs. Conventional PCB inspection has traditionally relied on human operators, which is time-consuming and error-prone under the best circumstances. Automatic optical inspection (AOI) has helped automate the inspection process, and greatly improved speed and accuracy. It does not replace human inspectors; instead it identifies the type and location of defects detected and sends that information to the human operator, who can then focus on the areas of concern and qualitatively judge the severity and significance of the defects.

Automated repair systems improve the speed and accuracy of the repair process and can perform more complicated repairs than human operators, as well as provide the ability to repair opens, something not normally possible by operators.

Conclusion

The steady advances in semiconductor technology that have enabled increased functionality in increasingly smaller packages have facilitated astonishing product advances in every



P - Pitch	L- Line Width	S - Space
500	75	90
400	50	50-60
300	40	40-50
200	30	30

units: um

Lower limit for conventional imaging
Laser direct imaging: reliability concerns w/ conventional etch
Modified Semi Additive Patterning (mSAP)

FIGURE 16. Conductor widths required to route between pads of fine-pitched arrays. The photoimaging and chemical etching processes used in conventional patterning are insufficient for lines widths ≤50µm.

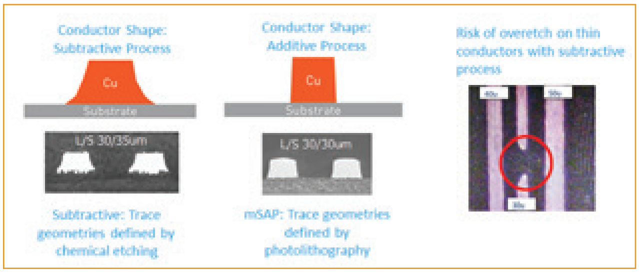


FIGURE 17. Subtractive processes (left) produce trapezoidal conductor shape due to chemical undercut; additive processes (center) are defined by photolithography, which produces straighter trace walls. Subtractive etching can overetch line widths ≤40µm (right).

FIGURE 18. Solder misregistration of a BGA pad array exposed an adjacent trace.

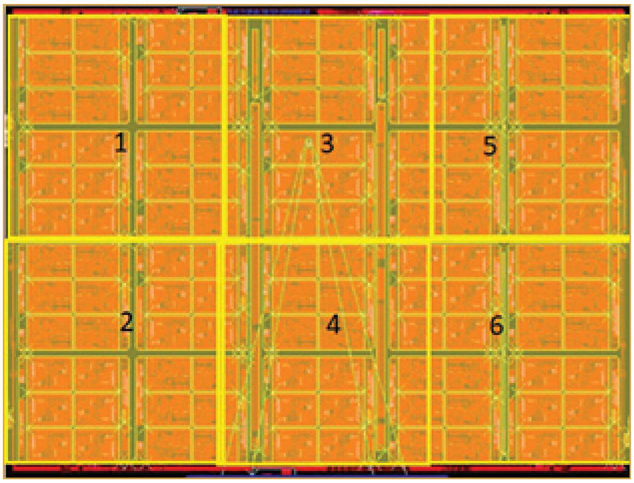


FIGURE 19. Advanced direct imaging equipment for solder mask exposure can expose a panel in localized regions and make real-time adjustments before exposing subsequent areas of the panel.

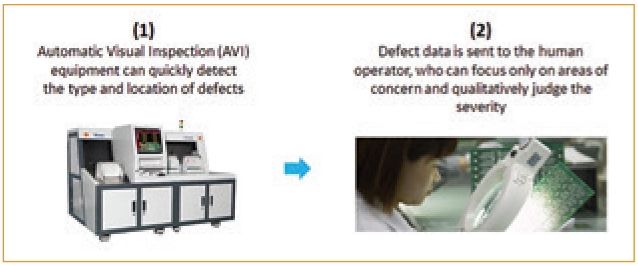


FIGURE 20. AOI technology does not replace human inspectors but helps them focus on areas of concern. (Source: Kaima PCB Inspection)

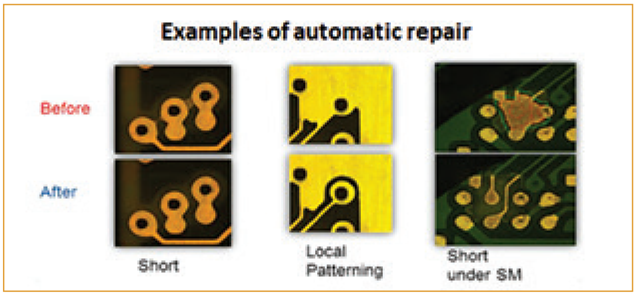


FIGURE 21. Automated repair systems perform repairs otherwise too complicated or small for operators.

sector of society but present unique challenges to the printed circuit board industry. In particular, the ever-decreasing pitch of BGA packages directly impacts most key PCB fabrication processes and requires significant capital investments. There is opportunity for suppliers willing and able to make the investments, but also risk: A recent slowdown in the smartphone market left the industry with a lot of idle mSAP capacity. If we've learned anything from the long journey in electronics miniaturization, it's the PCB industry is resilient and resourceful and always seems to stay one step ahead in the inexorable drive to make things smaller. □

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Can Tomorrow's A&D DESIGNS Handle the Heat?

New 3-D technologies with robust interconnects and thermal solutions are on the way. **by PETER M. CARTER**

Ed.: This is the fifth of an occasional series by the authors of the *2019 iNEMI Roadmap*. This information is excerpted from the roadmap, available from iNEMI (inemi.org/2019-roadmap-overview).

Aerospace and defense (A&D) products face several challenges unique to this particular market segment, including the extreme environments in which they operate, need for security, desire for reworkability, long duration storage requirements and the functional lifetime over which the products are expected to perform and be supported.

The critical issues for the A&D sector can be reduced to a list of 11 challenges that need to be resolved for efficient manufacture and reliable use of current and emerging commercial off-the-shelf (COTS) technologies in military form factors on military platforms. These are:

1. Affordability
2. Mitigating any risks associated with Pb-free products
3. Thermal management
4. Weight and size reduction
5. Increases in PWB density and complexity
6. Reliability and associated ruggedization of COTS technologies
7. Anti-tamper implementation
8. Component availability, obsolete part strategies
9. Configuration control
10. Testability (and reworkability)
11. Component authenticity (counterfeit concerns).

The industry's move to Pb-free electronics poses several issues for A&D products. These include: 1) the long-term reliability of Pb-free solder alloys, 2) potential for tin whiskers and the required risk mitigation options, and 3) logistical issues associated with the declining availability of Pb-based components, configuration control, and depot and OEM maintenance and repair issues. Most A&D companies have at least a short-term strategy of continuing to provide Pb-based products while their supply chain is transitioning to Pb-free. Many customers are requiring formal Pb-free control plans (LFCPs) to protect against the unintended intrusion of Pb-free materials into their products. LFCPs require formal process changes that will, when implemented, identify any Pb-free finishes or solder alloys in the product's design, assess its risk to performance and reliability, identify appropriate risk mitigation controls, implement controls that mitigate the risks, flow-down control requirements to the supply chain, and monitor incoming materials. One mitigation approach, for example, used by many military OEMs is to reball Pb-free BGAs with eutectic SnPb solder balls. This is an expensive approach.

Availability of components with either traditional eutectic SnPb solder balls or without solder balls would be simpler, but limited A&D volumes disincentivizes the component producer or drives greatly increased costs (and associated consistency risks) for a low-volume "defense-custom" alternative.

In A&D products, heat associated with power dissipation has traditionally been handled by passive conduction. The typical thermal path is from the component to the heat sink frame through "wedge locks" to the chassis. In the future, these conventional thermal management techniques will be inadequate. Improvements are required to reduce the thermal resistance across the wedge lock. Air and liquid "flow through frames" will be required, or changes that permit conduction cooling. These changes will require a significantly colder thermal interface for the assembly that is not always practical. These new thermal management designs must be assessed for their impact to interconnect reliability, testability and reworkability.

Component changes that increase the maximum allowable junction temperature would simplify board layout from a thermal perspective. However, the issues associated with thermal management may still become the biggest single roadblock to using some emerging technologies.

Uprating of commercial components is one method to meet thermal challenges, but not always affordable. Improvements in the thermal management approach and both bulk and interface materials will be required. Nanotechnology material improvements are needed to reduce thermal resistance at the component interface. These improvements will not only reduce the operational temperature of components, but also improve product MTBF and its expected service life. Work is ongoing to produce electronics that can withstand very high temperature operation, but cost, maturity and reliability concerns are still being addressed. The deep well industry is a source of new work in this area due to the extremely high-temperature environment.

Weight is extremely critical to the lifecycle cost of space and avionics systems. Weight reductions provide greater range, greater payload capacities, and significantly reduce operational cost of the platform. While significant opportunities reside with the platform structure, there are many additional opportunities in the domain of the electronic assemblies. It is anticipated both weight and size of MIL/AERO products will continue to decrease. Use of lightweight composite materials, including evolving nanotechnology materials, to replace conventional metals must continue to be evaluated, tested, and implemented. In many cases these materials provide not only weight reductions but also improvements in other critical areas such as thermal management. These opportunities need research and must mature to high-technology and high-manufacturing readiness levels. Expansion of 3-D technologies with robust interconnects and thermal solutions compatible with A&D product constraints is one area where weight and volume savings will be realized in the next few years.

Continued evolution is required at the PWB level to permit circuit routing of emerging array components. These design, material and process changes need to be defined, developed, tested, and implemented. In some cases, requirements for digital and RF PWBs are converging. Most PWBs currently have surface-mounted components attached to both top and bottom surfaces. This has roughly doubled the board wiring density. Many new design features common to leading-edge high-density commercial products will be required for military products. Microvias (including via-in-pad) are required to facilitate wiring of high I/O fine pitch area array components, and multiple layers of stacked microvias are also needed to achieve the proper electrical performance for high frequency and increasing wiring density. These features will become more prevalent over the roadmap period. Electrical performance will drive signal integrity requirements, resulting in the need for improved impedance control and power integrity distribution requirements, which in turn will require embedded capacitance layers. In general, PWBs will have smaller plated through-holes; finer lines and spaces; a variety of buried, blind and microvias; and contain multiple types of laminate materials, each providing a unique function (i.e., capacitance, resistance, thermal dissipation). Recent automotive electronics developments involve place and embedding of 01005 and 0201 discretes within a PCB.

A&D customers require and expect COTS components and assemblies. Many of these technologies are not, as procured, demonstrated as capable of performing in harsh military environments for long periods of time. Pb-free initiatives make this challenge more complex. Tools and models are needed to identify when ruggedization is required and to validate its adequacy. The design modifications must be producible, of minimal impact to testability and reworkability, and affordable.

Anti-tamper (AT) and counterfeit avoidance, particularly malicious-intent counterfeit component and material insertion, is being increasingly required to prevent or at least delay exploitation of critical technology on military systems. Implementation of AT will require development of unique materials that can be applied within a secure infrastructure. Technology cycles and obsolescence continue to be a challenge to A&D products. Fundamentally, A&D products are developed for a specific customer, whereas COTS products are developed for a general market.

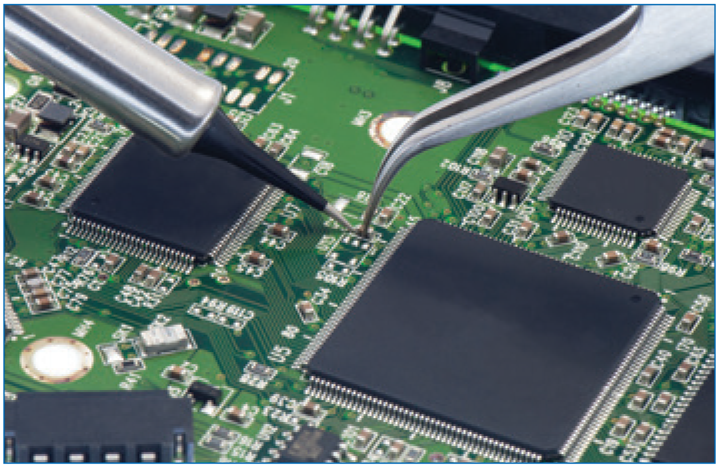

FIGURE 1. A&D customers want COTS parts, but many aren't ruggedized or pose reworkability issues.

In many cases, the time to develop a product to a military customer's specification and then perform some level of qualification testing (even highly accelerated life testing) is long in comparison to the planned lifecycle of its COTS components. There may be instances where COTS components become obsolete before the system goes into production. In addition, the designer must take into consideration the issue of spare parts availability and support over a typical military product lifespan of 10 to 30 years. Procuring end-of-life components increases the risk of counterfeits. Typical A&D products require both forward and backward traceability and stringent control of material and process change. This is not typically as closely controlled with COTS products. Again, with the transition to Pb-free components, configuration control of procured PCB assemblies and systems is more complex than in previous roadmaps.

A&D products require significant environmental stress testing prior to final customer sell-off and delivery. These tests consist of "shake and bake" testing, where the product in its final configuration is electrically tested over both accelerated temperature cycling and vibration that simulate a small portion of its operational life in the field environment. Prior to this phase of the production process, assemblies are conformal-coated and all thermal management completed (heat sinks attached, thermal interface materials added, etc.). It is critical that any problems detected at this level be diagnosed quickly to the component level for repair. To facilitate this, the design and test strategy must enable detection of issues as early in the manufacturing process as possible, where both fault isolation and repair are simpler. This emphasizes the importance of optimizing the test strategy relative to in-circuit or flying probe test, boundary scan test, and various emulators that permit increased levels of functional testing earlier in the manufacturing process. For failures detected at the final environmental screening, however, it is important to accurately and quickly diagnose the failure and be able to rework or repair product efficiently.

The issue of counterfeit parts is common to the entire electronic products domain, so it is certainly an issue to A&D products. The obsolescence issues associated with the production lifecycle, and certainly the sustainment phase of A&D products, magnify the issue. As described earlier, controls must be in place to avoid exposure to counterfeit parts, detect any suspect parts, and mitigate the risks of receiving counterfeit parts. New U.S. government rules levy the liability directly on the OEM for counterfeit parts in their products from any level in their supply chain. This ruling is being enforced, and the consequences are dire enough that an entire industry related to counterfeit part detection is rapidly expanding. ❑

PETER M. (MARC) CARTER of Aeromarc LLC chaired the Aerospace//Defense Product Emulator Group (PEG) chapter of the 2019 iNEMI Roadmap.

CLEANING AND DRYING before Conformal Coating

The steps involved in manual and automated contamination removal. by **EMILY PECK**

Printed circuit boards are subjected to many harsh environmental conditions, including extreme temperatures, strong chemicals, corrosive salts, dust and moisture. Encapsulating them with a protective conformal coating makes sense. Conformal coatings keep harmful elements from touching delicate components and degrading performance of the boards. However, for optimum PCB longevity, functionality and reliability, it is imperative boards are perfectly clean and dry before conformal coating.

PCB contamination comes from many sources: transport, handling, storage and manufacturing. The most common examples of PCB contamination are fingerprint oils and salts, flux residue, tape or other adhesive residue, solder balls, and even some inks or chip bonder.

Any contaminants or soils on PCBs may interfere with the proper bonding of the conformal coating to the PCB substrates. Salts or oils from fingerprints left on the boards can cause defects in the conformal coating (**FIGURE 1**). These include uneven coverage, pinholes, craters, blisters and fisheyes.

In addition, flux residue absorbs and holds moisture. If residue is sealed under the conformal coating, it will likely cause cracking and peeling when the conformal coating is cured and the trapped moisture releases. If that compromised board then makes it into the field, dust, water and salts can penetrate it, resulting in a variety of damage, including delamination, parasitic leakage, dendrite growth, electrochemical migration and shorting. In extreme conditions, it may also result in complete component failure. To prevent performance problems, cleaning the contaminants and drying the PCBs prior to conformal coating is essential.

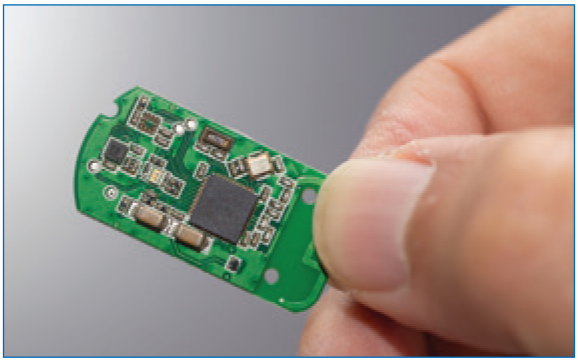

FIGURE 1. Fingerprint oils and salts must be removed prior to conformal coating.

Clean and dry before coating. Typically, the cost prevents many manufacturers from cleaning and drying before conformal coating. Those steps may seem like an unnecessary expense due to the extra time and cleaning fluid costs involved. However, cleaning and drying prior to coating improve PCB life-expectancy and reliability. They also help prevent unpredictable board performance, costly PCB failures, disruptive product recalls and expensive product returns, not to mention the added time and expense of removing a conformal coating to rework a malfunctioning PCB if it fails due to environmental exposure. So, cleaning and drying are typically worth the extra investment in time and materials.

Two of the more popular methods of cleaning and drying PCBs are either manual cleaning at the benchtop or automated cleaning using a vapor degreaser.

Benchtop cleaning and drying. There are four steps to successfully cleaning PCBs at the benchtop: wet, scrub, rinse and dry (**FIGURE 2**). These four steps ensure a good conformal coating adheres to the PCBs, cures without damage, and resists delaminating when exposed to extreme conditions. First, wet the board with a pure cleaning fluid. Second, scrub it using a good quality scrubbing brush. Third, rinse away any byproducts with more clean fluid. The final and fourth step is to dry the PCB completely to prevent moisture from being trapped under the conformal coating.

Manual drying is accomplished in a few different ways during benchtop cleaning. One of the common methods to dry PCBs is with a simple lint-free wipe. Gently push the wipe

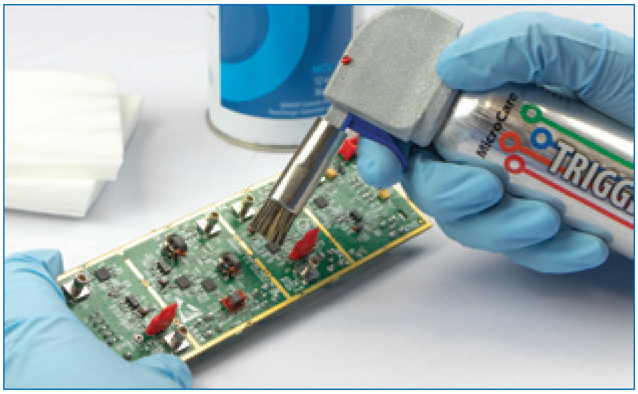

FIGURE 2. The four steps to successfully cleaning PCBs at the benchtop are wet, scrub, rinse and dry.

under low-mounted SMT components to absorb any excess spray of cleaning fluid. Or clean and dry at the same time by scrubbing components through a wipe placed on top of the board. Another way to dry PCBs before coating is with a dust remover. This can be a quick and effective way to blow out trapped moisture from underneath larger components that a wipe alone may not reach. The dust remover can be targeted to a very precise area on the PCB and works well to eliminate moisture in hard-to-reach areas of the circuit board. In addition, combining a duster with a wipe will double the drying power and prevent the fluid from being pushed back onto the board, spreading contaminant around.

Vapor degreaser cleaning and drying. As PCBs continue to shrink in size due to the demand for smaller electronics, manufacturers are squeezing multiple micro-components like flip chips, µBGAs and CSPs into tighter spaces on the boards. Low-standoff components like Mosfets and bottom-termination packages like QFN (quad-flat no-leads) are now commonplace. As a result, these tiny, stacked, high-density and complex PCBs are more susceptible to functionality problems, especially if exposed to harsh conditions. So, good cleaning and conformal coating is an absolute necessity.

But the dense construction of these PCBs makes them hard to clean and even more challenging to dry. Cleaning fluid can get trapped under these components, leaving the PCBs dirty, at risk of cross-contamination and unprepared for conformal coating.

A solution for effectively cleaning small, complex PCBs is to use a vapor degreaser and a modern, sustainable cleaning fluid. Vapor degreasing uses cleaning fluid immersion, combined with vapor rinsing and vapor drying, to remove all types of contaminants, including fluxes, pastes, particulates and residue (FIGURE 3). The fluid gets into and under all components, but more important, it gets out of the tiny channels between stacked components.

Vapor degreasing machines range in size from small benchtop models to huge floor systems. No matter what size vapor degreaser is used, the cleaning and drying processes are the same. The vapor degreaser boils a cleaning fluid at a low temperature, usually between 40˚C (105˚F) and 65°C (165°F), to produce a pure, clear and dense vapor blanket. PCBs are lowered into the boiling cleaning fluid in the boil sump to heat, loosen and remove most contamination. They then move to the rinse sump, where any vestige of contamination is rinsed away. Finally, the PCBs are raised and held inside the vapor blanket, where the parts dry and cool. The entire process takes approximately six to 20 minutes per batch.

The cleaning fluid has a low surface tension, permitting it to permeate the entire board, including under and between tightly spaced components to wash away fingerprint oils, fluxes and residue. A low-temperature fluid minimizes risk of damage to components, and since the cleaning fluid is ultra-pure, it leaves no residue behind.

The vapor blanket dries PCBs quickly. The vapor passes under the low-mounted components, so the PCBs come out of the vapor degreaser dry and cool enough to handle. This is important since PCBs need to be cool to help the conformal coating adhere to the board.

Removing conformal coatings. If necessary, conformal coatings can be removed for board rework and repair. Removing conformal coatings is challenging, however. They are designed to be durable and, by nature, hard to remove. If rework is required, the best way to dissolve the conformal coating is to use a cleaning fluid with a chemical composition similar to the contamination. For example, silicone conformal coatings offer great protection, while being light, durable and easy to rework. For silicone coatings, choose a remover that is siloxane-based, so it is chemically very similar to the silicone conformal coating.

Acrylic, epoxy and urethane coatings are more difficult to remove. They often need stronger, more aggressive cleaners and may require soaking to soften the coating before removal. Other conformal coatings, especially those used in military applications, are rock-hard and simply cannot be removed chemically. They often require physical abrasion like sandblasting, which can damage the PCBs.

For reliability and functionality, ensure PCBs are clean and dry prior to conformal coating. By properly preparing the PCBs prior to coating, manufacturers ensure optimized production yields, throughput and quality, and also avoid the major costs of coating removal and PCB rework. □

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FIGURE 3. Vapor degreasing uses cleaning fluid immersion, combined with vapor rinsing and drying to remove contamination.

Screen Printing Hacks: Cleaning Small PCBs

Is a wet cycle necessary after every print? Maybe not.

IN THE PREVIOUS installment of screen printing hacks, we discussed some proven workarounds for alignment issues. This month – and based on some recent customer observations – the advice centers on understencil cleaning, how lack of control can adversely impact this sub-process of printing and the overall result, and a few suggestions for correcting the problems.

Here's the backstory: A customer printing very small dimensions – 200µm square apertures with spaces of 130µm, on average – was experiencing sub-4 Sigma results on some NPI designs. Transfer efficiency was low, and there was a large standard deviation across devices and the PCBs, so a lot of inconsistent paste-on-pad volume. Our team developed new stencil designs and tested them in a lab environment with our SPI, yielding excellent results. After making some machine calibration adjustments onsite at the customer and integrating the new stencils, however, there still wasn't tremendous uptick in the process; improvement was observed but not at the expected level. Let the troubleshooting continue! We turned our attention to the cleaning process.

As is the case with many customers printing very small consumer product boards, protocol is to run an understencil clean after every board is printed. Unfortunate as it is, that's today's reality, given the tight dimensions and the impact of board stretch. In this situation, the cleaning routine run after every print was a wet-vac-dry, which is arguably a fairly aggressive approach. If the parameters on this setting aren't precise, issues such as those we observed can contribute to a lack of process stability. First, we noted the understencil cleaning roll paper was saturated with solvent, even on the indexed areas for the vac and dry cycles, so too much solvent was being applied, and the paper quality was such that the solvent wicked over a broad area. In addition, the cleaning system needed to be leveled to bring it back to spec, and there were some paper feed issues with the cleaning roll. Finally, we recommended taking a less aggressive approach and running dry wipes at a certain frequency in between the wet-vac-dry cycles to maintain stability.

If you suspect the understencil cleaning process may be contributing to less-than-acceptable results, try these remedies.

- **Adjust cleaning cycles and frequency.** Our company's screen printers provide up to six options for cycle combinations on the cleaner. As in this customer's case, a wet cycle may not be required after every print and, in fact, could be contributing to inconsistent paste release. While very tight dimensions may dictate a clean after every print, try using a dry-only cycle until the SPI indicates a more aggressive routine should be implemented. Then settle on that sequence frequency. The goal is to remove debris without adding much cycle time or introducing instability. New self-learning technology can make initial recommendations on cleaning parameters and ensure the process stays in check during production.
- **Analyze cleaning parameters.** It's not only about the sequence; multiple cleaning system parameters need to be optimized. Pressures, speeds and valve open times are all critical. If too much solvent is delivered to the paper, your wet-vac-dry could turn into a wet-wet/vac-wet, and then all bets are off. Ensure the characteristics of the solvent are aligned to the paper and how it wicks, so a dry wipe is indeed dry. (IPA has been known to contribute to solder slump and solder balling.)
- **Confirm quality of inputs and consumables.** Let's all say it together: "Good inputs equal good outputs." That's my mantra, as you know, and is as true for cleaning as for any other process. High-quality fabric and cleaning chemistries that enhance (instead of undermine) the process – especially with these ultra-small dimensions – are critical. Some understencil fabrics are lint-free, are constructed to trap solder paste particles, instead of smearing them, and help control contamination. Similarly, cleaning solvents should be highly compatible with solder flux chemistry. Less expensive does not always mean less costly!
- **Verify understencil paper positioning and indexing.** Understencil cleaning systems require some manual intervention to reload paper, manage solvent, etc. Naturally, this takes time and can be prone to error. If the paper isn't loaded properly, for example, it will not present as flat to the stencil, which may result in the stencil not being thoroughly cleaned. Operators should confirm the paper is correctly positioned, so flatness is maintained and indexing occurs as intended.

Ultimately, by addressing paper roll indexing issues, modifying cleaning cycles to introduce dry cycle sweeps in between the wet-vac-dry routine, and optimizing solvent quantity deposited, our customer's NPI assembly returned to 4-Sigma performance, and we are aiming to improve even more. ❑

CLIVE ASHMORE is global applied process engineering manager at ASM Assembly Systems, Printing Solutions Division (asmpt.com); clive.ashmore@asmpt.com. His column appears bimonthly.

Recent Advances in PCB Manufacturing Equipment

More lasers and improved and integrated software have factories humming.

THE METHODS AND equipment used to fabricate PCBs are becoming increasingly advanced and centralized. For example, computers, lasers, and AI are ever more common in all areas of PCB processing. In recent years, a considerable number of PCB manufacturers have invested heavily in the integration of the complete shop, with all equipment controlled by one central computer. The interconnection enables quicker file processing, higher accuracy, and improved yields.

One of the most expensive pieces of production equipment is the laser-direct imaging system (LDI), which has made significant improvements in accuracy, speed, quality, and in reducing overall manufacturing rejects. The newer models feature multiple cameras to locate lamination holes, compare them to the original Gerber file, then digitally scale the image to fit the panel. Newer laser imagers are capable of imaging down to 15µm line widths and spaces.

CAD/CAM software (computer-aided design and computer-aided manufacturing) is used to design and manufacture prototypes, finished products, and production runs. An integrated CAD/CAM system offers a single complete solution for design through manufacturing. From the beginning of a new PCB order, CAM software is used to inspect Gerber files, perform a design rule check, and identify trace or hole violations that could result in shorts or opens later in the process. The software checks impedance throughout the circuit traces and layers. It adjusts for laminate shrinkage by calculating scaling and resizing each layer to compensate. The software calculates etchback on traces and optimizes the job for maximum yield.

The software then coordinates feedback from post-lamination alignment and x-ray drilling and adjusts each layer's scaling in a database to ensure tight layer-to-layer alignment. The software then sends all the relevant information to the drills, routers, testers, imaging equipment and any other machines connected to the company's own intranet.

One major change has been the addition of laser technology to many operations and machines, from laser drills that sculpt through laminate, to lasers that cut to specific programmable depths to create blind microvias. Excise lasers built into automatic optical inspection (AOI) units can easily remove small shorts, and new technology even permits 3-D printing of copper to repair opens in the circuit, greatly improving yields.

Computer controls enable higher accuracy in the alignment of innerlayers by detecting errors in scaling with x-ray imaging and then correcting the drill files to correctly align tooling holes for lamination and drilling.

As such, today's drills are much superior to the machines of only a few years ago. They now offer laser drill size detection, broken bit detection, and feature drill canisters that automatically change bits due to wear or hit counts. These drills feature controlled-depth drilling for backdrilling of vias to reduce capacitance and improve impedance. Newer drills feature very high-speed drilling – up to 250,000rpm – with air-bearing heads and very accurate table servos. In addition to typical mechanical drilling, manufacturers use laser drills, powerful UV lasers that cut through copper and laminate to form microvias one or two layers down; thicker copper stop pads are used to halt the laser. Laser drilling is essential for HDI or very fine-featured PCBs.

To improve innerlayer drill registration, as mentioned earlier, x-rays look inside the PCB for special alignment pads that may have been compromised and then find the best location for the pads. The software subsequently calculates for stretch or shrinkage in the panel's size after lamination, and automatically adjusts the drill file size by using scaling and drill alignment holes so the drill will more accurately find the center for all pads. The machine will communicate with the drill, giving it new x-y and offset stretch coordinates to increase or decrease the data file position and size of the panel for greater accuracy.

Inkjet solder mask labeling units have replaced the outdated, messy and inaccurate silkscreen method. The machine has multiple inkjet heads that quickly spray accurate lines, letters and drawings in white ink on the finished solder mask. A powerful UV lamp dries and cures the ink as it is applied to the PCB. This eliminates the mess and issues associated with silkscreen application; e.g., the flip table, squeegee, etc.

Computers now control plating bath chemistry through constant monitoring and titrations. They may sense a deficiency in one of the many chemicals, for example, and automatically add the right amount of specific chemicals to correct the bath. Measuring and adjusting are performed in real time. Chemical baths do not suddenly go out of spec; therefore, important parameters such as copper ductility remain well-controlled.

Inkjet solder mask units have two different methodologies. Older ones spray the entire board, which is

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then imaged with an LDI and developed, then cured. Newer inkjet solder mask units apply the mask ink directly on the board, with openings for vias. A powerful UV light then cures the solder mask.

Lab computers enable quicker cross-sections and easier spotting of potential problems before boards are shipped. Computerized tracking using barcodes and/or QR codes show in real-time which jobs are behind schedule.

Newer flying probe electrical testing is much faster than the old systems, and is especially cost-effective for high-mix, low-volume production. The improved speed and accuracy eliminate the need for older fixed-bed ICT custom fixture-based testing, which is expensive, not cost-effective for short product runs, and requires much longer lead times to create the custom fixtures.

Laser-cutting quickly and very accurately shapes and cuts flex circuits, eliminating the old kick press and steel rule die method.

All fabricators seek to reduce costs, but a PCB fabricator lives or dies on its yields. A single LDI can cost well over a million dollars, but the payoff can be tremendous. In the past, a 70% yield was a sign that a fab shop was doing well. Today, with increased automation in manufacturing, shop yields are 90% and up. ❑

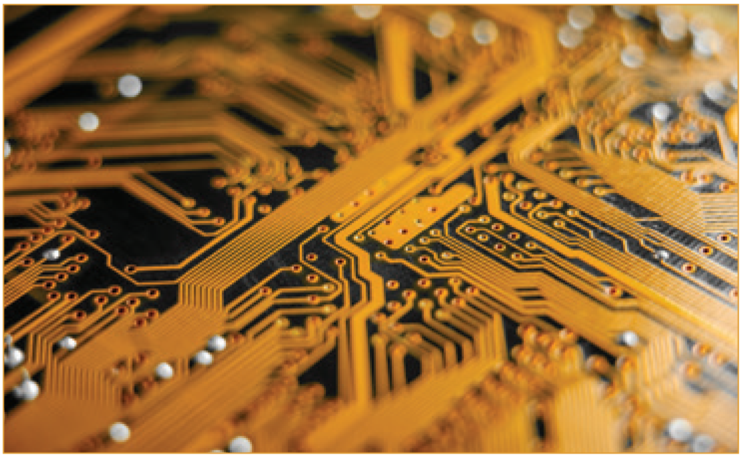


FIGURE 1. Advancements across a range of fabrication processes have boosted yields.

SMD CERAMIC FUSE

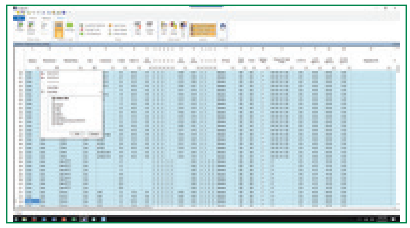
UMT-W is pulse-proof and has time-lag tripping characteristics. Is suitable as fail-safe device in demanding applications. Cuboid shape (5.3mm x 16mm). Comes in five rated currents from 5A to 20A and reaches rated voltages of up to 125V AC and DC, with breaking capacity of up to 1000A.

Schurter Inc.
schurter.com

BACK-FLIP FPC/FFC CONNECTOR

TF13 series features 0.4mm pitch, 0.9mm height, and 3mm mounting depth. Actuator is closed and protected before being mounted to PCB. Combined side-catcher, back-flip design provides greater FPC retention force. Side catcher prevents misalignment and ensures correct mating. Prevents solder wicking and flux penetration.

Hirose
hirose.com



STACKUP PLANNER

Z-planner Enterprise 2019.2 field-solver-based stackup planning and material selection software is optimized for front-to-back PCB design and signal-integrity flow. Enables design and validation of PCB stackups. Provides interfaces to common PCB layout and SI design flows, and large dielectric materials library.

Z-zero
z-zero.com

OTHERS OF NOTE

DYNAMIC BOUNDARY SCAN

XJTAG 3.10 introduces automated method for dealing with design updates that occur on board being tested. Intelligent device-matching algorithm analyzes new netlist and identifies devices with changed reference designators. Copies categorization information to new project and automatically updates all references to them.

XJTAG
xjtag.com

LOW-CTE LAMINATE

IS550H is CAF-resistant and comes in 2 to 60 mil (0.05 to 1.5mm) thicknesses. HTE Grade 3 and reverse treat copper foil; copper weight of 0.5 to 2oz. (18 to 70 µm). Tg is 200°C, Td is 400°C, Dk is 4.43, and Df is 0.016. Is for high-power and high-voltage applications.

Isola
isola-group.com

GROUNDING CONTACT FILM

PI gold conductive polyimide film has components of gold sheet over foamed gasket, SMD gasket and gold conductive tape, to be applied to smartphones and TVs. Comes in thicknesses of 12.5µm/25µm+. Sputtered seed (Ni/Cu alloy) + copper layer + gold layer: total thickness is 1µm/28µm. Electrical resistivity is 0.01-0.03ohm/sq. in.

Juyoung International
jyiemi.com

5G LAMINATE

TerraGreen 400G high-speed, low-loss laminate is halogen-free. Novel resin system is Pb-free-compatible and can be processed using standard PCB equipment and processes. Comes in 2 to 18 mil (0.05 to 0.46mm) thicknesses. Tg is 215°C, Td is 410°C, Dk is 2.9, and Df is 0.0018.

Isola
isola-group.com

POWER DEVICE VERIFICATION

Rohm Solution Simulator web simulation tool simultaneously verifies power devices and ICs on 44 different solution circuits. Performs complete circuit verification of power devices and ICs; validates SiC devices and gate driver ICs for driving SiC. Carries out simulations from initial development that involve component selection and individual device verification to system-level verification stage.

Rohm Semiconductor
rohm.com/solution-simulator

LOWER-WATER DIRECT METALLIZATION

Onyx is for high-reliability and complex PCBs. Is used in horizontal conveyorized equipment or in vertical immersion mode. Can process array of resin materials, including PTFE, polyimide, BT, flex, and epoxy-based resin systems. Is alternative to electroless copper deposition. Reduces water consumption to 4-6 gal./min. Contains no chelator.

RBP Chemical Technology
rbpchemical.com

5µM SPI

VP-9000 3-D SPI detects and relays data to printer. Multiple inspection switch has three resolutions (e.g., 15µm/7.5µm/5µm) for detailed and high-speed inspection. Automatic warpage compensation; programming in 3 min.; inspection capacity up to 8900mm^2/s.

Omron

inspection.omron.eu

HIGH-SPEED ROUTER

SAMCT34XJ high-speed router supports panels up to 400mm x 300mm. Cutting position is automatically adjustable. Easy-teach programming aided by on-board camera. Router bit height can be automatically switched for longer tool life. Repeatability +/-0.01mm.

Sakaya

sayaka.co.jp

Seika Machinery

seikausa.com

MEMORY MODULE AOI

3-D MX3000 final vision inspection system has two high-res multi-reflection suppression-enabled sensors; enables accurate, dual-sided final vision inspection. Identifies and rejects multiple reflections caused by shiny and reflective surfaces. Automation-ready.

CyberOptics

cyberoptics.com

OTHERS OF NOTE

MICROSCOPE EDITING SOFTWARE

Inspectis software 5.0 offers overlay features, including a built-in DXF creator and editor for producing scaled overlay graticules. Creates DXF file from object by optical edge detection; opens existing DXF CAD file, edits, draws patterns, shapes, adds text and overlay on live image; saves in DXF or PNG format and displays as digital graticule on live image. Provides tools for calibration of device magnification.

Inspectis

inspect-is.com

HIGH-TEMP. DIE-ATTACH EPOXY

Master Bond EP17HTS-DA is a one-component, no-mix, electrically conductive die-attach epoxy. Ag-filled system maintains Tg of 140°-150°C. Passes MIL-STD-883J thermal stability requirements at 200°C. Die shear strength is 35-40kg-f at room temp. Meets NASA low outgassing specifications.

Master Bond

masterbond.com

PARALLEL FLASH PROGRAMMER

SP08 performs fast onboard programming of PCB assemblies. Reduces functional test programming from separate test software and field software iterations to a single step.

Test-OK Systems

test-ok.nl

PROGRESSIVE CAVITY PUMPS

Vortik series have process controls for mass flow control and automated ratio control system for mixing two-component fluids. Include models for dispensing one-component (1K) and two-component (2K) fluids such as conductive epoxies, solder paste and adhesives. Flow rate of 0.2µl per sec.; produce lines narrower than 30µm.

Nordson Asymtek

nordsonasymtek.com

HIGHLY VISCOUS LIQUID DISPENSING

UltimusPlus air pressure fluid dispenser applies various liquids in manual and automated production processes. Comes with high-resolution touch screen to configure dispenser. Full operator lockout of application time, air pressure and vacuum pressure settings reportedly eliminates human variations. Compensates for syringe volume difference.

Nordson EFD

nordson.com/en/divisions/efd

FAST-CURING SILICONE COATING

UV Dual Cure 800-505 is a silicone coating with an initial UV cure of 3-5 sec., with secondary moisture cure for shadow areas. Rapid cure builds instant adhesion. Requires no work-in-process racking/staging and reportedly eliminates high-energy ovens. Is a sprayable, solvent-free coating. Dispenses by standard PCB spray coating equipment.

Novagard Solutions

novagard.com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PCB WEST 2020
Conference & Exhibition
Conference: September 8 - 11
Exhibition: Wednesday, September 9
See you in September!
PCBWEST.COM
SANTA CLARA CONVENTION CENTER, CA

In Case You Missed It

Adhesives

"Weak Bonds in a Biomimetic Adhesive Enhance Toughness and Performance"

Authors: Michael G. Mazzotta, Amelia A. Putnam, Michael A. North, and Jonathan J. Wilker.

Abstract: Developing high-performance adhesives is predicated upon achieving properties including strength and ductility. However, designing tough materials that are simultaneously strong and soft is usually contradictory in nature. Biological materials including shells and wood achieve impressive toughness by using weak bonds to connect larger structures at several length scales. Here, the authors show that this toughness design approach can be applied to synthetic adhesives. A biomimetic adhesive polymer, poly(catechol-acrylic acid), was examined in conjunction with several compounds containing two organic functional groups. In a typical example, the diol ethylene glycol decreased the overall system modulus. Performance was seen to increase significantly. Spectroscopic and physical methods indicated these bifunctional additives created an interpolymeric network of weak hydrogen bonds. Material toughness was enhanced when breakable bonds were available to dissipate mechanical stresses, while leaving the surrounding matrix intact. These discoveries illustrate how a biological materials strategy of interplay between strength and ductility can be achieved with sacrificial bonds in an adhesive. Such an approach may be a general principle applicable to designing higher performance electronics, transportation, and aerospace systems. (*Journal of the American Chemical Society*, February 2020; https://pubs.acs.org/doi/10.1021/jacs.9b13356)

Final Finishes

"Comparing the Reliability Performance of Electroless Palladium and Autocatalytic Gold in Production Environment"

Authors: Tom Scimeca, *et al*; tomscimeca@floridacirtech.com.

Abstract: The development of nanoscale surface finishes over copper pads such as electroless palladium and autocatalytic gold (EPAG) has been evolving in recent years due to increasing demands in terms of reliability, component miniaturization, and signal transmission. The authors conducted a full investigation of the production reliability of EPAG. As soldering and bonding are both possible with EPAG and of special interest in the microelectronics industry, the solder joint reliability and bonding results were evaluated. Increasing I/O counts have led to decreasing cross-sectional contact areas or, by default, an increase in solder performance expectations. The evaluation of this high solder joint reliability demand was satisfied by cold ball pull testing and high-speed shear testing. To examine EPAG's bonding abilities, the as-received (ASR) mode and aged condition at 150°C for 4 hr. were applied. Also, general storage reliability of the EPAG finish was simulated via aging for 100 to 1,000 hr. after bonding, assessing ENEPIG finish. In addition to soldering and bonding, the reliability of a final finish is also reflected in its wetting behavior and adhesion; therefore, solder indicator, dewetting and solder spread testing were performed. Reliability against external harsh conditions was tested via salt spray testing and compared to other common final finishes. (IPC Apex Expo, February 2020)

Materials

"Skin-Inspired Electronics"

Authors: Zhenan Bao, Ph.D.; http://baogroup.stanford.edu.

Abstract: New organic-based electronic materials permit an electronic system of fully integrated multifunctional components operating on the surface of or inside the body to enable smart healthcare for disease prevention and treatment and to enhance the functional capabilities of natural skin, and also serve as a module to connect our human body to the Internet, thereby allowing human integration with IoT. (Flex/MEMS & Sensors Technical Congress [MSTS], February 2020)

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.