Lee Ritchey: Minimizing Via Effects, p. 25

UP Media Group

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May 2020

PRINTED CIRCUIT DESIGN & FAB

CIRCUITS ASSEMBLY

CLEAN as can be

applying **IPC J-STD-001G** for **Material Changes**

- Multi-Board Design
- Quickturn Fabrication
- The Circuits Assembly Top 50 EMS Companies

Thin Lamination Board
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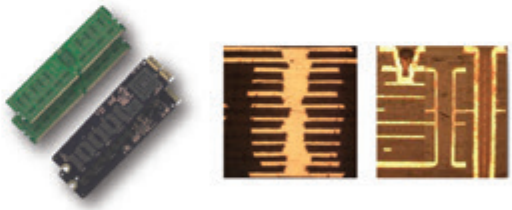
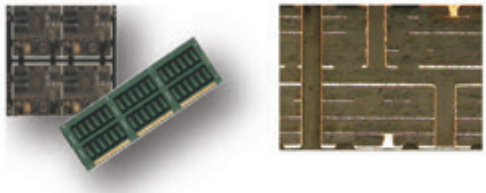
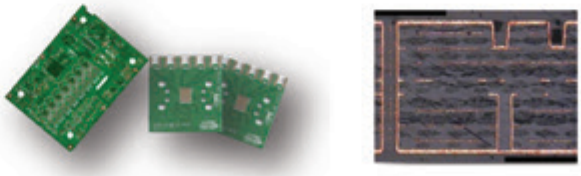
/ SSD Module



IOT / Build-up Board



Semiconductor TEST B'd
& 5G Network System



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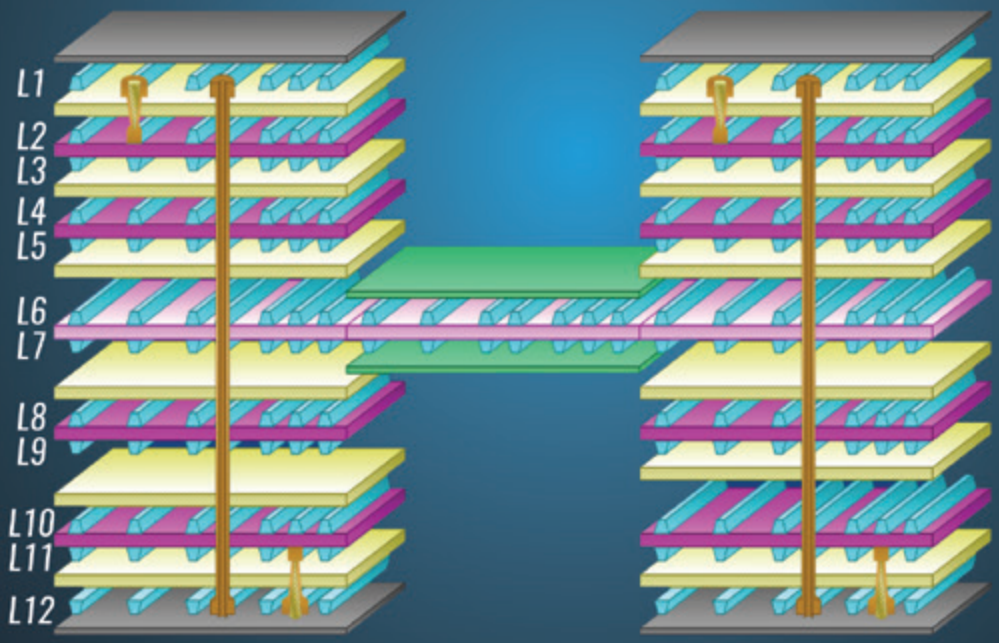

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MIKE BUETOW
EDITOR-IN-CHIEF

What Flexibility Really Buys Us

WE LEFT OFF last month commenting on the effects of Covid-19 on the supply chain and offering questions – and some opinions – on what might happen next. Interestingly, the real ugliness might not have hit yet. Anticipating the traditional supply drop-off during the Chinese New Year, most companies boosted inventories ahead of time. By the time China turned the lights back on, in late February/early March, the West was starting to slow, leaving stocks in a relatively decent position.

So far, so good.

Where China will feel it most, I think, is over the next two months, as Western demand lags and China's domestic-based suppliers pull back so as not to overstuff the supply chain. Already, we are starting to see some layoffs in Southeast Asia. If that region has to sustain another wave of Covid-19, look out. The chain could be in for a wild ride.

Count on a lot of energy spent over the next year or so looking back at the pandemic and how various business systems fared. Anticipate an abundance of white papers brimming with would-have/should-have/could-haves. Expect more than a few seers to pat themselves on the back for having predicted the disaster.

But the $1.5 trillion or so question is what are we going to do to (try to) prevent this from happening again?

Because it's not just a pandemic that can bring the supply chain to its knees in short order. An array of outages can stall even the largest of companies, and those stalls can trigger a chain-reaction of other problems. I'm old enough to remember when the electronics industry turned on the supply of epoxy cresol novolac resin – a key material used when etching line patterns into silicon wafers – and Sumitomo, which supplied more than 60% of the world market for ECN, was going to bail on manufacturing it because it couldn't make money. That wasn't a natural disaster or pandemic in the making, but it would have been equally disastrous to the supply chain. We have faced down flooding in Thailand, earthquakes in Taiwan and Japan, and typhoons in the Philippines. Any of a number of possible disruptions remain in play.

It's simplistic to say the manufacturing world will respond by becoming more digital, to ramp the so-called "Factory of the Future." We've been talking about lights-out manufacturing for more than two decades, yet it remains hypothetical, not practice. A handful of shops in the US – all assembly, not fabrication – purport to be digitally run, but inside the walls is plenty of human engagement with the process lines.

In the wake of the coronavirus, the consulting firm McKinsey has been churning out reports on leadership, rapid response, and team management. Yet a treatise authored in 2018 might hold most relevance for today's issues.

Unlocking Success in Digital Transformations looks at how and why so many operations fail when converting to computer-driven processes. (McKinsey pegs the longitudinal success rate at less than 30%, adding that only 16% of respondents say their organizations' digital transformations "have successfully improved performance and also equipped them to sustain changes in the long term.") Even so, when I speak to engineers and executives about what tomorrow's industry will look like, they most often settle on something to the effect of a "more digital enterprise."

Perhaps not coincidentally, McKinsey's advice for improving the chances of digital success heavily emphasize the human component: have the right digital-savvy leaders in place; build capabilities for the workforce of the future; empower people to work in new ways; communicate frequently via traditional and digital methods.

The issue to tackle, I think, is not whether to convert the human workforce to one run mainly by robots overseen by computer programs, but rather how the supply chain can become truly dynamic and responsive. Each factory must reach a level of heretofore unimagined flexibility. Manufacturers and suppliers must be able to adapt in real time to unfolding conditions. This isn't because we need to be able to respond to crises. Rather, this is because financial constraints ultimately will demand it.

Matt Kelly, IPC's new chief technologist, has extensive industry experience both at an EMS company (Celestica, six years) and an OEM (IBM, where he spent nearly 15 years in engineering and as a technology director). Kelly maintains the industry cannot truly perform technology transfer to the extent needed. Even the top EMS companies are only at half the peak capability when it comes to tech transfer, he says. And the reason, he asserts, "is not a lack of process replication or standardized equipment or training. People are the biggest issue."

It's unlikely we will see a day when a single factory can perform all the functions necessary to cost-efficiently produce a working PCB prototype, then scale that to program to volume. Imagine being able to move product rapidly, with no errors, from plant to plant and company to company, with the new factory able to run the job on the day received and at the requisite level of quality.

We reach that point, and no earthly disruption will stop us.

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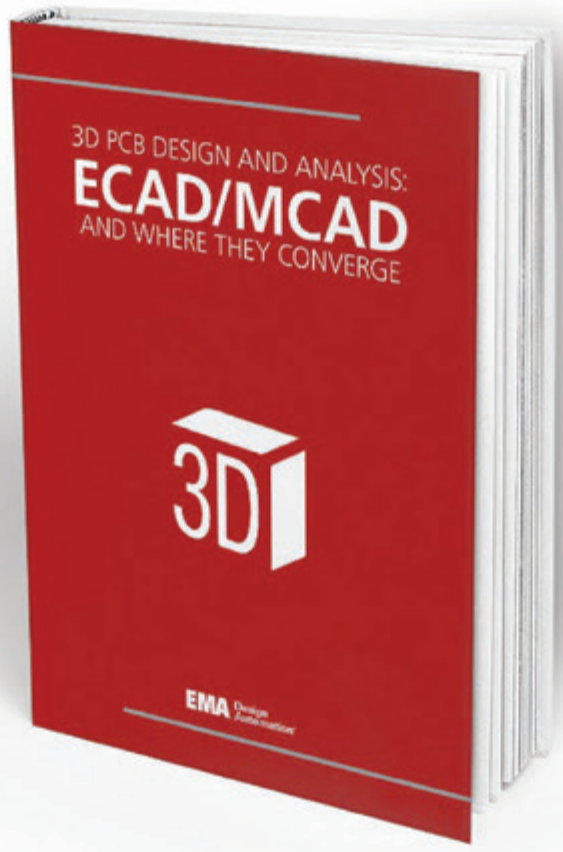

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PCDF People

AGC-Nelco Taconic named **Paul Cooke** technical sales manager. He has more than 20 years in PCB fabrication with Coretec, ITL, Siber Circuits, Dynamic & Proto Circuits, and most recently FTG, where he was director of field application engineering and technical sales.

Ansys promoted **Craig Hillman, Ph.D.,** to director of product management, new and emerging technologies. He was CEO of DfR Solutions for nearly 15 years, which he sold to Ansys in 2019.

Elmatica named **Adam Szostek** country manager in Poland, **Maria Ricart Bou** technical manager, and **Maryam El Bakkali** to customer service.

Vitesco Technologies named **Stefana Buraga** hardware PCB designer. She has a degree in electronics, telecommunications and IT from Gheorghe Asachi Technical University of Iași.

PCDF Briefs

APCT Anaheim is now capable of quick-turn production for rigid-flex product.

The **International Bromine Council (BSEF)** has filed a legal challenge against the European Commission's ban on the use of halogenated flame retardants (HFRs) in electronic displays under the EU Ecodesign Directive.

Intel and **Cornell University** researchers have developed an "electronic nose" system that can detect 10 different chemicals as accurately as a state-of-the art deep learning system, but with very little training required.

HSIO Technologies and **Flexible Circuit Technologies** announced a comprehensive technology agreement to produce flexible and rigid-flex circuits.

Keysight Technologies has validated an innovative new software approach, leveraging AI and advanced data analytics, in **Nokia's** 5G base station manufacturing processes, significantly improving test efficiency.

Schmid signed **Hakuto** to distribute its wet processing equipment in Japan.

Ventec's European headquarters has successfully recertified to AS9100D.

Deep Impact: Could All Electronics Benefit from Vibration Tests?

PITTSBURGH, PA – Electronics of all kinds are exposed to dramatic shock and vibration events in the field, and as such factory testing should be expanded beyond cellphones and other handhelds.

That's according to Ansys, which asserts even larger desktop and bench units such as monitors and servers can benefit from impact testing.

"The goal of these tests is to design server packaging and housings that can withstand the impacts, jostles and shakes of its environment. For instance, a server could drop, experience an earthquake or bounce around inside a shipping truck," Ansys says.

But while such testing gets expensive quickly, the EDA company says alternate methods available today are simply dumping live product to the floor. IBM, for instance, is using software to virtually perform drop tests.

Using specialized tools, engineers can set up parametric studies and use bidirectional CAD connectivity to assess how changing the geometry affects the impact performance of various designs, Ansys says.

The effort, the company suggests, could bring new meaning to "PC crash," and ultimately save consumers money and frustration. (MB)

UP Media Announces Technical Sessions for PCB West

ATLANTA, GA – UP Media Group announced more than 45 technical sessions have been selected for PCB West 2020 this fall. Overall, more than 80 abstracts were submitted for the annual conference, which takes place Sept. 8-11 at the Santa Clara, CA, Convention Center.

This year's conference features a pair of extended talks from Lee Ritchey on power delivery system design and stackup design, plus three full days of classes from Rick Hartley. The conference covers everything from RF/microwave and mixed-signal design, circuit grounding, understanding material choices, flex circuits, signal and power integrity, to fabrication and assembly processes. Talks are aimed at the spectrum of backgrounds, from novice to advanced.

"When it comes to the technical conference, we were clearly more selective than ever this year," said Mike Buetow, PCB West conference director and editorial director, UPMG. "Engineers and designers have limited knowledge of proper grounding, and we are emphasizing that, plus power distribution, to help overcome noise problems associated with power bus design."

"For those interested in new component technology, we will have talks on designing and assembling heterogeneous packages, high-density chip-scale and 3-D packages, and more," Buetow added.

In response to attendee feedback, the technical conference begins each day at 10 a.m. Attendees will also receive certificates indicating the number of hours of training received at PCB West.

On Sept. 9, PCB West will feature 10 free presentations covering the design to assembly spectrum. Highlights include talks on electromagnetic fields, high-speed digital circuits, AI-based smart routers, land pattern design, and thermal management from companies such as Intel, NXP and Analog Devices.

All free talks will take place on "Free Wednesday," to complement the one-day exhibition that features more than 100 leading companies.

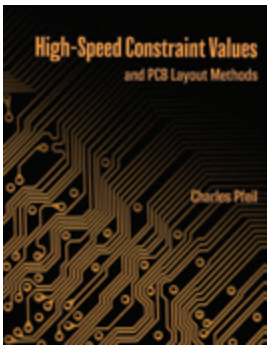
The free keynote address will feature Dr. Brian Toleno, director of new technology at Microsoft, who will speak on Augmented Reality New Device Challenges and

Enabling Industry 4.0. The keynote takes place at 11 a.m. on Sept. 11.

PCB West annually provides a conference and exhibition focused on the design and manufacture of PCBs, HDI, electronics assembly and circuit board test. The event annually attracts nearly 2,000 attendees. The event includes a four-day technical conference and one-day exhibition to be held at the Santa Clara (CA) Convention Center.

Visit pcbwest.com for details. (MB)

Charles Pfeil Publishes 'High-Speed Constraint Values' E-Book



ATLANTA, GA – UP Media Group announced publication of a new e-book by Charles Pfeil titled *High-Speed Constraint Values and PCB Layout Methods*. The free download, available from UPMG, includes the Constraint Value Calculator, an Excel-based worksheet developed by Pfeil.

High-Speed Constraint Values and PCB Layout Methods encompasses lessons learned from Pfeil's five decades in PCB design. It covers critical length, reference planes, timing, skew, crosstalk, coupling, vias, and routing. The book provides the underlying equations and specializes in practical solutions for real-life signal problems.

The Constraint Value Calculator that comes with the e-book provides rules with appropriate constraint values for high-speed designs. It includes options for edge rate, dielectric constant, and height between the layers to determine constraint values.

In the forward for the new e-book, leading high-speed expert Rick Hartley writes, "This fabulous treatise allows PCB designers and engineers to understand all the important constraints and determine their values in a fast and precise manner using the accompanying calculator. The calculator is marvelously designed and simple to use."

Both *High-Speed Constraint Values and PCB Layout Methods* and the Constraint Value Calculator are available for free via the PCD&F website at https://pcdandf.com/pcdesign/index.php/constraints.

Pfeil has spent over 50 years in the PCB industry as a designer, owner of a service bureau, and in engineering management and product definition roles at Racal-Redac, ASI, Cadence, PADS, VeriBest, Mentor Graphics, and Altium.

Most of his career was at Mentor Graphics, where he was a software architect focused on advanced development of PCB design tools. He was the original product architect of Expedition PCB, and an inventor of Team PCB, XtremePCB, XtremeAR, and the Sketch Router. He previously authored BGA Breakouts and Routing. (MB)

US EPA Eases Up on TSCA Fees

BANNOCKBURN, IL – The US EPA said it is exploring exemptions to the Toxic Substances Control Act (TSCA) Fees Rule, says IPC.

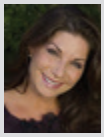
The TSCA Fees Rule is designed to collect revenues to pay for risk evaluations of toxic substances. However, the EPA now says it will consider exemptions for manufacturers that import articles containing high-priority substances or produce such substances as byproducts or impurities.

This regulatory relief has the potential to reduce long-term administrative and financial burdens for those three categories of manufacturers. If the change is approved, manufacturers who fall into these categories would no longer be required to self-identify under the TSCA Fees Rule.

In addition, the US EPA is providing a no-action assurance to these manufacturers with respect to the self-identification requirements. This means the EPA will exercise its discretion to not pursue enforcement action against such companies for violations of the self-identification reporting obligations. (CD)

CA People

AIM Solder appointed **Daniel Gil** sales manager for the Tijuana and Baja regions of Mexico.



AQS named **Brenda Martin** director of business development. She was director of business development at Zollner for three years, and has held related roles for Sanmina, Jabil and SMTC.

ECD announced **Mike Hayward** as director of EMEA operations. Hayward, who previously held a similar role with ECD, has worked in the electronics industry for over 35 years and has an engineering technology national diploma from Gwent College.

Insituware appointed **Denis Barbini, Ph.D.,** chief scientist. He has 20 years of industry experience with Vitronics-Soltec, Universal AREA Consortium and Crucial Machines, and a doctorate in chemistry, material science from SUNY Binghamton.

Indium named **Alexa Blasi** global logistics manager and **Huaguang Wang** research metallurgist.

IPC named **Ray Cirimele** senior instructional systems designer.

Steve Stiller, owner of Midwest Production Specialists, has passed away.

Zestron named **Jeff Kennedy** strategy and business development manager. He has more than 30 years of engineering and management experience in system integration, process development, PWB fabrication, packaging in the microelectronics industry, and over 20 years in contract electronics assembly, most recently with Celestica.

CA Briefs

Absolute EMS installed a **MIRTEC** MV-6 Omni 3-D AOI and an MS-11e 3-D SPI.

AIM Solder named **Masline Electronics** distributor in Northern New York.

Bosch has selected **MIRTEC's** 3-D AOI.

A cluster of HDD supply chain makers has been formed in Thailand with **CalComp Electronics & Communications** and **Quanta Storage** also participating, allowing them to circumvent impacts of the coronavirus outbreak.

Carestream's Non-Destructive Testing organization announced its partnership with **Creative Electron** for the NDT product portfolio.

CheckSum was selected to supply PCBA test equipment by a major automotive supplier of electronic systems located in Southern China.

Critical Manufacturing appointed **SMarTsol Technologies** representative in Mexico.

CyberOptics has received orders worth $2.8 million for its 2-D MX600 inspection system and a $1.2 million order for its SQ3000 Multi-Function AOI/SPI/CMM systems.

Enics is moving its electronics manufacturing and assembly services from Raahe, Finland, to other manufacturing sites.

ITW EAE named **Testerion** representative of all ITW EAE equipment in South Africa. ITW EAE also extended its partnership with **Metronelec** and **W-Tech France** to represent and distribute **Vitronics Soltec** soldering equipment.

The India Electronics & Semiconductor Association recommends setting up a National Electronics Commission to bring all electronics- and semiconductor-related activities under a single umbrella.

Jabil installed a cloud-based manufacturing app platform to provide operators with step-by-step instructions for each assembly application.

Javad EMS installed a **Hakko** HU-200 robotic soldering system.

Kyocera completed its previously announced acquisition of **AVX,** following the completion of Kyocera's tender offer to purchase all outstanding shares of AVX common stock that it did not already own.

Mesago Messe announced the SMTconnect trade show in Nuremberg, Germany, has been postponed to Jul. 28-30, 2020.

Niche Electronics named **FabSource** sales representative in the Southeastern US.

Robotas Technologies named **Island SMT** representative in Mexico.

SMTC has completed the closure of its manufacturing operations in Dongguan, China.

Sunburst EMS has been acquired by an internal management team led by Steve Haley and George Agyare.

Viscom named **PCB Technologies** sales representative in Italy.

Vision Engineering opened a 2,700 sq. ft. technology collaboration and training facility in Irvine, CA.

IPC Releases Automotive Soldering Addendum

BANNOCKBURN, IL – IPC has released new requirements for automotive printed circuit boards to its soldering and assembly qualification standards.

IPC J-STD-001GA/IPC-A-610GA, Automotive Addendum to IPC J-STD-001G, *Requirements for Soldered Electrical and Electronic Assemblies* and *IPC-A-610G, Acceptability of Electronic Assemblies*, is attached to both standards as it looks at board reliability requirements for the automotive industry, from assembly to inspection.

Committee members representing 17 countries worked for more than 30 months on the addendum to address criteria and acceptability requirements for PCB assemblies for the automotive industry not covered in IPC-A610G and IPC J-STD-001G. The committee was guided by the principle of providing criteria to be used in addition to, and in some cases, in place of, those in the base documents to ensure the reliability of soldered electrical and electronic assemblies that must survive the automotive environment. (CD)

Zentech Acquires CAMtek

BALTIMORE, MD – Zentech Manufacturing acquired Bloomington, IL-based EMS firm CAMtek for an undisclosed sum. Following the transaction, CAMtek will become Zentech Bloomington (IL) and joins Zentech Baltimore (MD), Zentech Fredericksburg (VA) and Zentech Dallas (TX), which Zentech acquired in January.

Christine Davis, founder of CAMtek, will continue to manage Zentech Bloomington.

CAMtek is AS9100D certified and features four SMT lines and more than 100,000 sq. ft. of manufacturing space. The company focuses on the military, industrial and commercial markets.

"CAMtek is an outstanding company with strong leadership, and we are very pleased to welcome them to Zentech," said CEO Steve Pudles. "From certifications to engineering talent, and from capabilities to technology commitment, CAMtek very closely mirrors our core values and will be a true asset to the Zentech brand as we continue our strategic build-out and market leadership across key geographies in the US high-reliability electronics contract manufacturing industry." (CD)

Lacroix to Open 'Smart Factory' in France

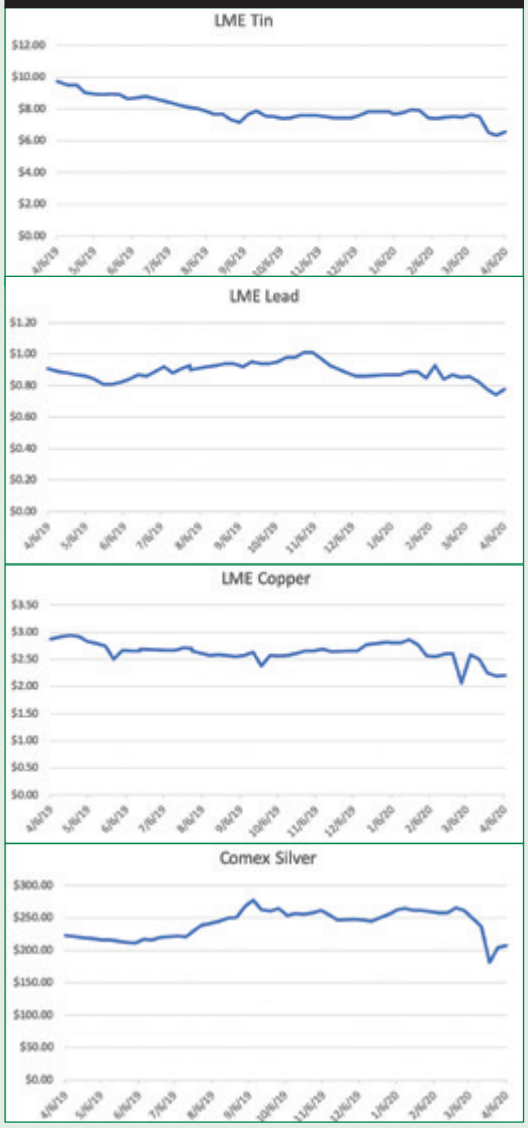
BEAUPREAU-EN-MAUGES, FRANCE – Lacroix Group is part of a group investing €25 million (US$26.7 million) to establish a 16,000 sq. m. (172,000 sq. ft) smart factory here. The new plant will feature six production lines, including one exclusively dedicated to large automated production runs, and is expected to be fully operational by the end of 2021.

The EMS provider is opening the plant with help from the SPI fund, administered by Bpifrance. It said it would increase its competitiveness in traditional electronics system markets but also develop its presence in new growth markets, particularly in industrial IoT and large automated production runs.

"I am extremely pleased and grateful for Bpifrance's support, through the SPI fund, for our 4.0 electronics factory project," said Vincent Bedouin, CEO of Lacroix. "We have conceived this project as the standard-bearer of industrial renewal in the French electronics assembly sector. With this entirely digitized factory, integrating the most advanced technological standards, we are equipping ourselves with a powerful industrial tool, capable of meeting the challenges of an electronics market that is complex, competitive, international, and rapidly changing."

"We are very happy to support the deployment of a 4.0 production site in Maine-et-Loire with Lacroix Group," said Eric Lecomte, senior investment director, Bpifrance. "This investment will make it possible to meet the strong growth in activity, and to maintain our skills and know-how in complex electronic equipment with a strong technological component." (CD)

METALS INDEX



KEY COMPONENTS

	OCT.	NOV.	DEC.	JAN.	FEB.
Semiconductor equipment billings[1]	2.5%	9.1%	17.8%	22.7%[r]	26.2%[p]
Semiconductors[2]	-12.7%	-10.7%	-5.4%	-0.35%[r]	5%[p]
PCBs[3] (North America)	1.11	1.08	1.09	1.05	1.15
Computers/electronic products[4]	5.49	5.50	5.47	5.45[r]	5.49[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

Top 50 EMS Company Revenues Flat in 2019

NEVADA CITY, CA – In 2019, the top 50 global electronics manufacturers had $344 billion in revenue combined, up 0.4% year-over-year, according to Manufacturing Market Insider, a division of New Venture Research.

Overall, the APAC region accounted for around 90.2% of the Top 50 EMS revenue, the Americas 7.4% and EMEA 2.3%. In contrast, during the 1990s the Americas accounted for more than 50% of all production, with EMEA assembling an estimated 30% and APAC serving around 20% of total production.

NOTHING TO SEE HERE

US electronics equipment shipments	% CHANGE DEC.	JAN.	FEB.	YTD%
Computers and electronics products	-0.1	-0.1	0.3	1.5
Computers	0.2	3.8	0.7	-13.0
Storage devices	-17.0	9.0	-2.3	37.2
Other peripheral equipment	-5.3	2.8	-1.8	8.3
Nondefense communications equipment	2.9	-1.4	-0.2	4.8
Defense communications equipment	27.1	-17.2	3.8	-9.9
A/V equipment	3.5	-10.0	-2.5	-28.2
Components[1]	0.8	1.7	-0.2	10.7
Nondefense search and navigation equipment	0.3	0.5	-4.5	-4.0
Defense search and navigation equipment	-2.0	-0.5	0.1	4.8
Medical, measurement and control	-0.2	0.9	-1.4	-2.9

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, Apr. 2, 2020

US MANUFACTURING INDICES

	NOV.	DEC.	JAN.	FEB.	MAR.
PMI	48.1	47.8	50.9	50.1	49.1
New orders	47.2	47.6	52.0	49.8	42.2
Production	49.1	44.8	54.3	50.3	47.7
Inventories	45.5	49.2	48.8	46.5	46.9
Customer inventories	45.0	41.1	43.8	41.8	43.4
Backlogs	43.0	43.3	45.7	50.3	45.9

Source: Institute for Supply Management, Apr. 1, 2020

Hot Takes

- Fourth quarter revenue at German region PCB fabricators fell 11.8% year-over-year, and orders dropped 7%. Sales for the year fell 11.1%, and orders were down 11.4%. (ZVEI)
- Worldwide IT spending is now expected to decline 2.7% in constant currency terms this year due to Covid-19. (IDC)
- IT infrastructure equipment sales rose 3.3% to $38.1 billion in the fourth quarter but fell 1.1% to $134.4 billion for the year. Non-cloud IT infrastructure fell 4.6% to $18.7 billion for the quarter and declined 4.1% to $67.7 billion for the year. (IDC)
- Fourth quarter combined DRAM and NAND revenue was $27.5 billion, down 23.4% year-over-year and up 2.5% sequentially. Blended NAND pricing will increase in the first quarter and likely again in the second, given current pricing momentum, normalized inventory levels, and limited production growth, offsetting lower seasonal demand growth and initial impacts from the coronavirus. (Yole Developpement)
- Spending on PCs, tablets, mobile phones, and peripherals is expected to decline 8.8% this year. (IDC)
- Global copper production in 2020 is expected to fall 1.9%, down from a previous outlook of 3.4% growth, due to Covid-19 impacts. (GlobalData)
- Server market revenue increased 5.1% in the fourth quarter, and shipments grew 11.7% year-over-year. In 2019, worldwide server shipments declined 3.1%, and server revenue declined 2.5% compared to 2018. (Gartner)

We Can Learn from Covid-19. Will the Lessons Take Hold?

Motivated by fear, businesses are valuing creativity as never before.

OVER THE PAST 60 to 90 days, I am sure I have heard the term "the new normal" at least a thousand times. Before Covid-19 has run its terrible course, I fully expect to hear it at least a zillion more. But what exactly is "the new normal?"

Sometimes global events become a catalyst for change. Events like the Great Depression and World War II had dramatic, difficult and often devastating impacts on the world. However, those impacts were mostly temporary reactions to transient events, like the aftermath of a very bad storm. Covid-19 is different, which makes trying to visualize and comprehend events, both in the now and the future, so difficult.

Covid-19 truly levels the playing field. Everyone on earth will at some point be impacted, regardless of gender, political orientation, geography, socio-economic status or faith. Everyone is at risk, and everyone will be impacted in similar ways. That differs from past global events that typically were the cause of regional wars (even WWII did not impact *all* countries), economic downturns, political eruptions, or local plagues. We really are all in this together.

Short-term, we know some definitions of the new normal include social distancing; self-quarantine; wearing gloves, face masks and other safety devices to reduce the possibility of exposure; plus the social changes caused by stay-at-home dictates that impact how we work, study and interact. This new normal will in time prove to be the relatively short-term definition.

But a year or five from now, will these changes be permanent, or will everyone revert to behavior as usual?

That is the intriguing aspect of our current Covid-19 lifestyle. People everywhere are discovering and embracing new and old technologies. Peers in non-manufacturing industries tell me they are rethinking their office environments and leaning toward making some aspect of work-from-home part of their future "normal." They are finding many tasks and activities can be done successfully and more efficiently from home, even with children, spouses, and pets underfoot. The technology is there, with identifiable benefits.

Some of my manufacturing neighbors in different industries are sorting through the tasks they can have employees do from home to support the stay-at-home requirements but still stay in operation. Simple tasks like packing product into boxes and basic inspection can often be handled as cottage trades, with kits supplied to an employee to work on at home. And a number of people I have spoken with are aggressively trying to run some automated equipment remotely, so once or twice a day someone can load and unload a work center, then operate it "lights out" from a remote location. Driven by fear, businesses are casting risk aside and valuing creativity as never before.

In our own industry, people are working on ways to keep going with fewer people per work center, shift or location to support social distancing and remain in production of needed product. Some workarounds may appear like something out of Rube Goldberg's playbook, while others may be schemes that work so well they will eventually become standard operating procedure. The fear of "what if something goes wrong while operating remotely" is being overcome by the reality of "what if we can't get product out the door." I am sure robotics combined with machinery that can be operated remotely will become more typical faster than anyone might have thought a few short months ago.

Meanwhile, on the home front, reports say many families have turned off the TV and computer to get away from the barrage of scary and depressing Covid-19 news and are rediscovering traditional social activities such as board games, jigsaw puzzles and card games. Might these very non-tech activities once again become part of the normal fabric of society?

Which brings me back to visualizing what, exactly, "the new normal" will look like. If, as in the past, this is relatively short-lived, as in a matter of months, likely the new normal will appear remarkably similar to the "old" normal. Either way, I fully expect many will conduct a deep-dive post-mortem on what happened and what we learned from the experience. I expect the findings will range from the basics – such as the need to be more careful with personal hygiene – to the comprehensive – opportunities for improvement in the home and workplace. Concepts that may have sounded good but did not work well when put to the test will fall by the wayside. Others that proved to work far better than first imagined will be analyzed to be harnessed, expanded and integrated further into work and home life.

Automation and communication will be winners. Tools such as Zoom and Skype will be better harnessed to enable remote interactivity, and working remotely may become normal. A refocus on the opportunities and best practices of lights-out technology, possibly with further integration of some robotics, will no longer be viewed as futuristic. The work-life balancing act may tip toward time spent at home.

Most significantly, it appears "the new normal" may have less to do with how we reacted to Covid-19, but rather how we came to learn to overcome our natural aversion to risk and embrace the new. □

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Is It Time for a Pandemic-Resistant Supply Chain?

Or will the West continue to risk exposure?

THE MASSIVE DISRUPTION caused by Covid-19 has revealed the fragility of the global supply chain. With proper leadership, however, many companies are adjusting (or will adjust) to the changes made necessary by this pandemic.

Predictably, this unprecedented disruption has prompted calls for nations to onshore their manufacturing. It's an argument that pops up periodically. And on the surface, it does make sense. Why leave a domestic market so vulnerable to what's going on in the rest of the world? Why not build all we need here?

But here's some straight talk: It is simply not realistic to think we can bring all manufacturing – including printed circuit boards – back to Western shores.

Would our companies – or our local, state and federal governments – be willing and able to invest the staggering amounts of money needed in the necessary technology? Would they also be able to help supply the skilled labor force required?

Crucially, would Western consumers be willing to pay the significantly higher prices necessary to make everything in their local markets?

I just don't see that happening.

The American PCB industry, for one, simply would not be price-competitive. Besides, during this global pandemic, domestic manufacturing lead times have been pushed out even more than those offshore, worsening the situation.

The truth is, while the coronavirus began in China, manufacturing there is already starting to get back on its feet. And it will be back to capacity faster than the rest of the world. That's because the Chinese have invested heavily in automation for years, and they already have a specifically trained (and less expensive) labor force.

The coronavirus has exposed the weak link in our global system of trade, affecting with stunning speed the entire world's ability to produce goods and services. It has literally leveled to the ground the entire global supply chain. Production, while not halted, has been seriously slowed, both for goods produced offshore *and* those manufactured domestically.

And the hard truth is, even after we get through the current situation, there will almost certainly be another. That begs the question: What steps will your company take to become "pandemic resistant?"

I can see many changes ahead to deal with this invisible and deadly enemy becoming part of a "new normal" in PCB manufacturing. These changes could include:

- Non-manufacturing personnel in sales, marketing, finance, and administration continuing to work remotely.
- More outsourcing of tasks previously handled in-house, further reducing overhead expenses.
- Manufacturing personnel continuing to work at least six feet apart, with facilities being rearranged to accommodate that distance.
- Plants redesigned to have fewer doors and surfaces that require employees to touch them, and changes made in ventilation systems to ensure air is circulated safely.
- Personal protective equipment (PPE) required for the onsite workforce to wear all the time. Or, at a minimum, a sufficient supply of protective items on hand.
- Employees no longer having full run of a facility. Their movements might be limited to only those areas required to perform their job function.
- Higher health care and business insurance premiums, dependent on onsite employee numbers or factory layout.

Not far from where I live, one of the largest EMS companies in the world is building a sprawling new headquarters. With fewer employees potentially required to gather in one location, do companies really need to spend all that money for an extravagant building? Who will be occupying those offices and conference rooms – and using all those nice amenities – during the next pandemic?

Would factory visits by customers or salespeople be curtailed or controlled, with a doctor's note required or visitors' temperatures being taken prior to entry to a facility? Will the receptionist be seated behind glass, not as a protection against armed entry but lethal droplets?

What about the need for international travel? In the PCB world, large OEM and EMS companies spend hundreds of thousands of dollars a year to send key employees overseas to inspect PCB manufacturing facilities. These trips may help with building business relationships and ensuring quality of product. However, do corporations continue to risk the health of their employees while they travel? And what about what they might bring back to their offices?

More firms may consider hiring offshore supply chain management firms, which are on the ground near the PCB manufacturers and can watch over

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What to Bring to the PCB Design Review

Design reviews can easily go off on tangents. Make sure you're the one sharing your screen.

EVERY JOB EVENTUALLY gets to tape-out day. But before that day comes, a lot of moving parts are wrangled into place. Even the simplest layout will require deliverables for assembly, including custom paste stencil and a bill of materials to associate the correct component for each location on the board. Along the way, a set of physical and electrical properties will be used to gauge line width and length, among other parameters (**FIGURE 1**). Getting the responsible parties to give guidance on the many assumptions made during layout is the point of the design review.

Placement spacing and orientation. Two types of assembly data are used in the factory: the kind we can see or touch and the kind that has meaning only to the machines. Robotic assembly is programmed from an x-y coordinate file. An assembly drawing provides a visual representation, including reference designators, component outlines and, important, the orientation with a pin-one mark. A hard copy of the assembly drawing is an item for the review.

If you're lucky and well-supported by physical design (MCAD), you might also see an outline drawing for the PCB and perhaps an interface control drawing (ICD) that presents all the electrical details pertaining to any connectors to the outside world. You don't usually expect these types of drawings until everything is said and done, and then only because the customer requested them. Every MCAD to ECAD flow has the potential for missed requirements. To close this loop, invite the physical design engineer to the review.

Routing tricks, workarounds, and neck-downs. Rules were made to be bent, folded, spindled and mutilated to complete the job in the real world. In this case, the real world is a virtual representation of a PCB that does not yet exist, but the point is we can't always meet every spacing and line width requirement. Zones set up to facilitate fine-pitch connectors or BGA packages permit rules to be relaxed.

FIGURE 1. The design review is a necessary part of the product development process. (Source: Business Matters)

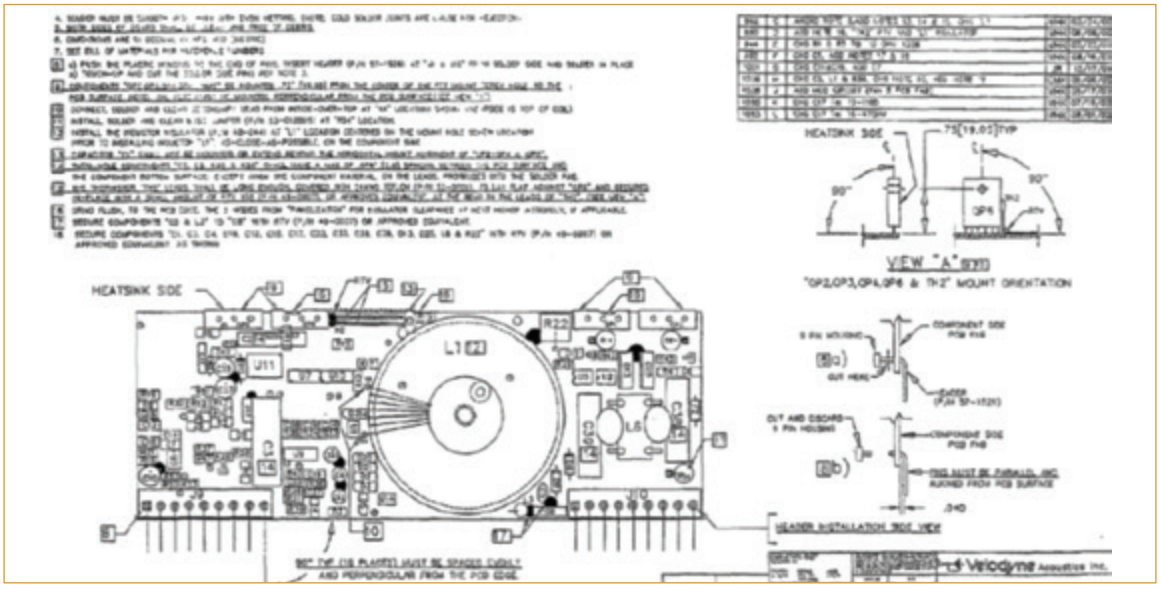

FIGURE 2. Hard copies of the CAD design reveal obvious errors. (Source: Velodyne Lidar)

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist, but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

Tradeoffs must be carefully managed. Signal integrity and power integrity (SI/PI) are battling for space. It's a tug of war for an airgap around the clock or metal for the VCC. Let the border wars begin. When everyone is equally uneasy, it's time to ship. Every major link in the design has a champion. Bring all of them together at least once, especially when the pickings are slim.

The document package. Of course, there will be a screen to show off the layout details. As you go through the highlights, comments can be captured in "red ink" on the printed docs. Speaking for myself, the act of turning on each layer of the design and plotting it out has revealed at least as many mistakes as the design reviews. Fix and replot.

The CAD screen can show details as you pan around. The hard copy makes errors like that one upside-down reference designator stand out in black and white (**FIGURE 2**). The plots are most useful for the folks who show up for the review on time. They can dig into any part of it that is of interest while you set up the A/V equipment. They're interested in something, or they wouldn't be there.

Down rev artwork for comparison. We can always count on some nostalgia for the old revision, if the design under consideration is based on an existing rev. Reasons for not wanting change if it isn't broken are valid, especially for analog, where there is an element of FCC regulatory requirements. Having to go through certification again works against the time-to-market drive.

The same holds for a hairy DDR maze or the power tree for a mobile computing device. Setting up slides where, for instance, you have the old work in blue, the new in red and the common elements in the overlapping purple helps people visualize the upgrades to each layer. If it becomes a Jackson Pollock sort of image, then they know you've been busy (**FIGURE 3**).

List of major upgrades, design rules and exceptions. The schematic is normally the warm-up act for the actual layout. This is more to share the interesting parts than to hash out schematic requirements. That was (or should have been) given its own review slot. One famous company I worked at had the EE locked in for five hours while people came and went reviewing their sections.

Still, co-development doesn't halt just because your 11th hour is nigh. The motto seems to be if it weren't for the 11th hour, nothing would get done. Design reviews can easily go off on a tangent, so make sure you're the one sharing your screen for the most part. The spotlight is on placement and routing, as far as we're concerned. A chip-by-chip approach is often more useful than a layer-by-layer presentation.

A slide deck is useful to an extent, since you can capture screenshots and add captions for everyone to "take home." It allows us to pace the review and ensure we at least acknowledged the data. Spelling out the risks makes them shared risks. When it breaks down is when questions come up. That will bring the board file back to the screen while you take measurements. I like slide shows as teaching aids, plus they are more portable than the PCB database.

FIGURE 3. Showing revisions and common elements in different colors helps with visualization. (Source: 1st Dibbs)

Beyond hard and soft copies of everything, a willingness to accept new information is key to surviving a design review. Action items are expected. "OK2FAB" is phrased as a question. Asking that question leads to answers. Until the situation becomes "OK," keep closing loops and closing deals and on 2 FAB! □

Better Board, continued from pg. 13

their orders 24/7, without exposing any employees to health hazards.

After considering the changes that may be coming to our industry in response to Covid-19, I had an idea about a new component within ISO: a registry of certified, pandemic-resistant facilities.

How long will it be before we hear supply-chain managers asking, "Does your manufacturing operation have CDC or WHO approval?" It's an idea that most of us would have dismissed just a few months ago. But I'll bet it's coming.

So, what are you doing to make your supply chain or company resistant to a pandemic? □

Onward!

An update on the PCEA direction, plus highlights of the Silicon Valley chapter.

IN MY DEBUT as author of this column, I provide updates on the direction and leadership of the PCEA, and Stephen Chavez shares his first "message from the chairman." In addition, Bob McCreight, president of the Silicon Valley chapter, discusses their "lunch and learn" event held in February. Last, we share our updated list of professional development and event opportunities, although some may be affected by the Covid-19 outbreak. Stay tuned for more updates.

PCEA Updates

Over the past few months, our writer for *The Digital Route,* Stephen Chavez, was unanimously elected chairman by our newly formed executive board at the PCEA. Steph graciously accepted, and the PCEA is delighted to be part of a vibrant, highly skilled team of PCB industry folks now led by an experienced, young and newly minted chairman. Steph has demonstrated a zeal for helping the electronics industry and is surely capable of leading us successfully into the next decade (**FIGURE 1**).

Steph has mentioned his main objective in writing was to promote continued globalization of knowledge-sharing for all involved in the design, fabrication, assembly, and test of printed circuit boards. *The Digital Route* has been Steph's labor of love for the electronics industry. He has put in many hours of his own time to lay the foundation, solicit interesting content, and craft this column into a must-read for people who want to engage.

All of us in the PCEA thank Steph Chavez for setting this high standard for this column and for inspiring excellence in all of us as we move forward. In closing out his column last month, Steph mentioned a process of evolving from a writer to a leader. As chairman, he has already proven himself a leader by becoming an effective delegator. Within a short time, the PCEA team was led to move quickly to nominate and elect a replacement communication officer so that this column would not miss a beat.

Well, here I am, and I want to thank Steph for his kind words and for the confidence shown by the executive team in nominating and electing me as PCEA's communications officer. I won't take this service lightly, and I will do my best each month to bring coverage of this unique association of professionals who are on fire for promoting collaboration, inspiration, and education within the PCB engineering industry.

Okay, let's try this out. Tap, tap … Is this mic on?

Who Serves the PCEA?

Over the past several months, a group of active people in the PCB design and electronics industries transitioned to form the PCEA. To move forward the preliminary ideal and goals the group set for the long-term, important organizational roles needed to be created and filled immediately. Leveraging time together while meeting at several industry trade shows and employing online meeting apps, the group was eager to begin nominations and elections to fill critical roles (**FIGURES 2** and **3**).

I am very proud to announce our progress in electing the first servant leaders to the PCEA executive board.

- Chairman – Stephen Chavez
- Vice chair – Mike Creeden
- Chairman emeritus – Gary Ferrari
- Administration – Cherie Litson
- Treasurer – Mike Creeden
- Communications – Kelly Dack, Stephen Chavez
- Media & Social Media – Judy Warner, Tara Dunn
- Sponsorship / endorsement – Mike Creeden
- Education – Susy Webb, Gary Ferrari, Rick Hartley
- Chapter liaisons – Scott McCurdy, Terri Kleekamp

KELLY DACK, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). Read past columns or contact Dack; kelly.dack.pcea@gmail.com.

FIGURE 1. Mike Creeden, Stephen Chavez and Cherie Litson.

FIGURE 2. Mike Creeden, Stephen Chavez, Randy Kumagai, Cherie Litson, Judy Warner, and Gary Ferrari.

These are exciting times for the PCEA. New ideas for the organization are being identified at just about every meeting. In the months that follow, I will provide coverage of the activities of the executive staff and their duties serving the PCEA, and work with Stephen Chavez to feature expanding chapters and report on how they will represent and grow the benefits and values of the PCEA in their own local areas and beyond.

Message from the Chairman

Stephen Chavez, MIT, CID+, PCEA Chairman

As chairman of PCEA, let me start this first-ever "Message from the Chairman" by saying it is an honor and privilege to be selected to lead such a large global group of talented, passionate, and veteran industry leaders. As we move forward and establish a path for PCEA, collaboration, inspiration and education are at the core of what the organization is all about.

Looking back at my career, when I made the decision (more like a huge nudge from one of my early mentors) to get involved and become an industry contributor, it made such an enormous positive difference in my career and within my personal life as well! Not only have I had continued success as a printed circuit engineer, but I have had the great fortune to meet many great industry colleagues who have become dear friends over time. I was lucky enough to get guidance back then, but only after lots and lots of struggling on my own.

As the newly elected chairman of PCEA, serving our global chapters and members, collaboration, inspiration and education are truly at the core of my passion as well. I intend to give my all to make a positive difference in our ever-evolving industry and to help others succeed in their profession, like those who have helped me along the way.

I highly encourage you all to get involved! Join the PCEA by visiting our website (www.pce-a.org) and registering as a member to become part of the PCEA collective. You can always reach out to me (stephen.chavez.pcea@gmail.com) or Kelly Dack (kelly.dack.pcea@gmail.com) to get more information as well.

Our evolution as a professional association within the industry is progressing as planned. We continue to solidify the foundation of PCEA now that the executive board leadership has been voted on and is in place. Our website is a work in progress, with a new and improved version coming this spring. Our incorporation status of 501(c)(6) nonprofit is coming together as planned. We should be getting our employer identification number (EIN) within a few weeks.

Things are moving quickly and coming together nicely due to the outstanding efforts, positive attitude, and passion each of the PCEA executive board members brings to the table. This is truly the right group of industry leaders to take on such a task and make it successful! I feel very humbled and blessed to be a part of such a team.

PCEA Chapter Spotlight

Bob McCreight, President of the Silicon Valley Chapter

On Feb. 13, 30 of us in the Silicon Valley Chapter enjoyed a sponsored "lunch and learn" and some very interesting presentations. After lunch, the technical director for design education at Insulectro, Mike Creeden, began the presentation portion by filling us in on the formation of the PCEA.

As the electronics industry is becoming aware, the PCEA is a new association formed to inspire and support collaboration and education between all facets of the PCB engineering, manufacturing and test sectors. There was a great amount of interest about the new organization from the audience, and several followed up with various queries.

Following a round of introductions from everyone in attendance, Faisal Ahmed, an application engineer at Cadence, provided a short demonstration of some new enhancements to Allegro, such as DesignTrue DFM Technology. This fresh take on design settings leverages technology files that are programmed to match the manufacturing capability from participating manufacturing partners. Designers now appear to have a direct link to DfM settings for some suppliers. Faisal also explained Cadence's 3D Canvas – a high-quality 3D visualization engine – and the Symphony Team Design Option, which allows multiple designers or teams to perform concurrent engineering using a shared canvas without setting up a partitioned project.

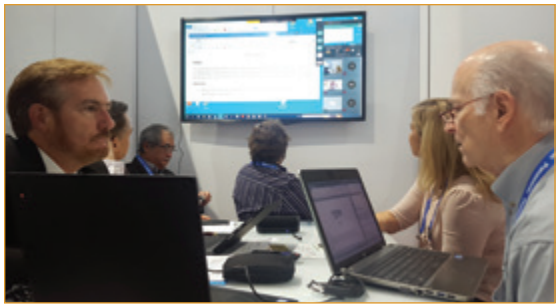

FIGURE 3. Members of the PCEA.

FIGURE 4. Atar Mittal.

Following the Cadence presentation, the meeting progressed to the feature presentation by Atar Mittal, general manager of Sierra Circuits' Design and Assembly Division (**FIGURE 4**). Atar presented his paper "Signal Degradation on PCB Transmission Lines: Causes and Remedies" and shared some vital points – including signal reflections, crosstalk, EMI, and PCB materials – comprising a very insightful talk that held

audience attention and resulted in a detailed Q&A session at the end.

All in all, the meeting went quite well. Our thanks go to Mike Creeden, Cadence and Sierra Circuits for providing their resources and expertise, which contributed to the success of this event.

Professional Development and Events

It has been our custom to highlight all upcoming industry events to look out for in 2020. We will continue this; however, with the challenges brought upon our industry by the Covid-19 outbreak, we can only remain hopeful these events will not be affected. If you have an interest in any of these events, please search and contact the event coordinators directly for the latest event status.

- June 13-18: IPC SummerCom 2020 (Raleigh, North Carolina)
- June 23-24: Realize LIVE 2020 (Virtual)
- September 8-11: PCB West (Santa Clara, California)
- Sept. 16-17: Del Mar Electronics & Manufacturing Show (San Diego, California)
- October 7-9: AltiumLive 2020 (San Diego, California)
- November 11: PCB Carolina (Raleigh, North Carolina)

We also want to spread the word. If you have a significant electronics industry event to announce, please send the details to kelly.dack.pcea@gmail.com and we will consider adding it to the list.

Conclusion

No matter what your part is in this industry, let's continue to move forward together by finding solutions for the unknown and having hope for the future. □

It's Often Maligned. But the Internet is Probably the Best Crisis-Management Tool We've Ever Had.

As we wait out Covid-19 at home, energy use and thermal management issues remain.

MANY OF US have been spending a lot more time with our computers than usual, working from home, shopping online, connecting with friends remotely, and consuming more streaming services. In the past, traditionalists have criticized such "virtual living," but in the current situation we are fortunate to have these services that help us connect and carry on without physical contact.

On the other hand, it seems the earth is enjoying the break, particularly areas of China and the US usually suffering from traffic smog, and in Venice's now clearer canals. The environmental effects of this unprecedented worldwide shutdown of human activity could provide interesting data to mull over as we seek solutions to our ongoing climate challenges.

It's less clear whether there will be any significant effect on global temperatures. Our online services are a lifeline, but running the internet consumes a huge amount of energy. It's reckoned that the six billion cumulative streams of the most popular music video in history – *Despacito* – have consumed as much energy as 40,000 US households in one year, generating carbon emissions equivalent to the annual output of 100,000 taxis.

We know the data centers at the heart of our cloud services consume huge quantities of energy. Operators have been keen to reduce consumption, at least as much to safeguard profitability as to save the planet. It's reckoned that efficiency improvements have cut data-center power consumption to about three-eighths of the level projected a few years ago. Even so, it takes more than 70 billion kWh per year to run the internet, which *Forbes* equates to about 1.8% of total US energy consumption.

Another well-known fact about data centers is that much of the energy supplied is dissipated as heat from servers and power supplies. Thermal management is a major engineering challenge addressed by measures such as water cooling and siting installations in cold climates to benefit from the increased cooling effect of a lower ambient temperature.

Technologies developed for high-end applications typically filter into the consumer space, and so it is with water cooling. Members of the gaming community are famed as PC power users, so we should perhaps not be surprised to find some intriguing looking water-cooled gaming PCs that flaunt their extreme engineering through the use of clear cases, clear coolant tubes, and custom options, including coolant dyes and colored lighting. I can see how hardcore gamers would relish the opportunity to turn their prized possession into the decorative centerpiece of a living room or dedicated gaming area.

Cost and complexity will likely prevent large water-cooling systems from becoming commonplace in ordinary desktop PCs, much less laptops and other portables. Fortunately, we, as engineers, have many other tools at our disposal to enhance cooling as the performance demands on computing systems continue to increase. Bear in mind low-loss substrates engineered to maximize signal integrity are designed to minimize the proportion of energy dispersed from high-speed signals into the motherboard and therefore contribute to alleviating thermal issues. These run the gamut from ceramic-filled composites widely used in telecom equipment, servers, backplanes, automotive and satellite communication equipment, and high-end handheld devices to insulated metal substrates for power-conversion and LED-lighting applications, which could also have a role in future computing applications.

Whichever techniques are employed to extract unwanted heat from hardworking system components, the challenge then becomes what to do with it next. Data-center operators have set up operations in cold climates to enable heat to be easily and cost-effectively dissipated by the lower ambient temperature. Clearly this option is not open to home computer users, but those involved in mining cryptocurrency may have a novel option: Recognizing the large quantity of heat produced by the compute-intensive process of calculating the crypto hashes needed to maintain the blockchain, commercial makers of mining rigs are now offering dual-purpose machines that double as space heaters for the home.

Mining bitcoin, currently perhaps the most mature cryptocurrency, is no longer the kind of activity done on ordinary PC CPUs. Having moved onto multi-GPU engines specially constructed from arrays of graphics cards, ASIC-based miners are now the weapon of choice to compete in a race that can realistically only be won by raw terahash-per-second computing capability. Even armed with these machines, owners are recommended to join a mining pool to combine their resources and share the rewards – paid in newly minted bitcoin, or BTC. (Having its own three-letter acronym does not mean the financial establishment – banks or governments anywhere – are ready to tolerate bitcoin. But that's a different story.)

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Who Should Be Concerned about the Fiber-Weave Effect?

Most boards will work just fine. But what if they don't?

OVER THE PAST year, I've written a good bit about glass-weave skew (GWS) and next-generation loss requirements, using PCI Express guidelines as a means of tracking what higher frequencies do to eye patterns. This month, we'll combine important elements of both these technology series, with just a bit of review in order to make this column one that can be read as-is.

The problem with human behavior is many of us wait for some sort of catastrophic event before we course-correct. When should we get serious about glass-weave skew, as opposed to ignoring it, while hoping it doesn't turn around and bite us at some point in the field? (A near-worst-case scenario.)

When I was marketing signal-integrity software in the 1990s, many engineers would appear on my radar *reactively,* playing whack-a-mole after spinning multiple prototypes or field failures. Over time, the list of possible causes grew to include crosstalk, loss in all its forms, and eventually power integrity. I've noticed many of today's hardware teams are sort of on cruise control relative to the "fiber-weave effect" as a design concern, so my objective here is to explore the concept of whether designers should worry about it *proactively,* given the potential impact of seemingly random field failure in production.

Background. Practically speaking, glass-weave skew and the fiber-weave effect (FWE) are the same thing. Or, more accurately stated, the fiber-weave effect *causes* glass-weave skew. Semantics aside, the fiber-weave effect is caused by one signal in a differential pair seeing a different micro-environment than the other signal in the pair. This is caused by the fact that "E" glass has a Dk of around 6.8, and resin has a Dk of around 3.0, though it varies from one resin system to the next. **FIGURE 1** shows if one signal is primarily adjacent to glass (P) in the resin-epoxy dielectric mixture, and the other differential signal is running across a mixture of glass and resin (N), the effective Dk is going to be different for the two signals, resulting in impedance and propagation-velocity variation as well.

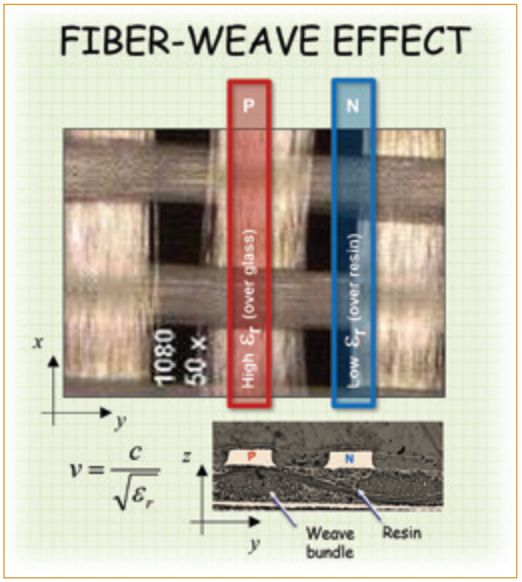

FIGURE 1. The semi-random alignment of differential signal routing, shown in red and blue, vs. the underlying glass alignment, often results in different average propagation velocities for each half of the differential pair. In this view, the positive differential signal is over glass (slower), and the negative side has a significant portion of the route over resin (faster). *c,* in the propagation-velocity relationship, is the speed of light.

Lee Ritchey provides TDR results showing these effects, while contrasting two different glass styles: 1080 and 3313 mechanically spread glass (**FIGURE 2**). Notice how much more uniform the impedance is as it travels across the glass weave when signals run parallel to both the weave (navy blue) and the fill directions (purple and green plots) compared to 1080 glass. This results in very low skew. Weaves known to cause skew in differential pairs include 106, 1080, 2116, and 7628 glass.

The 1080 glass exhibits a 5Ω swing. With the 3313MS glass, impedance variation is much less significant, with the variation parallel to the weave direction more significant than the signal running parallel to the fill.

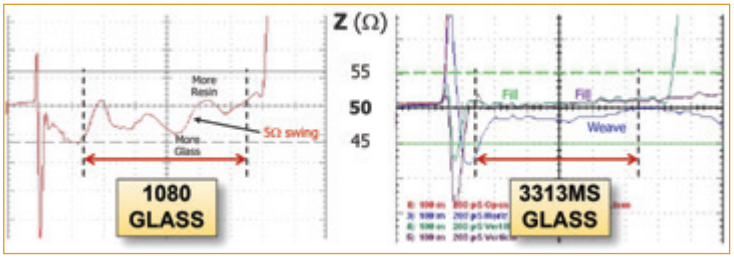

FIGURE 2. Impedance variation for a signal on 1080 glass on the left contrasted to impedance variations for a signal parallel to mechanically spread 3313 glass in both the weave direction (navy blue) and the fill direction (green and purple).

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Each differential serial-channel standard and speed has its own tolerance for skew. Most standards or chip manufacturers offer guidance on skew tolerance, but we can generically characterize that a channel's tolerance for skew is described as roughly 25% of the bit stream's unit interval (UI). For example, a 1Gbps (500MHz) signal would have a UI of 1000ps. Using 25% as a guideline, that represents a 250ps skew tolerance. That's a pretty wide window, and why most engineers didn't need to worry about GWS 20 years ago. Fast forward to designing at 10Gbps (5GHz). The unit interval will be 100ps, and the skew tolerance will decrease proportionally, to around 25ps.

PCIe example. We could talk about any number of bus standards, but I prefer to use PCI Express, since it's one many of us are familiar with. Doing the same math as above, **TABLE 2** shows that as you progress from PCIe 3.0 to PCIe 4.0 and PCIe 5.0, the tolerance for skew from all sources goes from 31ps, which is tight to begin with, down to 8ps. At any of these bus speeds, hardware designers can no longer ignore the prospect of glass-weave skew sneaking in and semi-randomly compromising otherwise well-planned designs!

Next, we'll explore what actually happens to otherwise-pristine eye patterns.

Glass-Weave Skew's Impact on Eyes

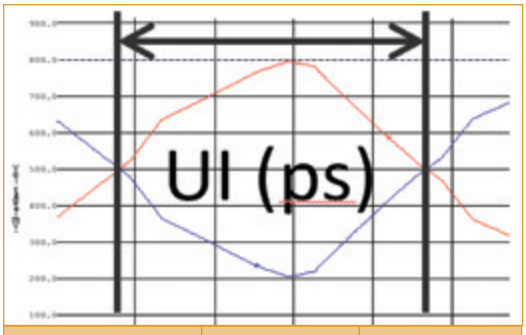
PCI Express 3.0. **FIGURE 3** shows simulation results for an 8-Gbps signal using a material that was successful on platforms that used PCIe 3.0. The blue keep-out region doesn't have any bits encroaching on it, which is what we want. This is simply intended as a high-level example of the interplay between frequency, eye mask, eye diagram and skew.

According to Table 2, if we introduce 45ps of fiber-weave-effect-induced skew into this differential signal – one that was already near the edge, as shown in Figure 3 – the eye pattern should be compromised. **FIGURE 4** shows this is indeed the case. The 25% unit interval rule-of-thumb seems to hold true here. The actual amount of glass-weave skew can be significantly more, depending on the interconnect length and the semi-random alignment between the two lines in a differential pair compared to the underlying glass fabric.

PCI Express 4.0. Keeping with this theme, let's consider a more expensive, lower-loss material for the next-generation requirement. We'll use 16Gbps and the PCIe 4.0 eye mask. **FIGURE 5** shows the result. Note the vertical scale was changed, adapting to the tighter keep-out requirements for PCIe 4.0 compared with 3.0.

Using guidance from Table 2, if we

TABLE 1. Data Rates, Unit Intervals and Approximate Tolerances for Skew[1]



Data Rates (Gb/s)	**Unit Interval** (ps)	**Quarter UI** (ps)
1	1000	250
2.4	416	104
3.125	320	80
5	200	50
6.125	180	45
10	100	25
13.5	74	18.8
27	37	9.25
40	25	6.25
100	10	2.5

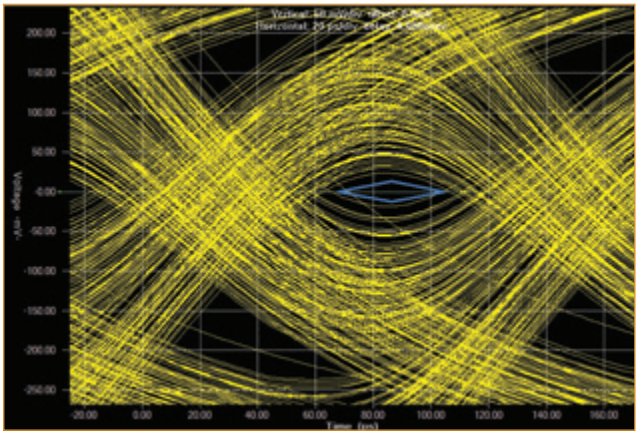


FIGURE 3. Intel PCI Express 3.0 simulation and eye mask from Mentor HyperLynx software.

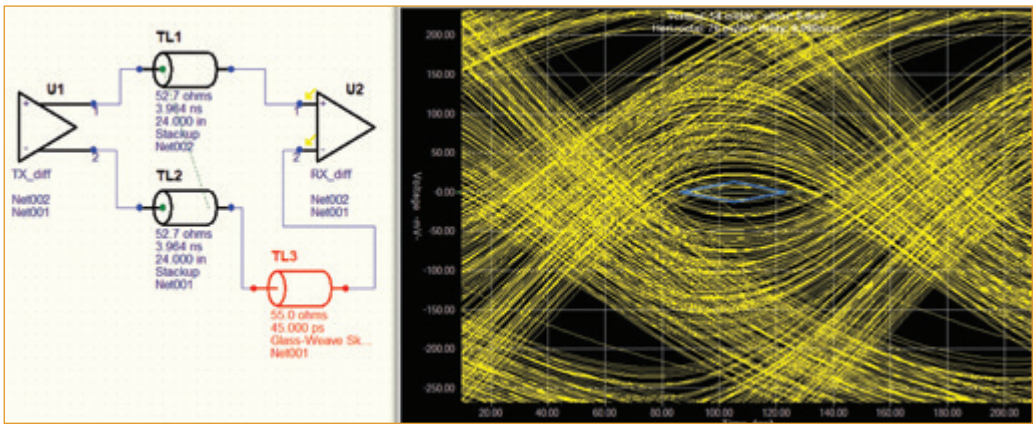


FIGURE 4. Intel PCI Express 3.0 simulation and eye mask with 45ps of glass-weave skew introduced.

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introduce just 16ps of fiber-weave-effect-induced skew into this differential signal – one that was already near the edge, as shown in Figure 5 – the eye pattern should be compromised, as **FIGURE 6** shows. The same amount of skew that was perfectly acceptable for PCIe-3.0, 16ps, was absolutely *unacceptable* for PCIe-4.0.

PCI Express 5.0. The same simulation exercise could be performed for PCIe 5.0 and higher frequencies, although the task of producing acceptable eye patterns at the receiver gets much tougher and of course the tolerance for skew decreases, as expected.

Parting thoughts. One of the problems with the fiber-weave effect is prototypes may work just fine. And 95% of the signals on 95% of the boards may work just fine. Systematic elements tied to glass-weave skew result from most trace routing running parallel to the weave and fill directions in the adjacent glass weave. And there's a systematic element tied to frequency effects, design margins and the pitch of the differential pairs as they relate to the adjacent glass. More of these effects are controllable than hardware designers realize, in my observation.

And mitigating the risk begins with the realization that this may be something you need to be concerned about as speeds increase. The frequency guidelines offered here hopefully answer the question I posed at the top.

For glass-weave skew mitigation tips, I covered the means by which glass-weave skewed can be controlled in a previous series in PCD&F. Part 2 surveyed the options, and parts 3 and 4 drilled into more detail, including glass styles and differential pitch. See pcdandf.com for more details. □

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1. Lee Ritchey, Speeding Edge, "Minimizing Skew in High Speed Differential Links," December 2015.

TABLE 2. Data Rates, Unit Intervals and Approximate Tolerances for Skew for Recent Generations of PCIe

	Frequency (Ghz)	**Data Rates** (Gb/s)	**Unit Interval** (ps)	**Quarter UI** (ps)
PCIe 3.0	4	8	125	31
PCIe 4.0	8	16	63	16
PCIe 5.0	16	32	31	8

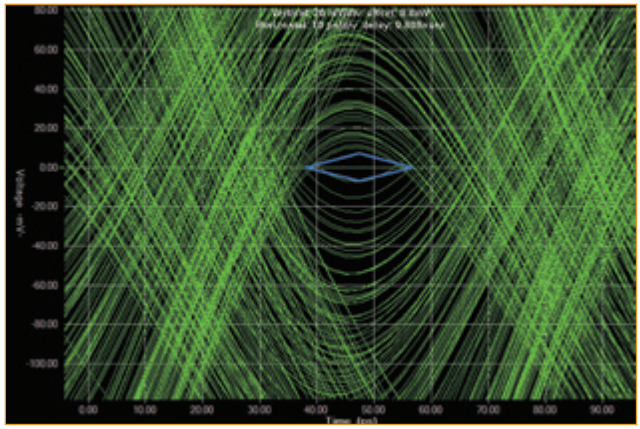

FIGURE 5. A barely acceptable PCI Express 4.0 simulation and eye mask using Mentor HyperLynx software.

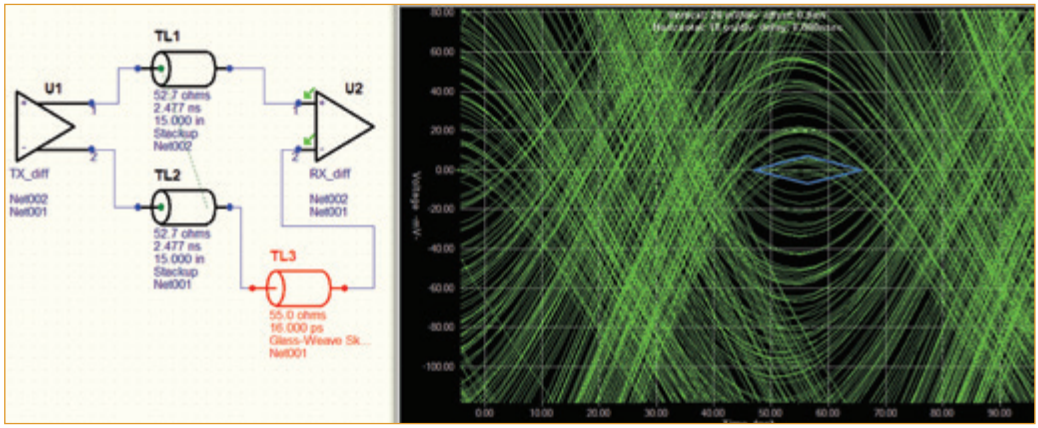

FIGURE 6. Intel PCI Express 4.0 simulation and eye mask with 16ps of glass-weave skew introduced.

MULTI-BOARD DESIGN for Applications with Different Voltages

The benefits of developing all boards of a system concurrently on a single CAD canvas. **by RICHARD WARRILOW**

A multi-board system comprises two or more interconnected PCBs in a single enclosure. Typically, the boards will have very different roles. For example, if you consider e-mobility (i.e., the industry trend of switching over to electric drive trains and actuation in the automotive, aerospace and other transportation sectors), many modules are multi-board systems. One board will be a controller. Another will be for switching in and out potentially high current loads.

While they share many common design and manufacturing considerations, the PCBs will warrant special attention when it comes to their specific roles. In this respect, the controller board might be very high-density and feature BGA devices (with hundreds of balls each), flip-chip devices, wire-bonded die and embedded components (i.e., the PCB substrate contains structures with resistive and/or capacitive properties).

The controller board may also feature high-speed digital and possibly even RF signals, and ensuring signal integrity through impedance matching will be of paramount importance. As for the power board, it may need to handle hundreds of amps, so thermal management may be the biggest challenge.

All in one. Modules containing PCBs with dedicated functions have been around for decades. All e-mobility sectors are now looking at how the boards are physically connected. A current trend is to mount them on top of each other, with the controller board placed as if it were a large BGA device on the power board.

The advantages of board-stacking are many. Most benefits derive from no longer needing mechanical connectors and cables. For example, there are cost savings because there are fewer parts; assembly is simplified (also a cost-saver), and reliability is improved through virtue of not having "mechanical" links formed using connectors and cables.

These benefits come at a price, however. The design process is now more complex, and we are, for all intents and purposes, designing two PCBs at the same time – at least the first-time around, after which one or both boards might be used in subsequent projects.

Clearly, the physical connections – i.e., where the module's bumps connect with solder-paste pads on the main board – must align precisely and be electrically correct, with no signal mismatches between boards.

Designing the boards in a single environment – again, there might be two or more – has considerable advantages. Some ECAD tools support such concurrent design in a single canvas. At the schematic level, connector symbols are used to represent interfaces between boards. These connectors initially exist as a temporary component on each board and build up the connectivity between both.

Typical flow. For layout purposes, start with the controller board. Define its shape and size, and place all standard components. Most would be placed on the top side but, as mentioned, embedding (if only partially) is an option. Some design tools automatically create a temporary component for placement on the underside of the controller board. This temporary component exists initially as connection point crosses, an indication of pad (or ball, if you prefer to think BGA) positions and padstacks.

Regarding placement of each pad, the signal's "intent"

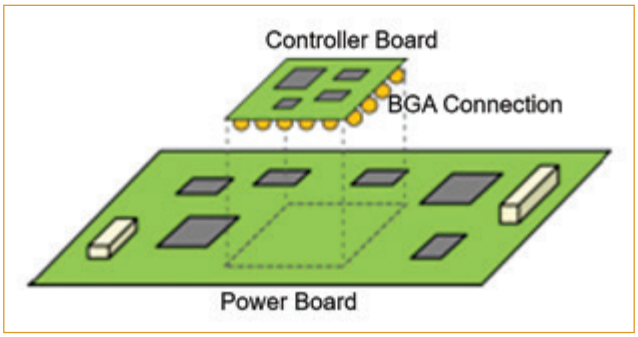

FIGURE 1. Mounting controller boards onto power boards is a growing trend in e-mobility sectors, and CAD software enables design of multiple boards in a single environment.

must be a factor. In other words, for a signal that must connect with the base board, routing from the pad of a topside component to the nearest pad on the underside might be practical for the controller board. However, it may not be as convenient for the base board to receive the signal from that physical location.

Next, the base board would be assigned a shape and dimensions. Again, all standard components would be placed. The controller board would be assigned to the temporary component of the base board schematic and subsequently placed at its intended position.

As with the assigning of signals to pads on the controller board, the same considerations apply for the base board. Signal integrity must be maintained through, for example, impedance matching for high-speed signals. Here, the beauty of working in a single canvas is impedance matching can be managed for signals that transition between boards.

Indeed, design rule-checks (DRCs) should flag an infringement, such as failing to maintain a suitable galvanic isolation distance when routing high current signals. Accordingly, if the pad of one board is reassigned, then executing an "update" will keep the two design parts in sync. For example, to reduce crosstalk, it is sometimes necessary to switch the +ve and -ve halves of an LVDS signal over. If the signal transitions boards, the inversion needs to be made on both.

Electrical updates are not the only ones that can be easily implemented. Sometimes, it is necessary to move one or more pads relative to the others, and we have this flexibility if the underside of the controller board and its position on the base board exist as temporary components. The traditional BGA grid is a default starting pattern.

Stacked in your favor. The benefits of designing the PCBs for a multi-board module – at the schematic entry and board layout levels – are considerable, and the practice is proving increasingly popular. Whether the top board is regarded as a "component" or as part of the single board (that happens to have different design requirements and therefore rules) is academic, and electrical and physical continuity (pads) is assured throughout.

Also, it does not matter if the board technologies vary considerably. For example, if the base board of a module will be close to a heat source – such as a combustion engine or power inverter – it can be prototyped in FR-4, be functionally verified on the bench, then the design re-spun for ceramic. The controller board would then be a forced-air-cooled component on that board. ❑

RICHARD WARRILOW is a former hardware engineer and technical writer.

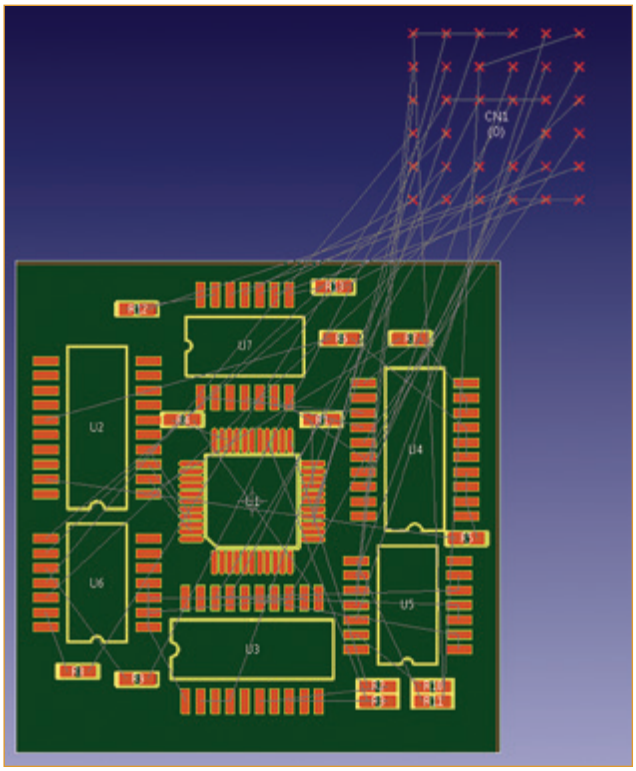

FIGURE 2. Multi-board system design is greatly simplified when the designs exist in a single environment and the designer can see roughly where the board-to-board connections must go.

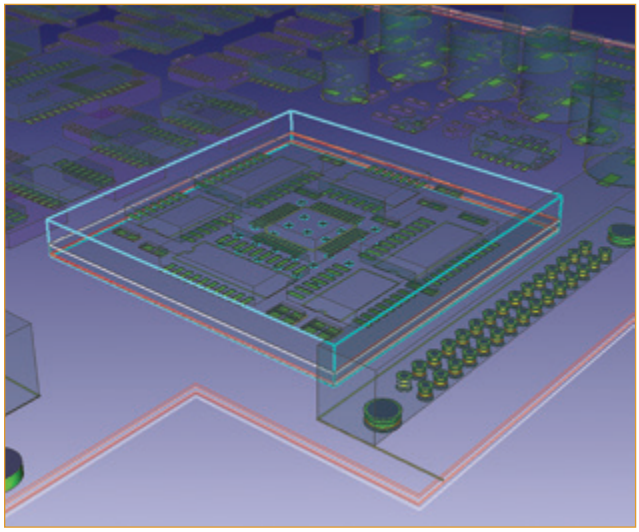

FIGURE 3. When designing multi-board systems, any board intended to be mounted on top of another exists as a temporary component – making placement easy.

Minimizing the EFFECTS OF VIAS on Very High-Speed Digital Signals

Unwanted capacitance hanging off signal traces can cause unwanted resonances and excessive attenuation. **by LEE RITCHEY**

Data rates for very high-speed data links keep climbing. PCI-Express Gen 4 is 16Gb/s, and Gen 5 is 32Gb/s. Data rates on links in high-speed routers and servers are as high as 56Gb/S. RF engineers would call all these microwave frequencies, even though they are "just" digital. It should come as no surprise that elements that did not matter at lower data rates can have significant effects at much higher data rates. Vias are one of these.

It has been shown many times that the vias used to connect signal pins to traces on innerlayers of PCBs are visible. It has also been shown that the effects of these vias can be ignored at the clock frequencies used until the advent of very high-speed differential signaling. Much to the dismay of design engineers, at very high data rates these vias often are the source of unexpected signal degradation, often to the point of failure. Here we show examples of this degradation and where it comes from, along with methods for minimizing this degradation.

For the purposes of this article, "via" refers to any plated through-hole used to connect a signal trace to a component pin or a connector pin. A via has distributed inductance along its length just like any other conductor. A via also has distributed capacitance along its length, formed by the barrel of the plated hole and the surrounding planes through which it travels. When a signal travels the length of the via, the two parasitics, capacitance and inductance, form a transmission line much like any signal trace. When the signal travels only part of the length of the via, some of the capacitance is left hanging off the signal trace. This is often called a "via stub" by mistake. **FIGURE 1** shows the effects of these two choices. The layer-changing via is located in the center of each trace.

Notice in the case of the signal traveling only part way along the via (left-hand waveform), there is a negative-going reflection, which is what one expects when a small capacitor is attached to a signal trace. In most cases, this small reflection does no harm, and we use vias freely. (The negative-going reflection at the start of the waveform is the via used to access the trace with a TDR.) As shown by the right-hand waveform in Figure 1, when the signal travels the full length of the via, this capacitance is spread along the lengths of the via, and a very small reflection is positive-going, indicating a very small decrease in capacitance because the via used this way has an impedance slightly higher than the 50Ω trace it is part of. We have effectively made the via "disappear."

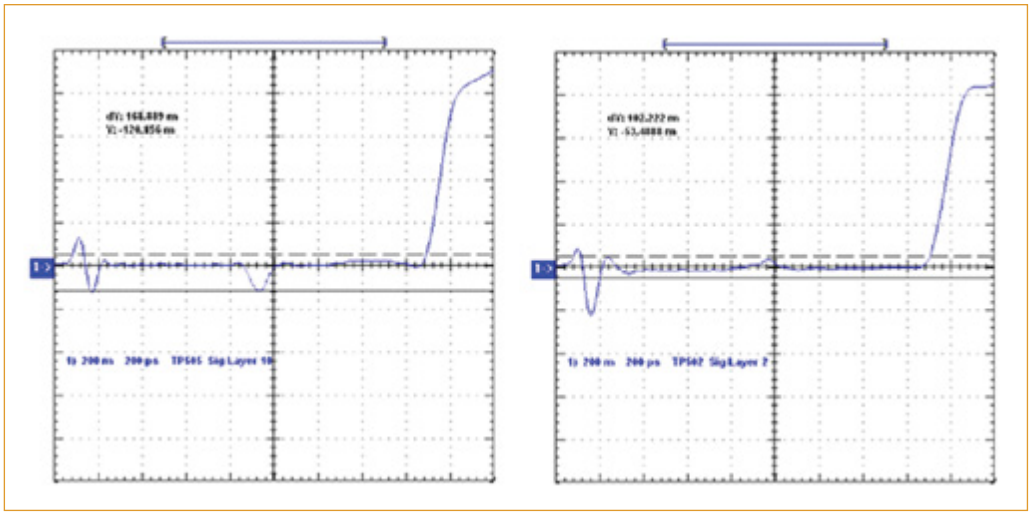

FIGURE 1. Signals traveling various lengths of a layer-changing via. (a)TDR result for trace traveling from L9 to L10 in a 22-layer PCB. (b)TDR result for trace traveling from L2 to L21 in a 22-layer PCB.

FIGURE 2 shows the loss vs. frequency

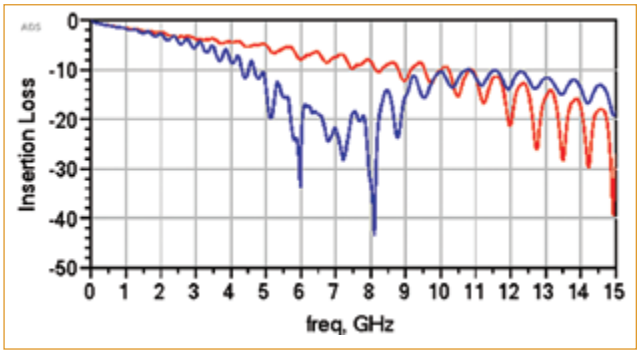

FIGURE 2. Loss vs. frequency for two different signal paths.

for two signal paths. The signal paths are both 8" long (20cm). Each has a 12-mil (0.3 mm) drilled via at each end. The PCB is 108 mils (2.74mm) thick. The red trace is the loss vs. frequency for the signal routed on layer 14 of the 16-layer PCB, permitting the signal to travel nearly the full length of the via. The blue trace is the loss vs. frequency for the signal routed on layer 3 of the same 16-layer PCB. Notice how severe attenuation is at 8GHz on the blue waveform. Suppose this blue trace were the signal path for a PCIExpress Gen 4 signal. The link would likely fail due to excessive attenuation.

Equivalent Circuit of Signals in Figure 2

FIGURE 3 is an equivalent circuit of the signals measured in Figure 2. As the energy traveling down the transmission line encounters each via, a small amount reflects toward the source. When the remaining energy encounters the second via, again some reflects and encounters the first via. If the frequency is just right, this energy reflects back and forth and is trapped there, thus being attenuated. An RF engineer might also call this a low-pass filter.

The shape of the loss curve resulting from multiple vias on a net depends on two things: The first is how large the vias are, and the second is how long the connecting trace is. For vias used for press-fit connectors on backplanes, the via capacitance can be as large as 2pF. This can result in attenuation at much lower frequencies than those in Figure 2.

Why isn't this a problem for long nets? Steinberger[1] describes a server design where none of the long 10Gb/S nets failed, and the short ones did. Most engineers have focused on making sure the loss in the long nets is low enough they do not fail and assume the short nets will be fine. What Steinberger's case shows is that only the short nets failed, even though the long nets had the same number of vias. The reason the long nets didn't have the problem shown in Figure 2 was there was enough loss in the signal path that the reflections were attenuated and did not cause problems. This is an example where loss is your friend.

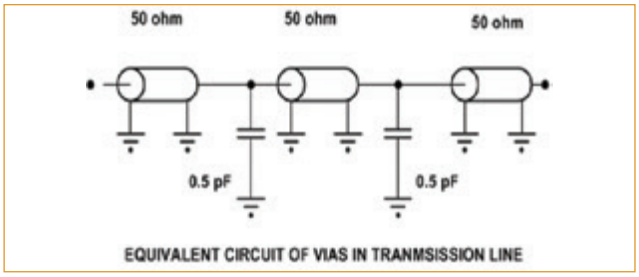

FIGURE 3. Equivalent circuit for signals in Figure 2.

Mitigating Effects of Vias in Short Nets

Since it is clear unwanted capacitance hanging off signal traces can cause unwanted resonances and excessive attenuation of a signal, minimizing its presence is desirable. There are several ways to do this (see below), and they have merits and drawbacks.

Use only layer one for very high-speed signals. This is a very good choice, provided there is room for all the signals on layer one. This won't work for a backplane design since L1 is the poorest for impedance control, because it is an outer layer.

Traveling the length of the vias routing only on the lower layers. This is the best choice, provided there is room on the lower layers for all the signals. Impedance control is very good at no added cost. The author has designed several PCBs using this technique, where there were dozens of 28Gb/S differential pairs, with very good results.

Route signals in any layer and backdrill away the part of via below the trace layer. This is necessary for backplanes, as all signal layers are likely to be used for very fast signals. Backdrilling is a second operation after the PCB has completely fabricated and adds significant cost. There is also the risk of drilling too deep and severing connections to trace layers.

Route the signal on Layer 2 and access with a laser-drilled blind via. This method represents the best tradeoff

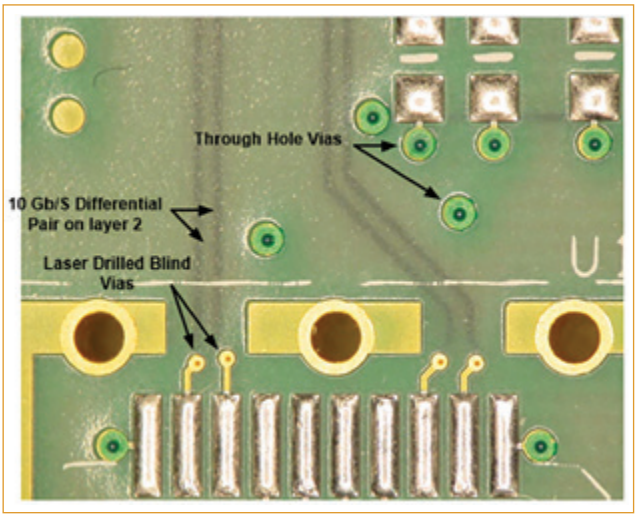

FIGURE 4. A laser-drilled blind via accessing a 10Gb/s differential pair on layer 2.

between manufacturability and signal integrity, as the blind via has virtually no added capacitance. Blind vias are laser-drilled at the same time as through-hole vias, representing only a very small change in processing. The disadvantage is there may not be enough room on layer 2 for all the signals. **FIGURE 4** is an example of routing a 10Gb/S signal pair on layer 2 with blind vias for access.

As speeds of differential pairs continue to increase, small discontinuities, such as vias, can cause catastrophic failures. Managing these discontinuities has become a critical part of the layout rule set for engineers and PCB designers. If these rules are carefully constructed, it is possible to achieve data rates as high as 56Gb/s using high-performance laminates and standard PCB fabrication processes. □

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1. Michael Steinberger, Ph.D., *et al,* "When Shorter Isn't Better," DesignCon, February 2010.

LEE RITCHEY is considered one of the industry's premier authorities on high-speed PCB and system design. He is the founder and president of Speeding Edge (speedingedge.com), an engineering consulting and training company, and will speak at PCB West in September; leeritchey@earthlink.net.

Material Gains, continued from pg. 16

Mining bitcoin is getting tougher, by design. The system is architected for a maximum of 21 million bitcoins and, although 98% are expected to have been issued by 2030, the final 2% will take until 2140 to mine. However, other cryptocurrencies are available – to (not) coin a phrase. Ethereum, for instance, operates on slightly different principles, and hashes can still be generated effectively using an independent GPU-based mining rig. However, the volatility of cryptocurrencies, and the high price of energy needed to keep calculating hashes, mean the profits from mining are uncertain. Depending on local climate and electricity charges, a discounted heating bill may not be enough to break even.

For many of us, staying warm is probably not our biggest problem right now. Whatever you do, stay safe. □

QUALIFIED MANUFACTURING PROCESS Development by Applying IPC J-STD-001G Cleanliness Standard

A test vehicle and qualification test for proving out process changes. by MIKE BIXENMAN, VLADIMIR SITKO and MARK MCMEEN

IPC J-STDF-001G states, "Unless otherwise specified by the User, the Manufacturer shall [N1D2D3] qualify soldering and/or cleaning processes that result in acceptable levels of flux and other residues. Objective evidence shall [N1D2D3] be available for review."[1] (*Ed.:* N1D2D3 means no requirement has been established for Class 1, and the condition is a defect in Classes 2 and 3.)

In a qualified manufacturing process (QMP), manufacturing materials and processes used to produce electronics hardware are benchmarked and validated against electrical performance in hot/humid conditions.[2] Characterizing chemical residues that exist on a manufactured assembly, and assessing the impact of those residues on electrical performance, has much to do with the end-use environment in which the hardware will operate. The other important factor is the circuit density and component types. Leadless and bottom-terminated components are more susceptible to residue challenges due to low standoff gaps, tight pitch, high solder mass, and blocked outgassing channels.

Here, we assess the impact of process residues on electrical performance to qualify electronics hardware and the manufacturing process. The qualification methodology will determine the acceptability of the residue condition at the point of the manufacturing process just prior to the application of conformal coating.

All manufacturing processes result in residues on circuit assemblies in one form or another.[3] Manufacturing processes also have some variation that is part of daily manufacturing. Changes in manufacturing materials and processes, whether intentional or unintentional, can change the residue condition on the manufactured product. Materials characterization is needed to define process conditions to render electronics hardware with acceptable levels of flux and other residues. Designing for electrochemical reliability requires the assembler to consider the major elements that impact residue levels:

- Flux or flux-bearing materials (e.g., flux, solder paste, paste flux, cored wire solder).
- Cleaning agents (e.g., solvents, aqueous detergents, topical cleaners).
- Changes in manufacturing suppliers.
- Changes in solder mask type.
- Changes in printed board fabrication processes or surface metallization.
- Geographic change in manufacturing location.

The objective of material and process characterization and qualification is to quantify any harmful effects that might arise from solder flux or other process residues on external surfaces after soldering requires test vehicles representative of the electronic circuits. Test vehicles designed to evaluate electrical and chemical properties can demonstrate that a manufacturing process or process change produces electronics hardware with acceptable end-item performance related to electrochemical risk.[3] Changes may involve any assembly process step, a change in the printed circuit board supplier, solder mask or metallization, soldering material supplier, cleaning agent, cleaning tool, conformal coating, etc. The test vehicle construction will vary to be representative of the actual production hardware.

Test vehicles should be prepared at the manufacturer's location using production processes and equipment whenever possible. Care must be taken to ensure the processed test vehicles are kept free from any secondary contamination while in transit to the test site. Testing of the prepared test vehicles can be performed by the user or at a suitable independent laboratory.

The electrical test method allows an assembler to perform material and process characterization/qualification. This test records changes in surface insulation resistance (SIR) on a representative sample of a printed circuit assembly. During this test, ionic contaminants dissolve in moisture. This solution forms an electrolyte, which is a substance that produces an electrically conducting solution when dissolved in a polar solvent, such as water.[4] This electrolyte can mobilize metal ions present in either the residue or at the soldered areas. When an electrical potential is applied, the metal cations flow to the negative electrode. The metal ions start to form small dendrites known as leakage currents. These leakage currents cause a downward drop in insulation resistance (**FIGURE 1**).

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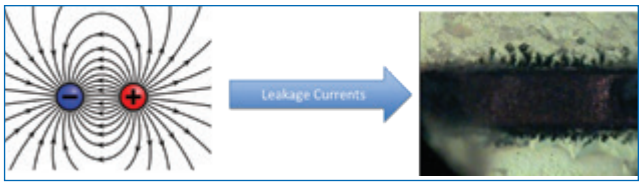

FIGURE 1. Resistance properties.

Conversely, when there are no problematic ions present, insulation resistance will remain stable and high.

Methodology

The following materials and equipment were used to qualify a soldering and cleaning process that results in acceptable levels of flux and other residues on components that are specific to production hardware.

The solder paste was a no-clean (R0L0), halogen-free SAC 305 alloy. The cleaning agent had high solvency for flux vehicles, multi-metal compatibility in both packaging and assembly, automatically controllable cleaner/water intermix, and improved bath life by holding soils in the aqueous phase.

The cleaning tool (**FIGURE 2**) is linear spray-in-air type, effective at cleaning leadless and bottom-terminated components. It features deflection energy and targeted spray patterns, programmable wash, rinse and dry periods, and drying under low-gap components.

Experimental

The properties of the flux residue, component types, cleaning agent, cleaning machine and process conditions can affect the ability to remove process residue. Leadless and BTC parts are typically more challenging to clean. The low-standoff gap and tight pitch can require longer cleaning time, focused cleaning energy, and higher wash temperatures. Glass test boards populated with ceramic 0805 chip caps (**FIGURE 3**) are excellent for dialing in the cleaning process conditions needed to remove flux residues under low-profile components.[5]

The test board is prepared as follows (**FIGURE 4**):

1. Order the flux portion of the solder paste from the manufacturer.
2. Dispense a bead of the flux vehicle along the top row of chip caps.
3. Place the test board on a hot plate. Elevate back legs to a 15° angle for the base plate. Maintain a temperature range of 45°-60°C. As flux goes to the liquid state, the flux wetting properties will permit the flux to flow under chips. Squeegee off excess flux.
4. Reflow the glass slide using the profile used to build production hardware.

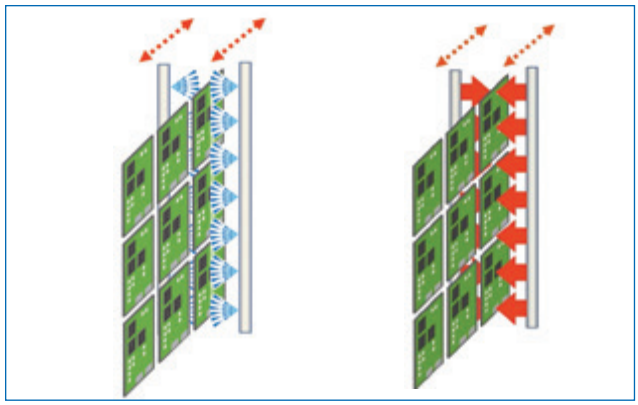

FIGURE 2. Cleaning tool design.

The data find that wash temperature reduces cleaning time (**FIGURE 5**). With a good understanding of the wash temperature and wash time to remove flux residues from under leadless components, a DoE was designed to perform temperature-humidity-bias (SIR) testing.

SIR Test Method

SIR testing is a standard method used to characterize soldering and cleaning processes that result in acceptable levels of flux and other residues. The experimental DoE is reported in **FIGURE 6**. The factors studied are wash time, wash temperature and rinse time.

The test board (**FIGURE 7**) was set up as follows:

- Channel 1: QFN component representative of bottom-termination components used on production hardware.
- Channel 2: BGA with center lug representative of grid arrays used on production hardware.
- Channel 3: QFP-160 to test cleanability of tight pitch lands and rinsing effectiveness.
- Channel 4: An array of caps representative of capacitors

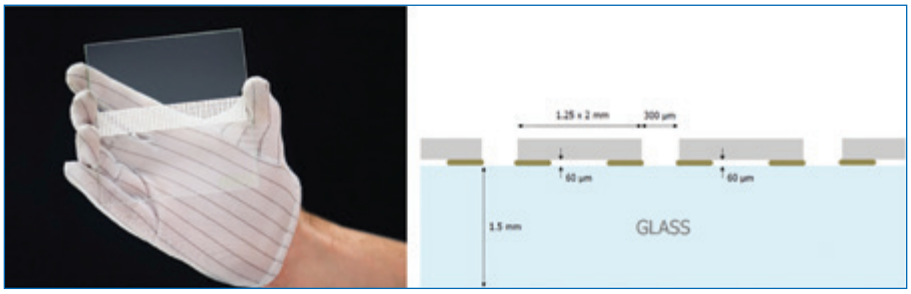

FIGURE 3. Glass test boards populated with 0805 ceramic chip caps.

FIGURE 4. Preparation of glass test board.

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and resistors used on production hardware.

- Quadrant 1: QFN48T.5-F-ISO (48 leads, body 7 x 7mm, pitch 0.5mm.
  - Edge Pin1 = Odd pads | edge pin 2 = Even pads + gnd lug.
- Quadrant 2: FBGA 244 (244 leads WG, body 19 x 19mm, pitch 1mm).
- Quadrant 3: QFP160 (160 leads, body 28 x 28mm, pitch 0.65mm).
- Quadrant 4: QTY 10 each of the following: 10pF caps 0805, 0603, 0402, 0201.

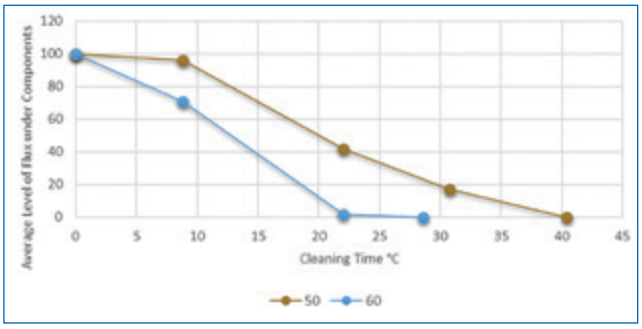

FIGURE 5. Cleaning time as a function of wash temperature.

TABLE 1. Experimental DoE

Solder Paste	Cleaning Machine	Nozzle Span (mm)	Cleaning Agent	Wash Conc. (%)	Wash Time (min.)	Wash Temp. (°C)	Spray Pressure Bar	DI Rinse I (min.)	Rinse Temp. (°C)	DI Rinse II (min.)	Final Rinse Conductivity (µs)	Rinse Temp. (°C)	Dry (min.)	Dry Temp. (°C)
R0LO SAC 305	Linear SIA	80	Eng. Aq.	20	22	50	2.6	2.2	40	4.4	1.2	50	15	110
R0LO SAC 305	Linear SIA	80	Eng. Aq.	20	22	50	2.6	2.2	40	4.4	1.2	50	15	110
R0LO SAC 305	Linear SIA	80	Eng. Aq.	20	30.8	50	2.6	2.2	40	4.4	1.3	50	15	110
R0LO SAC 305	Linear SIA	80	Eng. Aq.	20	30/8	50	2.6	2.2	40	4.4	1.3	50	15	110
R0LO SAC 305	Linear SIA	80	Eng. Aq.	20	30.8	50	2.6	2.2	40	11	0.5	50	15	110
R0LO SAC 305	Linear SIA	80	Eng. Aq.	20	22	60	2.6	2.2	40	4.4	1.3	50	15	110
R0LO SAC 305	Linear SIA	80	Eng. Aq.	20	22	60	2.6	2.2	40	4.4	1.3	50	15	110
R0LO SAC 305	Linear SIA	80	Eng. Aq.	20	30.8	60	2.6	2.2	40	4.4	1.2	50	15	110
R0LO SAC 305	Linear SIA	80	Eng. Aq.	20	30/8	60	2.6	2.2	40	4.4	1.2	50	15	110
R0LO SAC 305	Linear SIA	80	Eng. Aq.	20	30.8	60	2.6	2.2	40	11	0.4	50	15	110

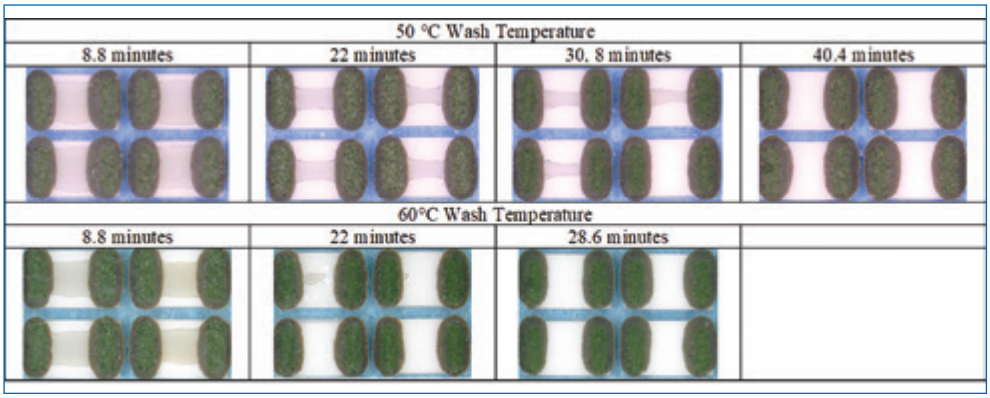

FIGURE 6. Flux residue as a function of cleaning time and wash temperature.

What is a "good" SIR number? When viewing SIR data, a common question is what is a good or acceptable number? That is a difficult question to answer. No single number has been determined to divide acceptable from unacceptable performance, and since SIR test data also depend on the geometry of the test electrodes, the data will vary by the test pattern. The chart in **FIGURE 8** records insulation resistance values in LogOhms on the y axis and the number of measurement sets on the x axis. IPC committees have generally agreed that values above 8 LogOhms are considered acceptable performance.

Unprocessed control board. An unprocessed control board, a test vehicle that has not been exposed to candidate assembly manufacturing material/processes, was run. The unprocessed control board used for this study was free of ionic contamination.

Data Findings

Each component type represents a different cleaning challenge. Studying components that have low-standoff gaps, and that trapped a significant level of flux residue under the bottom termination, allows assemblers to understand processing conditions needed to clean production hardware.

QFN. The bottom-terminated QFN component represents one of the toughest cleaning challenges. The standoff gap is typically less than 50µm (2 mils). Flux residue can underfill the bottom termination. During reflow, outgassing channels

can be blocked. The QFN is at high risk for leakage currents and dendritic growth when flux residue is present. In view of the difficulty of cleaning this component type, it may be considered a good focal point for evaluation. To clean this component, wash time, wash impingement, wash temperature, cleaning agent and rinsing are critical factors. The SIR data to understand wash time, wash temperature, and rinse time are shown in **FIGURE 9**.

The data find that most optimal wash parameters are:

- 60°C wash temperature.
- 30 min. wash time.
- 12 min. rinse time.

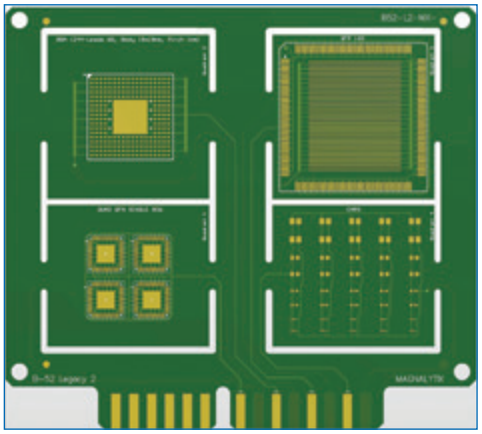

FIGURE 7. SIR test board.

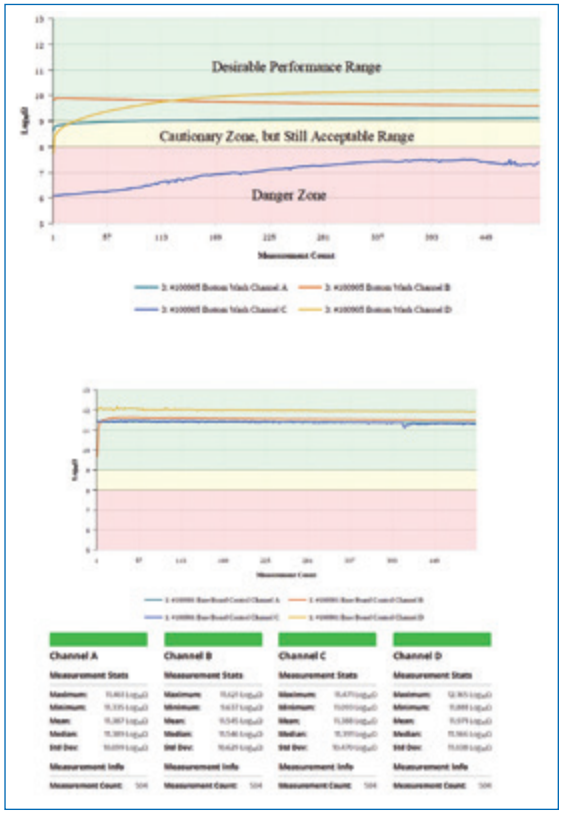

FIGURE 8. SIR data on unprocessed control board.

BGA with center lug component. The BGA (**FIGURE 10**) used on the test board has a standoff gap higher than 250µm (10 mils). The flux has ample channels to outgas. This component is typically easily cleaned, and therefore is generally not recommended as the best choice for benchmark to set cleaning parameters or other process conditions.

The data find that most optimal wash parameters are:

- 60°C wash temperature.
- 22 min. wash time.
- 6.6 min. rinse time.

QFP160 laminate dummy. The QFP160 laminate dummy (**FIGURE 11**) is a challenging component that has unique design attributes for gauging the ability to clean tight pitch pads (0.65mm) and rinsing under low-profile components. Solder paste is printed on the pads located under the bottom termination. The pad dimensions are 0.45 x 1.95mm. The tight pitch and pad length results in flux bridging the pads and blocking flow channels. This results in a highly difficult part to clean. The part can be thought of as a large QFN in reference to the cleaning challenge. The mechanical dummy has J-leads located around the four perimeters outside the package. The laminate dummy is a much more challenging part to clean than the J-lead mechanical dummy. The large SIR comb pattern adds a second dimension to the cleaning challenge. Wash fluids not fully rinsed will lower insulation resistance. This component can be thought of as the worst-case condition. Knowing this, the assembler can use this component as a gauge to better

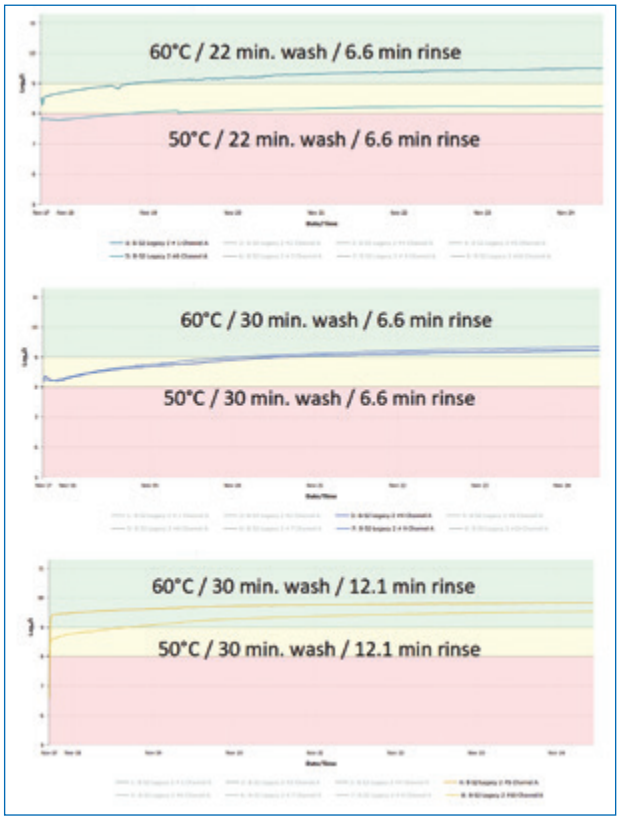

FIGURE 9. Data findings for the QFN.

define cleaning parameters.

The data (FIGURE 12) find the most optimal wash parameters are:

- 60°C wash temperature.
- 40 min. wash time. Note: We did not run longer than a 30 min. wash cycle. Insulation resistance improved with longer cleaning time. There is a high probability an additional 10 min. of wash will achieve acceptable cleanliness.
- 12.1 min. rinse time.

An array of caps representative of capacitors and resistors used on production hardware. Chip caps are leadless components commonly found on electronics hardware. The caps represent a cleaning challenge due to the low-standoff gap and tight pitch. It is not uncommon for flux to bridge the bottom termination.

The data (FIGURE 13) find that most optimal wash parameters are:

- 60°C wash temperature.
- 22 min. wash time.
- 6.6 min. rinse time.

Conclusion

SIR testing on a representative sample of a printed circuit assembly allows an assembler to qualify any harmful effects that might arise from solder flux or other process residues left on external surfaces after soldering. A test vehicle representative of the electronic circuits used on production hardware yields both quantitative and qualitative data. This test is used for process qualification, demonstrating a proposed manufacturing process or process change can produce hardware with acceptable end-item performance related to cleanliness.

The SIR test board contains test patterns adjacent to, and beneath, components. The components on the test board were chosen as representative of typical constructions and spacings used in electronics designs. The objective is to replicate the effects these components have on production hardware and their impact on entrapping process materials. These components are soldered onto the test board using assembly and cleaning methodologies that replicate production techniques.

Inferences from the Data Findings

Building reliable electronics hardware is a function of the following factors:

1. The end-use environment in which the hardware will be operated
   a. Moisture dissolves ionic contaminates. This electrolytic solution can mobilize metal oxides.
   b. Improper handling of electronics hardware can leave contamination that can impact electrochemical reliability.
2. Life expectancy
   a. Risk of failure must be understood using temperature-humidity-bias test conditions.
   b. Proper qualification and validation is critical to understanding the robustness of the process conditions used to build the electronics hardware.
   c. The impact of design, materials and manufacturing can be assessed using the SIR test method.
   d. Some components are more susceptible to electrochemical reliability than other components.
      i. Testing problematic components on a specifical design test vehicle can be used to extrapolate chemical reliability across a wide range of components.
3. Test methods
   a. Chemical test methods are useful in determining bulk cleanliness and for quantitating specific ions.
   b. Electrical test methods are useful in determining the robustness of electronics hardware when exposed to temperature, humidity and bias.

The test board populated with four leadless and bottom-terminated components illustrated how flux residue changes across components. This results from low-standoff gaps, narrow pitch, high solder mass, and flux outgassing. Flux resi-

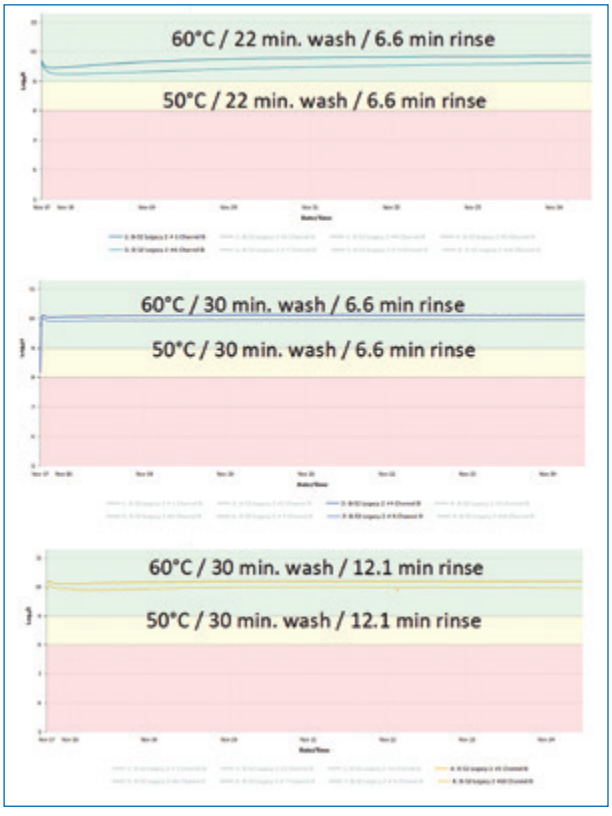

FIGURE 10. DoE findings for the BGA.

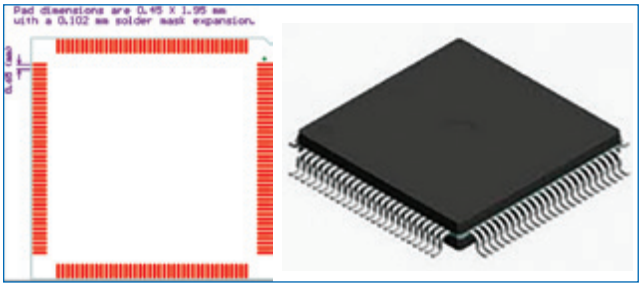

FIGURE 11. QFP 160 laminate versus mechanical dummy.

dues can bridge conductive pathways. The cleanliness of each component provides a risk profile for metal migration in the form of electrochemical leakage and dendritic growth when performing SIR testing.

Materials characterization of the soldering residues, cleaning materials, cleaning tool and process conditions provides the assembler with data from which to dial in the process. Temperature-humidity-bias testing allows the assembler to quantify any harmful effects that might arise from solder flux or other process residues left on external surfaces after soldering requires test vehicles representative of the electronic circuits. The qualification methodology provides "objective evidence" as to the acceptability of the residue condition at the point of the manufacturing process just prior to the application of conformal coating. . □

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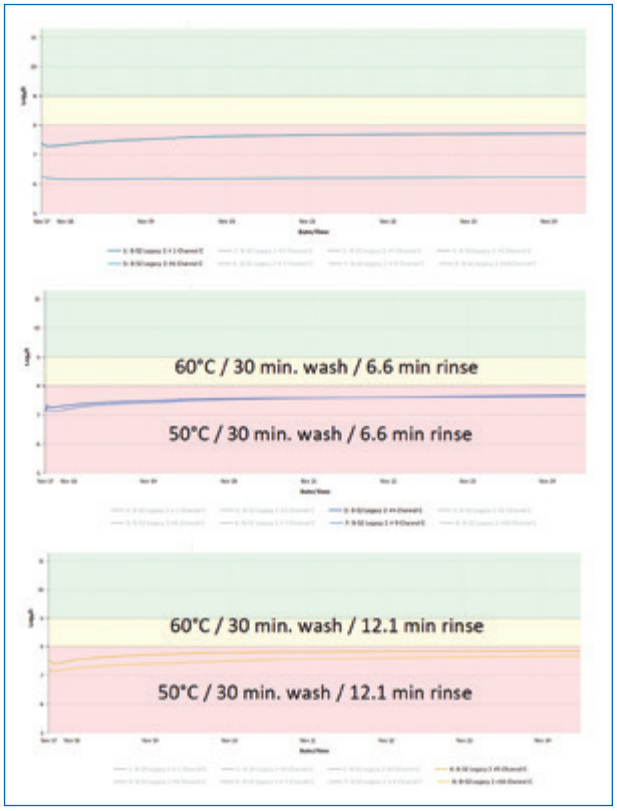

FIGURE 12. Data findings for the QFP 160 component.

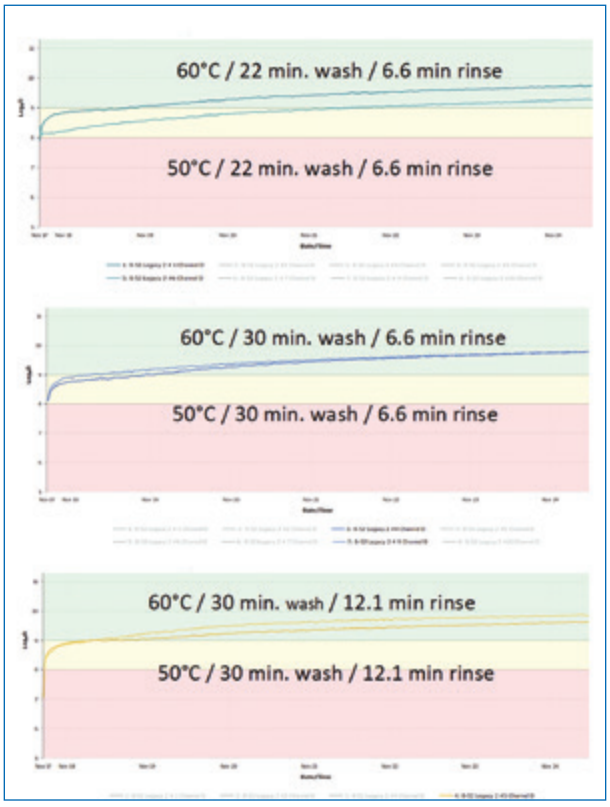

FIGURE 13. Data findings for the array of caps.

EMS 2019 in Review: Trade Wars Batter Supply Chains, Profits

The largest players in contract assembly toughed out last year. This one might be worse. **by MIKE BUETOW**

No matter what happened in 2019, it will be remembered as the end of a bull run. On financial charts, it will look 2001 and 2006, the last spike before the ensuing crash. As it now stands, it will take a significant surge over the rest of 2020 to make the year look respectable compared to the past several. Thanks, coronavirus.

As we roll out the CIRCUITS ASSEMBLY Top 50 EMS Companies list, we chronicle the past calendar year, where M&A activity rose, and many manufacturers spoke of tightening their profit belts.

It seems passé now, but for most of the year the big story was the escalating trade war between the US and China. Although the accusations and antagonisms were swelling on both sides for years, the US fired the first real shot, slapping tariffs on washing machine and solar panel imports in January, followed two months later with steep taxes on steel and aluminum imports. A month later, China retaliated with tariffs of up to 25% on more than 100 US-made products, and the battle was on. When all was said and done, supply chains were being revamped, and manufacturers were scrambling to adjust pricing and maintain margins.

In response to the higher selling prices and ongoing uncertainty, several companies announced or brought new factories online outside China. Vietnam was the big winner: Electronics exports to the US jumped 90% year-over-year (**FIGURE 1**). KeyTronic, Pegatron, Wong's International, Compal and Wistron were among those setting up shop, while Inventec and even Foxconn were considering new campuses there. Taiwan and Malaysia also reaped gains. Many Taiwanese-based ODMs relocated or added to their plants on the island. Malaysia saw ATA IMI, Hotayi Electronics, Seetek EMS and VS Industry among the companies adding capacity, and the country reported double-digit increases for overall electronics imports for the year. All three countries pocketed billions in new investment from US companies looking to avoid China.

As for the Top 50 EMS firms, much remained the same. No. 1 **Foxconn** has been atop the leaderboard for so long, it's hard to remember that 15 years ago it had less than a $10 billion lead over the next largest company. Today, the distance seems almost insurmountable. Overall, Foxconn's currency-translated revenues reached $177 billion last year. Just how much of that is pure ODM/EMS work is anyone's guess. The conglomerate has famously pushed into connectors and cables (Foxconn Interconnect Technology, Pan-International), semiconductors (Albit, now Shunsin), branded TVs and displays (Sharp, Innolux), branded networking gear (Belkin), and branded phones (FIH Mobile, which also owns a 6% stake in the company that designs Nokia's phones). Removing most of those companies (Foxconn does not list Sharp under its subsidiaries in its annual report) knocks $27.3 billion off Foxconn's annual revenue. Big deal. In other words, Foxconn could lose combined entities about the size of no. 4 **Wistron,** and still be more than $100 billion larger than no. 2. **Pegatron.**

Apple still accounts for half of Foxconn's revenue. Will that change post-Covid? Not in the near-term. Still, even with a new chairman in place – founder Terry Gou stepped down amid a failed campaign for Taiwan's presidency last year – don't expect any slowdown in Foxconn's relentless march toward total market domination. (It has even invested in organic farming. Look out, Whole Foods.) What makes Foxconn so interesting is how all its major acquisitions have taken

FIGURE 1. Electronics Exports to US, 2017-19. (Source: US Census Bureau)

place outside the EMS space. If true consolidation among the world's 6,000 or so EMS companies ever happens, I'd take the Foxconn against the field as to who will be standing at the end.

For the purposes of the CIRCUITS ASSEMBLY Top 50, we include the large flex circuit fabricators that also perform SMT assembly. This means **Zhen Ding Tech** (no. 23) and **Nippon Mektron** (no. 29) make the list. For our purposes, we estimate about 40% of their revenue comes from contract assembly. (Admittedly, that could be way off, and it's unlikely the companies themselves know for sure.) Our view is an OEM could purchase bare boards from ZDT and send them to, say, Jabil to assemble, or they could have ZDT assemble those same boards. Either way, it's a contracted assembly service.

Where possible, we do make concessions for non-SMT sales, however. So ZDT had about $4 billion in sales in calendar 2019, but once bare boards are subtracted, they are at about $1.6 billion, which is the figure we use. Likewise, we carve out nearly $10 billion from no. 8 **Jabil** to account for its engineered material unit, no. 11 **Sanmina** takes a $1.44 billion hit for its bare board and components sales, and no. 6 **Flex** gets dinged $50 million (an estimate) for its Sheldahl flex circuit business. When we do that, some companies like Global Brands Manufacture (GBM) drop from the list, because about 56% of its sales are bare boards.

Some companies offer confusing data. In its Shenzhen Stock Exchange listing, no. 48 **DBG** had currency-converted revenues of $314 million. But there's a catch: China and the US use different accounting practices. As DBG told us, Chinese practice excludes materials bought and sold for clients in its India factory. Under US guidelines, its revenue was $449 million. Who knows how many other Chinese companies are affected by this, and to what degree.

Despite the trade barriers, China's EMS companies are coming up in the world. They are tricky to track, however. Some go by several names. Others have ownership stakes that we would find unusual in the West. For example, New Kinpo Group, which is most associated with no. 14 **Cal-Comp**, also owns a stake in no. 4 **Compal.**

On that note, we list Cal-Comp Electronics (CCE), not its parent New Kinpo Group. Reason: NKG includes several non-ODM/EMS entities, including OEM and semi design companies such as XYZ Printing, CastleNet and Qbit Semiconductor. But there's a twist. Another NKG subsidiary, Cal-Comp Philippines, was scheduled to go public last year on the Philippines Stock Exchange. In keeping with initial public offering protocols, CCPH has posted its financials for 2016 to 2018, plus the first half of 2019. Due to market conditions, however, CCPH has twice pushed its planned IPO, most recently in November, and the firm has not yet released its second-half financials. As a result, our ranking includes full-year revenue from CCE plus $450 million from Cal-Comp Philippines, which is a CIRCUITS ASSEMBLY estimate based on actual first-half sales, historical second-half sales, and the changing market conditions.

Interesting quirk: We found the Japanese data relatively easier to come by this year.

TABLE 1. Currency Conversions

1 USD =		12-Month Change
	0.91 euros	0.20%
	7.04 Chinese RMB	0.02%
	7.75 Hong Kong dollars	-0.01%
	323.1 Hungarian forint	12.30%
	108.4 Japanese yen	-0.01%
	4.33 Malaysian ringgit	0.04%
	1.42 Singaporean dollars	0.04%
	9.93 Swedish krona	0.03%
	30.1 Taiwanese dollars	-0.03%
	32.7 Thai baht	0.03%

Currency factors. We calculate all companies' sales in their native currency, then convert to US dollars. We used exchange rates as of April 9. Unlike 2018, currency played a minor role in determining this year's rankings. The only serious movement was the Hungarian forint (**TABLE 1**), which impacted just one company, no. 38 **Videoton.**

Slow at the top. As noted, it was a touch-and-go year for the Top 50. Most of the top 10 were flat or lost ground in 2019. No. 10 **BYD Electronic** was the only firm to show significant growth on a percentage basis, up 29%, making it also the largest gainer in the Top 50. Five of the top 10 and 11 of the top 20 saw revenues shrink in 2019 (**TABLE 2**).

According to Manufacturing Market Insider (MMI), the top 50 EMS companies worldwide collectively were up a scant 0.4% year-over-year to $344 billion. Our calculations place the Top 10 composite at a higher mark, $365 billion, and the Top 50 at about $430 billion.

This is because CIRCUITS ASSEMBLY has a somewhat different methodology for our rankings. We track calendar year revenue only, except where noted, and use a hard date for currency conversion. MMI accepts fiscal year data, which can mean including sales from 2018, and bases its currency translation on the Federal Reserve average. Also, we don't distinguish between ODMs. In other words, if Foxconn and Jabil make the list, then so too should its major competitors like no. 2 **Pegatron,** no. 3 **Wistron,** no. 4 **Compal** and no. 5 **Quanta.** Each makes millions of end-products for big-name OEMs such as Apple, Dell, Acer, H-P and others. For the same reason, we don't include Qisda (which some may remember by its old name, BenQ), because it sells millions of its own-brand products and doesn't break out ODM sales. We did decide to include no. 14 **Lite-On Technology,** a major vendor of modules for "smart" buildings and cars, solid disk drives, camera modules for phones, and various components. We excluded revenue from its LED and optoelectronics unit. That $4.7 billion figure might still include some non-ODM work, but Lite-On certainly produces more than enough to qualify for the Top 50. Apologies to AllCircuits, which at $405 million would have otherwise made the list.

TABLE 2. The Circuits Assembly Top 50 EMS Companies, 2019

Rank	Company	Nationality	2019 Revenues (US$M)	URL	Notes
1	Foxconn Electronics[1,2]	Taiwan	$149,879	foxconn.com	Enterprise business new driver
2	Pegatron[1]	Taiwan	$45,433	pegatroncorp.com	Smart car dashboard could drive auto electronics sales
3	Quanta[1]	Taiwan	$34,237	quantatw.com	Revenue flat 3 straight years
4	Compal[1]	Taiwan	$32,602	compal.com	Beat out Quanta for Apple's latest Apple Watch
5	Wistron[1]	Taiwan	$29,203	wistron.com	$1B expansion in US, China, Vietnam and India
6	Flex[1,3]	US	$24,901	flextronics.com	Loss of Huawei costs $1B/yr.
7	Inventec[1]	Taiwan	$16,659	inventec.com	PCs make up 80% of sales
8	Jabil Circuit[1]	US	$16,394	jabil.com	Materials unit adds another $9.9B
9	TPV[1,E]	Hong Kong	$8,348	tpv-tech.com	China Electronics Corp. took private in 2019
10	BYD Electronic[1]	China	$7,529	byd-electronic.com.cn	Adding 2 factories in China and 2 in Europe
11	Sanmina[1,4]	US	$6,658	sanmina.com	Betting on optical
12	Celestica[1]	Canada	$5,888	celestica.com	Q1 profits masked 3 straight quarters of losses
13	Universal Scientific Industrial Co. (USI)[1]	Taiwan	$5,282	usi.com.tw	Acquiring Asteelflash in Sept.
14	Lite-On[1,4]	Taiwan	$4,681	liteon.com	Selling SSD unit to Kioxia
15	Venture Corp.[1,5]	Singapore	$3,485	venture.com.sg	New business from medical, life sciences
16	Cal-Comp Electronics[1,6,E]	Thailand	$3,141	calcomp.co.th	Includes $450M from Cal-Comp Philippines
17	Plexus[1]	US	$3,522	plexus.com	Upgraded all its NPI and engineering facilities
18	Benchmark Electronics[1]	US	$2,268	bench.com	80% of sales to come from A&D, medical and semi-cap
19	SIIX[1]	Japan	$2,055	siix.co.jp	Auto electronics sales down 17%
20	Shenzhen Kaifa[1]	China	$1,922	kaifa.cn	5.3M sq. ft. across 9 sites
21	Zollner Elektronik	Germany	$1,697	zollner.de	Investing in I4.0 ops
22	Fabrinet[1]	US	$1,630	fabrinet.com	Can Sanmina dent their optical dominance?
23	Zhen Ding[1]	Taiwan	$1,598	zdtco.com	Acquiring BoardTek Electronics
24	UMC Electronics[1]	Japan	$1,335	umc.co.jp	Hitachi I&T purchase boosted revenue
25	Taiwan Surface Mounting Technology Corp.[1]	Taiwan	$1,261	tsmt.com	Making Nokia phones in India
26	Kimball Electronics[1]	US	$1,253	kimball.com	Will GM strike put brakes on growth?
27	Sumitronics[1]	Japan	$1,200	sumitronics.co.jp	Opened Cambodia factory in December
28	Integrated Micro-electronics Inc. (IMI)[1,7]	Philippines	$1,100	global-imi.com	Automotive softness slowed sales
29	Nippon Mektron[1,E]	Japan	$1,020	nok.co.jp	New 180,000 sq. ft. plant in Vietnam
30	AsteelFlash Group	France	$980	asteelflash.com	About to become the world's largest prototype shop?
31	Kaga Electronics	Japan	$900	taxan.co.jp	13% jump over 2018
32	VTech Communications[1]	Hong Kong	$882	vtechems.com	Expanding in Mayalsia
33	V.S. Industry[1]	Malaysia	$871.3	vs-i.com	Can't make money in China
34	Neo Tech[E]	US	$860	neotech.com	Want to balance A/D, industrial, medical sales at 33% each
35	Pan-International[1]	Taiwan	$851.4	panintl.com	Foxconn subsidiary. Includes connectors, PWBs
36	3CEMS Group (FIC Group)[1]	Taiwan	$818	3cems.com	Includes Prime Base
37	ATA IMS Berhad[1]	Malaysia	$793	ataims.com.my	Nearly 1.5M sq. ft. of factory space in Johor
38	Videoton Holding[E]	Hungary	$640	videoton.hu	New plant in Székesfehérvár
39	Scanfil[1]	Finland	$633.7	scanfil.fi	Acquired Germany's Hasec-Elektronik
40	Hana Microelectronics[1]	Thailand	$623.9	hanagroup.com	Predict 10% rise in profits in 2020
41	Enics[E]	Switzerland	$623.6	enics.com	Pushing ODM power supplies
42	Neways Electronics[1]	the Netherlands	$583.3	neways.nl	Renewed focus on profits
43	Creation Technologies[E]	Canada	$568.1	creationtech.com	Acquired by PE firm Lindsay Goldberg
44	Katolec[E]	Japan	$560.2	katolec.com	EMS is 70% of overall business
45	Wong's International Holdings[1]	Hong Kong	$487.7	wongswih.com	Hurt by US-China trade war
46	SVC Public Co.[1]	Thailand	$457.9	svi-hq.com	Going private?
47	Fujikura[1]	Japan	$449	fujikura.co.jp	Flex circuits
48	DBG / Huizhou Daya Bay Guanghong Electronics[1]	China	$448.7	dbg.com.cn	Making 70M cellphones a year
49	KeyTronic EMS[1]	US	$436	keytronic.com	New 133,000 sq. ft. facility in Vietnam
50	Zowee Tech (Shenzhen Zowee)[1]	China	$433.6	zowee.com.cn	Built fully automated mobile phone line

= Largest revenue gainer
= Largest percentage gainer

1. Publicly held.
2. Excludes sales from PWB, connectors, Sharp, Innolux, etc.
3. Excludes $50 million in PWB sales.
4. EMS only.
5. Includes Univac Precision.
6. Includes $200M from Prime Base.
7. Excludes $203M from Via Optronics.

E = Estimated.

M&A. Lincoln International, the investment bank advisor, tracked 29 EMS transactions in 2019, down from 31 in 2018. There are always several private deals that fly under the radar, especially in Asia, so in all likelihood the actual total was at least twice that.

At least four major transactions were consummated in 2019. Interestingly, none involved companies going public.

Two took place in North America. In one, no. 43 **Creation Technologies** exchanged hands in a deal between private equity interests. And erstwhile Top 50 member Nippon Manufacturing acquired Sony's manufacturing business in the US and Mexico at the end of March 2019.

In Europe, Denmark-based GPV purchased CCS Group, headquartered in Switzerland. That provided a major revenue jolt – about $179 million – bringing the merged entity to an estimated $381 million in 2019.

The biggest deal was also the quietest one. No. 9 **TPV Technology** was taken private in October in a deal worth $1.15 billion. Prior to the friendly takeover, TPV was majority-owned by China Electronics Corp. and a pair of its subsidiaries. CEC teamed with Mitsui & Co. for the transaction, made even more interesting because the former is owned by the Chinese government and the latter is a venerable Japanese conglomerate. (Talk about strange bedfellows.)

While the buyout won "M&A Deal of the Year" at the Asian Legal Business Hong Kong Law Awards, it made nary a ripple in Western media.

One deal consummated in 2018 between two mid-tier players failed to pay off in the rankings. SMTC completed its integration of MC Assembly, which it acquired in November 2018, but the merged entity fell short of its revenue forecast and is unranked here.

One other deal, announced in December but still pending as of this writing, will have repercussions for years to come. No. 13 **Universal Scientific Industrial** agreed to acquire no. 30 **Asteelflash** for $450 million in cash and stock. After that deal closes – it is scheduled to be completed by September, subject to approval by the governments of China, the US and the European Union – Asteelflash will become a subsidiary of USI (which also goes by the Chinese name of Huanxu Electronics). The merged entity will have annual sales of roughly $6.2 billion.

Change is coming. We haven't seen dramatic change to the CA Top 50 the past few years. A few Chinese companies have elbowed their way into the rankings, but for the most part the industry has experienced organic growth coupled with strategic acquisitions. We sense that over the next decade that will change. India's population is only 60 million or so behind China, and is set to take over the top spot by 2027. That massive consumer market is fueling what has become the world's fifth-largest in GDP and third-largest by purchasing power. According to the *Economic Times*, five years ago India had but two mobile manufacturing companies. Now, it boasts 268. Government-backed efforts to breathe life into the domestic manufacturing base, especially in the key mobile and semiconductor markets, will in all likelihood boost at least a few heretofore unknown EMS firms into the rankings, perhaps even to lofty spots.

Western players: You've been warned.

As always, any errors are those of the author's. ▫

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TABLE 3. Top 50 Entrants by Nation

Canada	2
China	4
Finland	1
France	1
Germany	1
Hong Kong	3
Hungary	1
Japan	7
Malaysia	2
the Netherlands	1
Philippines	1
Singapore	1
Switzerland	1
Taiwan	12
Thailand	3
US	9

How to Build a Batch of 12-Layer PCBs in 72 Hours

An hour-by-hour look at the quickturn fabrication process.

WE WERE PRESENTED with a challenge: Is it possible to build 10 prototype 12-layer boards in 72 hours? It wasn't a rhetorical question; a customer really wanted just such an order. So, with time at a premium, our engineers put their heads together and created a "plan of attack" that optimized all resources. One key to success is performing a number of the steps in sequence as needed, so panels are ready when they are required. We'll describe the procedure hour-by-hour as follows:

Hour 1: The CAM operator runs a DRC (design rule check) process and accepts or rejects the data files. If a problem exists, they contact the buyer to work out a solution; e.g., if two traces are too close, and one needs to be moved. Once the data file is accepted, the next action is to set up the innerlayers.

Hour 3: The innerlayer part of the multilayer in CAM is set up first. This will start the process before procedures like drilling or solder mask, which are not required yet. The CAM operator will scale up the innerlayers, so after etching they are all the same size. Since the innerlayers contain different dimensions of copper area, the copper and initial lamination procedure locks in stresses. Once the copper is etched off, the laminate is free to relax and stretch back, changing the size of the panel. Between the smallest change – i.e., a double-sided copper full ground plane and an innerlayer with only a few thin traces – there can be up to 18 mils of length difference between innerlayer panels over 24" to account for. Once panelizing and processing the data for the innerlayers is finished, the CAM operator is free to work on the rest of the manufacturing package, while the innerlayers are processed.

Hour 5: The thin innerlayer laminate is removed from stock, tooling holes punched, the panels cleaned and dry-film laminated.

Hour 7: After imaging, the panels are developed and etched. If the PCB facility has an LDI, the files will be ready by the time the innerlayer panels arrive dry-filmed. If not, the photoplotter will be plotting the innerlayers during hours 2 and 3, so they will be ready when the innerlayer panels arrive for imaging.

Hour 8: Once an AOI (automatic optical inspection) unit inspects the innerlayers, they are punched with the optical lamination pinholes. This ensures the innerlayers are properly registered (line up) with each other in the press.

Hour 10: The innerlayers head to hot press lamination for layup in a press book for lamination.

Hour 11: The actual hot press lamination and cooldown runs for 5 to 6 hr. In the meantime, the CAM operator completes the rest of the images and creates solder mask and white marking programs. The CAM operator also creates a drill-and-route program and finally an electrical test software routine or program.

Hour 18: The panels are removed from the cooldown press; the edges are trimmed, and the panel is sent to the x-ray alignment drill. This machine looks inside the panel and chooses the best location for the drill tooling holes and adjusts the drilling software to the size of the panel.

Hour 20: Due to heat, the process of lamination changes the overall dimensions of the panel by as much as 15 mils. This needs to be measured and adjusted. The x-ray alignment machine will send a file with each panel to the drill to change its program size to more accurately hit the centers of the innerlayer pads.

Hour 22: Boards are pinned, attached to the drill bed, centered and the through-holes drilled.

Hour 23: The panels are deburred, cleaned and dried in an oven in preparation for electroless copper application.

Hour 25: The panels are processed on the electroless line or through a conductive polymer spray machine.

Hour 28: The panels head to cleaning and dry-film application.

Hour 30: After dry-film, the image is exposed to UV light using a phototool or shot with an LDI.

Hour 32: After exposure, the panels are run through the developer.

Hour 34: The panels are copper-plated, and a thin layer of tin is applied as an etch resist.

Hour 39: The panels head to dry-film removal and are processed through a copper etcher to remove the outer layer of excess copper that is not protected by the tin coating. The tin is removed in a conveyorized machine.

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Hour 44: Panels undergo AOI. If shorts are present, a laser ablates them.

Hour 48: Once the outer layers are inspected and passed, the panel heads to solder mask, which can be a silkscreen operation or applied by inkjet machines. After exposure and developing, the next stage is solder mask curing, either in an oven or through a UV machine.

Hour 53: The final finish is applied either by ENIG or hot-air-leveled tin.

FIGURE 1. Sequential processing aids quick turns.

Hour 56: The panels are sent to electrical test to be tested for shorts or opens, typically on a flying probe. If required, the coupon is impedance-tested.

Hour 60: Once electrical test is passed, the panels proceed to white marking, either by silkscreen application or inkjet spray to apply the markings.

Hour 62: Each individual PCB is routed, as required.

Hour 64: Quality Control checks the boards for overall size, ensuring hole dimensions are correct and within tolerance and the overall quality of the board and solder mask are acceptable.

Hour 69: The boards are vacuum-packed and boxed, ready to be shipped.

Hour 71: Ten 12-layer PCBs are finished, with one hour to spare. In the meantime, between processes after etching and solder mask, coupons are punched out, and the laboratory cross-sections them and performs tests to ensure no cracking of hole corners and the correct amount of copper plating was applied. The cross-section will also allow inspection of inner-layer alignment. If all is well, the finished boards ship to the customer. ▫

DEFECT OF THE **MONTH**

Solderability Testing Using Simulation

A simple in-process test for determining component wettability.

THIS MONTH WE illustrate solderability testing using simulation. This is basically conducting simple on-the-shop-floor solderability testing to decide whether to use old components. I use paste printed onto glass slides using the paste and stencil from production. I use the same reflow profile for the board design and components in question.

These J-leaded component terminations wet successfully with the solder paste deposits on the glass plate. The paste has reflowed up, wetting the termination on the front face of the lead (**FIGURE 1**). However, look at the edge and the corners of the leads. If the solder paste has not added to the original tin plating, it calls into question the coating and component age. We have recently used this test to look at the compatibility of low-temperature solders on different terminations as well.

This simple in-process test can be used at high and low temperatures to illustrate wetting and is far better than dip-and-look but not as good as wetting balance measurements, which are quantifiable and the industry standard.

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at youtube.com/user/mrbobwillis. ▫

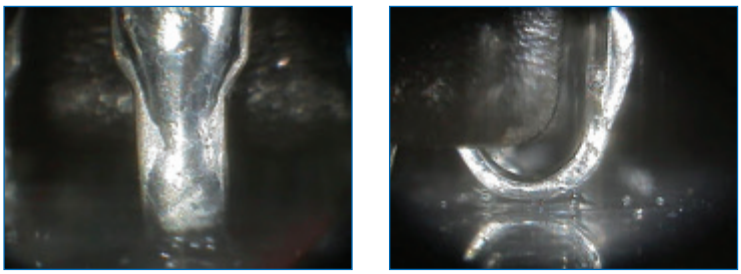

FIGURE 1. J-leaded component showing solder wicking up the lead (left) and at the bottom termination (right).

BOB WILLIS
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Factory Automation is Growing. What Will Workers Do?

How Lean Six Sigma prepares workers for tomorrow's workplace.

PEOPLE OUTSIDE OF manufacturing often imagine that technology's next step is to turn factories entirely over to robots. While factory automation is growing by leaps and bounds, the reality is most automation is paving the way for workers to be far more involved in critical decision-making on the factory floor. Just as Industry 4.0 is the driving force behind smarter machines that automatically analyze and adjust processes as they inspect product, Lean Six Sigma is paving the way for a smarter workforce, capable of analyzing production trends and optimizing processes.

The benefit of Lean manufacturing philosophy is a holistic focus on eliminating issues that create bottlenecks, defects and wasted effort. It aligns well with an Industry 4.0 vision, since greater levels of automation help drive reduced variation, and eliminate excess handling and errors related to manual processing. However, while a Lean vision helps drive efficiency and improve throughput, factories with a lot of product variation, as is found in contract manufacturing, do develop inefficiencies that need to be addressed. Six Sigma provides a powerful methodology and toolbox for addressing these inefficiencies. Implemented correctly, it creates problem-solving discipline that teaches production teams how to make good choices in the problems they choose to solve, thoroughly analyze root cause, test their preferred solution and make sure the improvement is sustainable over time.

The DMAIC (define, measure, analyze, improve, control) methodology represents the heart of this discipline, teaching teams to use a measured process in their problem-solving efforts. The skillsets taught incorporate best practices in management, process engineering and quality.

In the define phase, teams learn to focus on the right issues and lay the groundwork for a disciplined process. The problem statement helps team members align on the core issue they are trying to solve. Building a business case and analyzing the financial impact helps ensure the ends justify the means – in other words, that correcting the issue generates sufficient savings to justify the time spent. Identifying critical to quality (CTQ) elements, defect metrics and voice of the customer (VoC) specifications helps ensure team members focus on analyzing process outcomes meaningful to all stakeholders.

In the measure phase, teams are introduced to a set of core tools that ensure they are collecting meaningful data on the process variances identified in the define phase and drilling down to the variances that impact process outcome. Core tools such as cause-and-effect, Pareto charts, SIPOC (suppliers, inputs, process, outputs, customers) diagrams, capability analyses to assess the ability of a process to meet specifications, and gage R&R measurements enable the team to collect the data necessary to move to the next phase.

In the analyze phase, teams apply critical thinking skills to analyze the data collected to determine trends and possible corrective actions. Tools such as the hypothesis test, cause-and-effect diagrams and IPO charts are used to establish whether the key process outcomes are truly the result of the identified process drivers and inputs. This is expressed as the equation $Y=f(x)$, where Y is the key process outcomes, and x is the variables or drivers within the process.

In the improve phase, teams learn to implement improvements and utilize design of experiments (DoEs) to determine if the proposed solutions correct the problem. For example, in one SigmaTron DMAIC project focused on solder dross reduction, the team made the logical assumption solder dross residue on wave solder pallets was contributing to the dross accumulation issue they wanted to reduce. DoEs established the cleanliness of solder pallets had no impact on accumulation, and as a result, pallets are not being put through an unnecessary added cleaning step.

The control phase drives teams to implement measures that ensure continued achievement of desired metrics, since short-term improvements rarely justify the time spent to develop a DMAIC project.

Generally, those closest to a production process understand what works well and where it could use improvement. However, often these staff don't have the ability to articulate a business case for why process improvements should be initiated. Lean Six Sigma training helps change that when disciplined DMAIC processes are part of the equation. In a world where production teams are increasingly required to focus on continuous metric improvements at a work-cell level, rather than mundane tasks at individual workstations or a machine, Lean Six Sigma training can help production operators evolve into the workers that the highly automated 21st century workplace requires. □

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A Not-So-Hot Tub of Disaster

Can a head in the sand avoid a corpse in the water?

"WE'RE LINE DOWN."

Sorry to hear that. (Not really, but fake empathy makes them feel better.) They got the job as the low bidder. You reap what you sow.

"We've been building this product for five years. That's 22,846 units manufactured successfully and counting."

Congratulations. You just confirmed the adage that one "oh s--t" equals one million "attaboys."

"Not a single electrocuted hot-tubber in that time."

How reassuring. It is of such integral services as these that our gross national product is composed.

"Now we've had three units fry in the space of six weeks. Customer is freaking out. Our bankers are freaking out. Management is freaking out. We are freaking out. We are dead in the water until we get to the bottom of this."

Behold: a freaking mess. Not only is your product failing, perhaps through your own misguided decisions, but you have unforgivably bad taste in metaphors.

"Can we send some of these units to you for failure analysis?"

Sure. What are the symptoms?

"They don't work."

Glad we cleared that up.

"Oh, and they burn up."

Incontrovertible evidence of a problem. Probably not the outdoor barbecue accessory you were looking for. Puts an abrupt end to many a festive garden party.

"Can you x-ray them or even CT scan them?"

Yes to both.

"What images can you provide?"

Magnificent, highly detailed, high-resolution images of a very charred area. Think PCBA moonscape. Chernobylized electronics, double-seared on reentry to Earth's atmosphere.

"You can't find the root cause?"

Don't know. Burning may have carried away the evidence. Combustion does that.

"We need to try. I'll have my buyer contact you to make shipping arrangements."

We're good at trying. How urgent?

"Very. Customer wants to sue us. Three different customers, actually. Class action."

Next morning. The buyer emails and requests an RMA. Reiterates the urgency and informs us she'll be shipping UPS. Ground. From Florida. Key West in fact. Hot tub world headquarters, I guess.

I thought this was urgent. We're in California. A ground shipment from Florida takes a week in the best of times.

"It is urgent. When can you get it back to us?"

When will it arrive?

"I don't know. Maybe a week. Possibly a little more. I'll send you a tracking number, so you can complain if it's late."

Late compared to what? You hired UPS to ship ground. You do the complaining if it's late.

"If it doesn't arrive in two weeks, let me know. Can I get an RMA number?"

No.

"What do you mean, no?"

I meant exactly what I said. RMAs are issued for defective product by the manufacturer. We aren't the manufacturer. We're trying to help you find the source of the defect. So, the answer is no to an RMA.

"We have procedures. We can't ship this without an RMA to reference."

I'd suggest you revise your procedures. Or get an RMA from your manufacturer. And the answer from us is still no.

"Our procedures don't cover this contingency. And our factory is in China."

Clearly, they don't cover. Change is good. Revise the script. Bummer about your supply chain choice. Bet you're feeling like a logistical genius right now. I'm sure they're a Six Sigma producer too. Or used to be.

"How do we ship this defective product to you?"

Put it in a box and ship it.

Click! (Cue elevator music while being put on extended hold.)

"Okay, I spoke with management, and they agreed to waive the RMA requirement."

Wise choice. Bless them.

"They've also decided to waive the standard shipping requirement. Shipping method will be changed from ground to overnight. This is urgent."

Now you're talking.

"We'd like to know exactly how fast you can turn this around?"

Is this an essential product?

"What do you mean?"

Is your product considered an essential medical- or defense-related item?

"It's essential to us. Without shipping on a continuous basis, our cashflow comes to a halt. I'd call that essential."

The federal government would not call that essential. Under current Covid-19 operating conditions, in this state, nonessential activities must be halted altogether, until shelter-in-place restrictions are lifted.

"When can you x-ray our product?"

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On or about April 7, when the restrictions are lifted. Subject to change, of course.

"But it's March 19. April 7 is nearly three weeks away."

Indeed it is. Have you looked around at what is going on right now?

Click! (More hold music. This time the manager who called yesterday returns to the line in an anxiety-infused voice.)

"I must insist you process these units immediately, upon receipt of them tomorrow."

I must insist you read the law. To do this would entail the risk of a fine, imprisonment or both.

"This situation is a hoax, amplified and sensationalized by the news media."

Is that the view from Key West? Tell that to the majority of 40 million Californians who are home right now. Yours truly included. For good measure, tell it to the residents of Lombardy in Northern Italy; and Madrid; and Wuhan. New York City, too. You think we like this, or invented this, or want this? We have businesses to run too. It's one hell of a practical joke if it's a hoax, and no one's laughing. It's an equal-opportunity, non-discriminating hoax, too. The reality is that it's evidence-based, and the evidence is overwhelming. This is not a drill, and it is not fake news. So, I need a better answer from you, or you wait at least until April 7. Maybe longer. *Einverstanden?*

"This is an essential product."

Essential for certain superficial lifestyles. That doesn't match the government's definition.

"This is a fluid flow control device, vital for life support."

I thought it was a pump motor controller for hot tubs.

"That's what we want the world to think. It diverts attention from what we're really doing."

Well, I'm diverted. Now all you need to do is divert me back with a letter from either the government or your OEM stating that this is an essential product or service, warranting ongoing manufacturing during the Covid-19 crisis, and we're, pardon the expression, safe.

"Letter? What letter?"

It's not enough for you to say you're essential. "Saying it" and "being it" are two different things. We need written proof we can show the authorities should we be challenged about the presence of our crew working on your stuff. We keep a file of written authorizations for that very reason. For example, if your work is essential and defense-related, you should have a DPAS (Defense Priorities and Allocations System) rating that indicates certain products you make are essential. Trump invoked DPAS and the Defense Production Act the other day when he asked General Motors to reconfigure an auto assembly plant to produce ventilators for hospitals. You may have a heightened opinion of yourself, but we still need the letter.

"These are essential products. I'm ordering you to inspect them tomorrow when you receive them."

I don't work for you, so orders don't apply.

"Okay, I'm imploring you to inspect them."

Still sounds like a hot tub controller card to me. Show me the letter.

"I'm begging you to inspect them."

We will. You can count on us. On April 7.

Click! (More hold music. Same song. Didn't know the third verse of the "Star Spangled Banner." Covid-19 has provided the opportunity to learn new things.)

Click!

"If we can obtain the letter you request, will you inspect our defective products immediately?"

Yes.

"What are the risks?"

That we don't find anything.

"How will you know if you don't find anything?"

A great big black CT scanning image resembling a crash site in the desert is usually a leading indicator.

"How will you know if you do find something?"

It's usually highlighted in fluorescent yellow with a tag marked "smoking gun" affixed to it. Alternately, the tag sometimes says "issue" if its nature is ambiguous.

"Very funny."

I thought so. What do you think you pay us for?

"Speaking of which, what do you guys charge for CT scanning?"

$500 per hour. Minimum of three hours.

"Any estimate of how long this will take?"

No clue. Any estimate of how much your class action suit will cost you?

"Depends. We have good lawyers. Do you think your analysis will take hours, days, or weeks?"

Depends. We have good technicians. But problems like these are elusive. Sometimes we find them; sometimes we don't. That's the way board forensics works. Sometimes, we detectives are rewarded for our diligence; other times it ends in frustrations. So it goes. You take risks.

"What do you recommend we do?"

Get that letter. Once we have it, buy a block of time. Ten hours. Twenty hours. Whatever. Your choice what you're comfortable with. When we reach the designated limit, we'll stop and contact you. If we've been successful, then we're done. If the trail is cold to that point, we'll make a joint assessment and determine whether to cease activity or scrutinize further. Throughout the process, you will stay informed. You will not be blindsided by a huge, unexpected bill.

Click!

Two days elapsed. Then three. Then five. I had to contact them.

"We elected not to use your services. We consider the failure rate an acceptable risk and a cost of doing business. Many thanks for your help in clarifying our decision-making process. We appreciate your time and will keep you in mind should similar situations arise in the future."

Keep calm and carry on. ❑

EASY-USE OSCILLOSCOPES

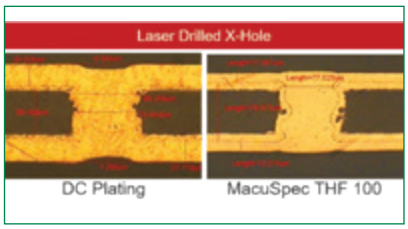
InfiniiVision 1000 X-Series oscilloscopes now have four 2-channel models of 50MHz to 200MHz bandwidth, including a standard decode function for five serial data protocols and remote connection via local area networks and USB. Use same user interface and measurement technology as higher-performance oscilloscopes. Intuitive front panel, now available in 15 languages, features built-in help, including setup tips for complex analysis options.

Keysight Technologies
keysight.com

RIGID/FLEX DEPANELERS

CuttingMaster 2000 and CuttingMaster 3000 handle panels up to 350mm x 350mm or 500mm x 350mm, respectively. Come in standalone or inline configuration with integrated conveyor. High-speed and high-precision linear motor drive system with rigid granite construction. CircuitPro system software.

LPKF Laser & Electronics
lpkf.com



1-STEP CU PLATING

MacuSpec THF 100 electroplating copper through-hole filling process enables improved thermal and structural designs for IC substrates. Copper structure has higher thermal conductivity than paste without thermal expansion. Reportedly faster than DC plating.

MacDermid Alpha Electronics Solutions
macdermidalpha.com

OTHERS OF NOTE

FLEX CIRCUIT ADHESIVE

Pyralux AG all-polyimide double-sided copper-clad laminate comes in sheets and rolls for high-volume consumer, medical and automotive applications. Pyralux GPL adhesive is formulated for high-speed, high-frequency flexible circuits; it has thermal resistance, peel strength and UV laser drilling process capability.

DuPont Interconnect Solutions
dupont.com/electronic-materials.html

PCB STACKUP TOOL

Speedstack online and On-premise libraries now come with additional materials, including ITEQ IT-968SETC core and IT-968SEBS prepreg materials; TUC TU-87P SLK Sp prepregs and TU-872 SLK Sp cores; Isola IS550H prepregs and cores; Arlon 35N, 85HP and 85N cores; and Shengyi Autolad1 cores and Autolad1B prepreg.

Polar Instruments
polarinstruments.com

SHUNT RESISTORS

GMR50 resistors deliver 4W rated power (at electrode temp. TK = 90°C) in 5.0mm x 2.5mm size. Are for current detection in motors and power supply circuits used in automotive systems and industrial equipment. Combine revised electrode structure with device design that improves heat dissipation to PCB where resistor is mounted.

Rohm Semiconductor
rohmsemiconductor.com

LABEL PRINTER APPLICATOR

BradyPrinter A8500 automates PCB labeling for traceability. Prints and applies labels from polyimide auto-apply label range that resist PCB production process. Prints and applies 4mm x 3.18mm labels in 600dpi on PCBs. Can be installed anywhere along production line; can receive label data from most company ERP-systems. Offers industry 4.0 connectivity and is OPC UA ready.

Brady
bradyid.com

'ALL-MATERIAL' DIRECT METALLIZATION

Onyx direct metallization system is for high-reliability and complex PCBs. Is used in horizontal conveyorized equipment or in vertical immersion mode. Can process array of resin materials, including PTFE, polyimide, BT, flex, and epoxy-based resin systems. Is alternative to electroless copper deposition. Reduces water consumption to 4-6 gal./min. Contains no chelator.

RBP Chemical Technology
rbpchemical.com

RSE TEST SYSTEM

R&S TS8996 measures radiated spurious emissions from 5G components in frequency ranges FR1 and FR2. R&S Elektra EMC test software has been upgraded with measurement and calibration routines for 5G. Covers entire 5G FR1 and FR2 frequency ranges for radiated spurious emission measurements.

Rohde & Schwarz
rohde-schwarz.com

HIGH-SPEED 3-D AOI

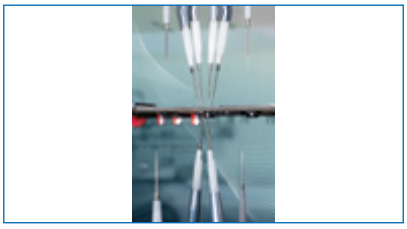
TR7700Q SII comes with optical system that reportedly increases stability and speed up to 25% compared to previous model. Has higher accuracy gauge R&R with stop-and-go imaging technology. Is said to be capable of 1µm optical resolution.

Test Research Inc.
tri.com.tw/en

0201 THERMAL TWEEZER

MT-200 MiniTweez is designed to rework tightly spaced micro-components such as 0201s, 0402s and 0603s. Multi-axis tip alignment capability. Tip-gap adjustment wheel matches gaps between the tips to the work.

Pace Worldwide
paceworldwide.com



NET-BASED ICT SETUP

Net Signal Wave (NSW) enables flying probe testing of PCBAs for large or small and single- or double-sided PCBs. Creates net-based test program where each net in a board is characterized and a signature is learned for each. During test, production boards are compared against signature for each net. Effective for large-area, densely populated PCBAs with many nets. A large-area PCBA with 11,853 total nets, 15,534 total components, and 58,137 standard electrical test steps was tested in fewer than 10 min.

Takaya
texmac.com/takaya

OTHERS OF NOTE

'NO TOOLING' BOARD HANDLING

2segment permits inline selective soldering without boards being panelized or tooled. Comes with dual fluxers and dual solder pots and can solder two singulated boards in parallel mode in line with conveyor direction. Solders two PCBs at the same time without need for boards to be in a panel or palletized.

Nordson Select
nordsonselect.com

SQUEEGEE ASSEMBLY

A new advanced holder assembly for SJ Innotec SMT printers incorporates Soft-Touch 4th gen. paste retainers, a lightweight squeegee holder body and Permalex edge metal squeegee.

Transition Automation
transitionautomation.com

ELECTRICAL MEASUREMENT TOOL

ST-5S Smart Tweezers are for on-board inductance, capacitance, and resistance measurements and testing of SMDs and troubleshooting PCBs. Combine gold-plated tweezers and digital LCR meter. Automatically detect L, C, or R measurements and select correct measurement range and test frequency. OLED display shows component type, value, and component analysis, such as Z and ESR.

Saelig
saelig.com

PB-FREE SELECTIVE SOLDER WIRE

Delta 99C is an SnCuNiGe alloy for Pb-free soldering. Is said to be a drop-in replacement for leaded solder. Contains no silver or bismuth. Melting range is 441°F (227°C). Meets J-STD-006C and RoHS compliant specifications. Comes in 8lb. spool, in diameters of 0.79" (2.01mm) or 0.092" (2.33mm).

Qualitek
qualitek.com

BIG-BOARD AOI

PowerSpector GTAz inline AOI series now comes in three longboard models and up to nine cameras: one top and eight side cameras. 350L handles PCBs up to 350mm x 250mm, 650L handles up to 650mm x 550mm, and 800L handles up to 800mm x 550mm. Inspects PTH components with a top clearance of 60mm. Side cameras offer larger field of view and 20µm resolution. For 2-D and first-article inspection.

MEK (Marantz Electronics)
marantz-electronics.com

THERMAL-RESISTANT COATINGS

Berquist microTIM mTIM 1000 durable, thermally conductive thin-film coatings enhance thermal performance between module and heatsink. Reduce operating temp. at a rate of 0.33°C per watt. Resistant to salt corrosion, abrasion and vibration, and compatible with service temp. from -40° to +200°C.

Henkel
henkel-adhesives.com

In Case You Missed It

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

3-D Printing

"Charge-Programmed Three-Dimensional Printing for Multi-Material Electronic Devices"

Authors: Ryan Hensleigh, Huachen Cui, Zhenpeng Xu, Jeffrey Massman, Desheng Yao, John Berrigan and Xiaoyu Zheng

Abstract: The authors report a 3-D printing approach that can volumetrically deposit multiple functional materials within arbitrary 3-D layouts to create electronic devices in a single step. The approach prints 3-D structures with a programmable mosaic of distinct surface charge regions, creating a platform to deposit functional materials into complex architectures based on localized electrostatic attraction. The technique allows selective volumetric depositions of single metals and diverse active material combinations, including ceramic, semiconducting, magnetic and colloidal materials, into site-specific 3-D topologies. To illustrate the capabilities of this approach, the authors fabricate devices with 3-D electronic interfaces that can be used for tactile sensing, internal wave mapping and shape self-sensing. (*Nature Electronics,* Apr. 6, 2020; nature.com/articles/s41928-020-0391-2)

Stretchable Electronics

"Robust and High-Performance Electrodes via Crumpled Au-CNT Forests for Stretchable Supercapacitors"

Authors: Yihao Zhou, Changyong Cao, Yunteng Cao, Qiwei Han, Charles B. Parker and Jeffrey T. Glass

Abstract: Stretchable supercapacitors based on vertically aligned nanotubes or nanowires have attracted considerable attention because of their improved robustness and electrochemical performance under large and repeated deformations. Here, the authors demonstrate a robust and high-performance stretchable electrode based on crumpled Au-coated carbon nanotube forest (Au-CNT forest). Experimental measurements show the resistance of the Au-CNT forest electrode is around one order magnitude lower than that of a pure CNT forest electrode. The biaxially crumpled Au-CNT forest electrode demonstrates nearly identical electrochemical performance at different measured charge/discharge rates under different strain conditions (i.e., from 0% to 800% area strain). The as-prepared symmetric supercapacitor demonstrates a maximum specific capacitance of ~6mF cm^{-2} at the current density of 40mA cm^{-2} under large strains, exhibiting superior mechanical and electrochemical stability. This research presents a facile process to fabricate highly stretchable supercapacitors based on vertically aligned nanotubes or nanowires for achieving exceptional and robust electrochemical performance. (*Matter,* Mar. 19, 2020, cell.com/matter/fulltext/S2590-2385(20)30113-2)

Thermal Management

"Reversible Spin Storage in Metal Oxide – Fullerene Heterojunctions"

Authors: Timothy Moorsom, *et al.*

Abstract: The authors show that hybrid MnOx/C60 heterojunctions can be used to design a storage device for spin-polarized charge: a spin capacitor. Hybridization at the carbon-metal oxide interface leads to spin-polarized charge trapping after an applied voltage or photocurrent. Strong electronic structure changes, including a 1-eV energy shift and spin polarization in the C60 lowest unoccupied molecular orbital, are then revealed by x-ray absorption spectroscopy, in agreement with density functional theory simulations. Muon spin spectroscopy measurements give further independent evidence of local spin ordering and magnetic moments optically/electronically stored at the heterojunctions. These spin-polarized states dissipate when shorting the electrodes. The spin storage decay time is controlled by magnetic ordering at the interface, leading to coherence times of seconds to hours even at room temperature. (*Science Advances,* Mar. 20, 2020, https://advances.sciencemag.org/content/6/12/eaax1085)

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YOUR PARTNER IN SOLDER ASSEMBLY MATERIALS

AIM's worldwide technical support network of IPC certified engineers assists customers in obtaining optimal results in local time and local language.

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AIM Global Solder Solutions

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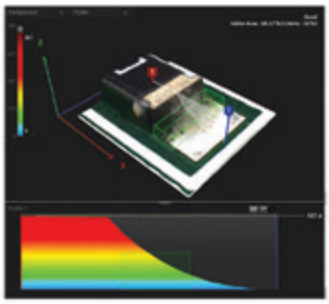
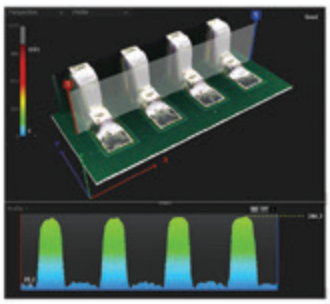
MIRTEC

Spectra-Tech
MANUFACTURING, INC.

"Spectra-Tech continuously invests in the latest technology to provide the highest level of accuracy and quality of assembled products. As part of our commitment to continuous quality improvement, Spectra-Tech recently acquired a total of five (5) new MIRTEC MV-6 OMNI 3D AOI systems. After evaluating several leading 3D AOI vendors, we selected MIRTEC as the best solution to meet our ongoing quality initiatives. Our MIRTEC MV-6 OMNI AOI machines have performed extremely well! The defect detection capability has proven to be outstanding for both SMT and Through-Hole inspection. We are equally pleased with the level of customer service and after sales support."- Craig Wilson, Vice President of Spectra-Tech





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