UP Media Group

Lee Ritchey: Stackup and Design Rules for 4-Layer PCBs

PRINTED CIRCUIT DESIGN & FAB

CIRCUITS ASSEMBLY

pcdandf.com
circuitsassembly.com
July 2020

What Makes **Differential Signals** Different?

Fighting **Crosstalk**

Lights-Out Manufacturing Communication

Dedicated **Work Cells:** Are They Worth It?

LCR-Reader.com

SIBORG SYSTEMS INC

Universal Digital Multimeter / Oscilloscope

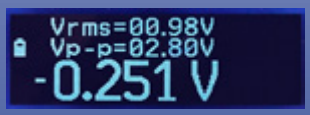
Ultimate PCB Troubleshooting Tool

LCR-Reader-MPA®

LCR and ESR Measurements

Oscilloscope Mode

Signal Generator



Voltage Measurements

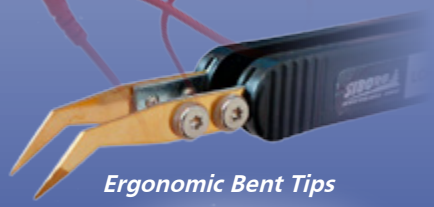
Frequency Measurements

Current Measurements

Summary of Features

- L-C-R-ESR and LED/Diode Measurements
- AC/DC Voltage/Current Measurements
- Frequency, Pulse Period, Duty Cycle Meter
- Oscilloscope, Signal Generator
- NIST Traceable Calibration Certificate
- Open/Short Calibration
- Component Sorting
- Super Cap Testing
- Optional Bluetooth Module

LCR-Reader with Kelvin Probe Connector



Ergonomic Bent Tips

Coil Ring Tester

Technical Specifications

Basic Accuracy	0.1%
Test Frequency	100 Hz - 100 kHz
Test Signal Level	0.1, 0.5, 1.0 Vrms

Measurement Ranges

Resistance R:	5 mΩ to 20 MΩ
Capacitance C:	0.1 pF to 1 F
Inductance L:	1 nH to 100 H

Physical Specifications

Size:	18 x 3 x 1.6 cm
Weight:	1.35 oz.
Battery:	3.7V LiPo

Optional Bluetooth Enabled

- Bluetooth Low Energy connectivity
- Real Time data recording
- Microsoft Windows support

Siborg Systems Inc.
24 Combermere Crescent, Waterloo, Ontario, Canada N2L 5B1
Phone: 1-519-888-9906 Fax: 1-519-725-9522

www.siborg.com

Thin Lamination Board
TLB

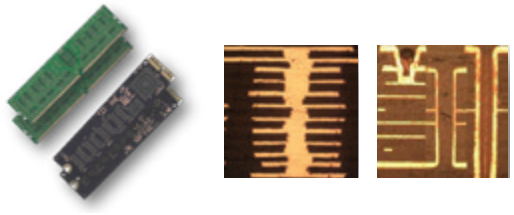
TLB, a global leader in the 4th industrial revolution.

TRUST 2030

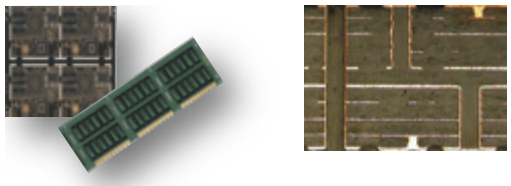
Good Company in 20 Years,
Great Company in 30 Years.

TLB is specialized in manufacturing PCB for semiconductors. By joining World Class 300 in 2018, we have become a company specializing in materials and components leading the fourth industrial revolution. Based on technology and quality, we will establish ourselves as a material parts company that leads not only Korea PCB but also world PCB.

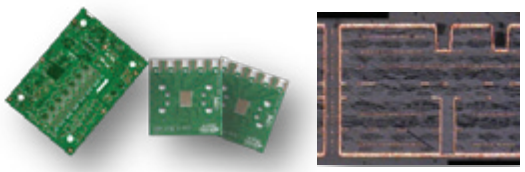
DRAM Module / SSD Module



IOT / Build-up Board



Semiconductor TEST B'd & 5G Network System



TLB CO., LTD.

15602) 305, Sinwon-ro, Danwon-gu, Ansan-si, Gyeonggi-do 16BL 17LT **Tel.** 031-8040-2096 **Fax.** 031-492-6623
Domestic Tel. 031-8040-2071, **E-Mail.** cmh@tlbpcb.com **Offshore Tel.** 031-8040-2060, **E-Mail.** will_shin@tlbpcb.com

TIME TO MODERNIZE YOUR FACTORY

Lowest Prices Ever on Yamaha Machines!

YCP10
Printer

YSM10
Mounter

YSi-V 3D
AOI

Now is the Time! Modernize and meet the new challenges of the manufacturing world with top-quality YAMAHA SMT assembly machines at the lowest prices ever.

- Upgrade to a full featured YSM10 Series Mounter with feeders and programming software for **less than the price of a similarly equipped used machine!**
- Bundle your mounter with a YCP10 Printer and a YSi-V 3D AOI for a complete production line at a fraction of the cost!
- See it all without leaving your office, through full streaming, remote demonstrations.
- "Application Only" lease options start at **less than $2,000/month.****

** 5 Year, $1 Buyout Lease Example for a YSM10 Introductory package, subject to credit approval

Learn more at www.yamaha-motor-im.com

Promotion available in the Americas for a limited time only. For inquiries and further details on this promotion, please contact your local representative or Yamaha directly at info-yima@yamaha-motor.com or (770) 420-5825.

YAMAHA
Revs Your Heart®

JULY 2020 • VOL. 37 • NO. 7

PRINTED CIRCUIT DESIGN & FAB CIRCUITS ASSEMBLY

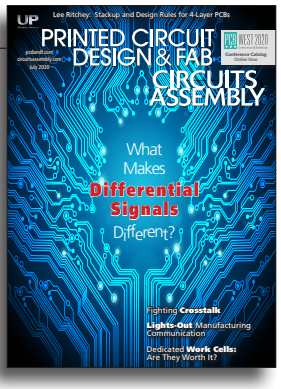
FIRST PERSON

MONEY MATTERS

TECH TALK

DEPARTMENTS

FEATURES



IN THE DIGITAL EDITION

ON PCB CHAT (pcbchat.com)

PCB Chat

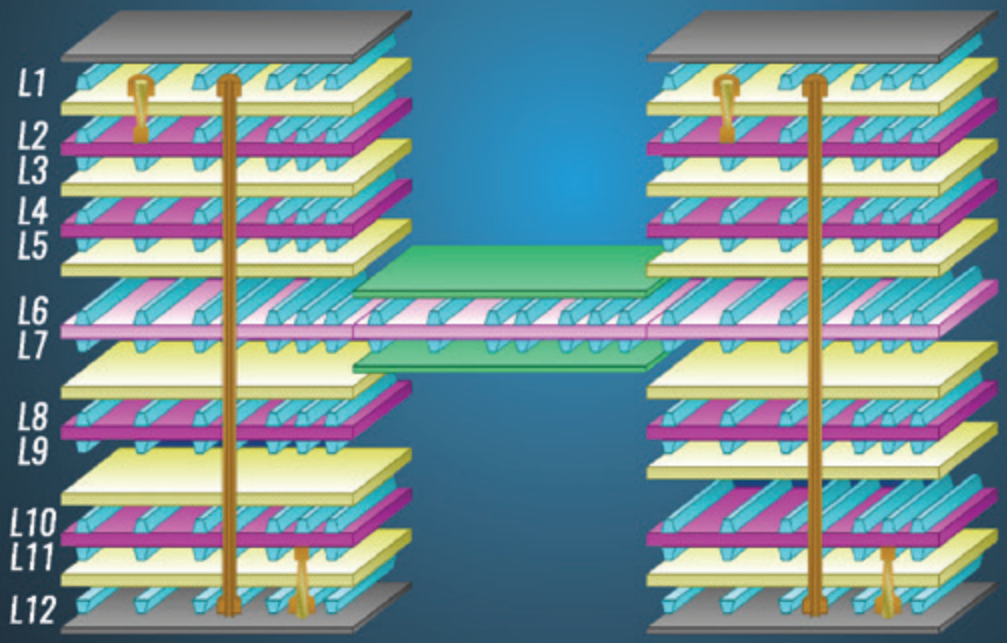
POSTMASTER: Send address changes to
PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY, PO Box 470, Canton, GA 30169

RUSHPCB

20 YEARS OF MANUFACTURING EXPERIENCE WITH BLIND AND BURIED VIAS, RIGID FLEX & FLEX PCB ELECTRONIC DESIGN, & QUICK TURN CIRCUIT BOARDS, ASSEMBLY & FULL TURNKEY

Multilayer PCB Stackup

12 Layer Flex Rigid, 0.030" Thick Rigid, 0.008" Thick Flex
Blind Via L1-L2 & L11-L12, 0.003" Hole, Resin Filled,
0.002"/0.002" Trace/Space, Controlled Impedance



Manufactured on August 2016

When you're in a rush call RUSH PCB

Affordable Pricing ★ Satisfaction Guarantee ★ Fast Response ★ Free Quote ★ Fast Shipping
HDI Boards ★ Stacked Micro Vias ★ 2 mil line & Space ★ Flex & Rigid Flex

Located in the Silicon Valley
PCB up to 12 Layers in 3 days
PCB Assembly Same Day Turn
Full Turnkey Service

Certified: ISO9001/ITAR/UL

www.rushpcb.com | Sales@rushpcb.com | 1 408 496 6013
Rush PCB Inc, 2149-20 O'Toole Ave, San Jose, CA 95131, U.S.A

PRINTED CIRCUIT DESIGN & FAB

pcdandf.com

circuitsassembly.com

CIRCUITS ASSEMBLY

PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is distributed without charge to qualified subscribers. For others, annual Subscription Rates in U.S. funds are: $80 (U.S. and Canada), $145 (all other countries). Single copy price is $8.50. All subscription and single copy orders or inquiries should be directed to PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY, PO Box 470 Canton, GA 30169, email subscriptions@upmediagroup.com. Photocopies and issues on Microfilm/Microfiche (16mm, 33mm or 105mm) are available from University Microfilms International, 300 N. Zeeb Rd., Ann Arbor, MI 48106, Telephone 313-761-4600.

PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is published monthly by UP Media Group Inc., PO Box 470 Canton, GA 30169. ISSN 1939-5442. GST 124513185/ Agreement #1419617.

Periodicals postage paid at Canton/Ball Ground, GA, and additional mailing offices.

Postmaster: Send address changes to PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY, PO Box 470 Canton, GA 30169.

semi

Registration is Now Open

SEMICON® WEST 50 YEARS

JULY 20-23, 2020
VIRTUAL EVENT

Yes, you heard it right, SEMICON West 2020 is going virtual!

Join us online for LIVE and On-Demand programs from the comfort of your home or work office using any mode of connection through your laptop, desktop, tablet, or mobile device. You'll have four days of programs on electronics manufacturing and design topics presented by experts and driven by technology and innovation.

Accessible On-Demand 24/7 through Sept. 20

EXPERIENCE LIVE KEYNOTES

- **Al Gore**, Former United States Vice President
- **Gary Dickerson**, Applied Materials
- **John E. Kelly III**, IBM Research
- **Tetsuro Higashi**, Tokyo Electron
- **Steve Brown**, The Innovation Ultimatum
- **Lea Gabrielle**, Global Engagement Center U.S. State Department
- Plus many more

PROGRAMS

- Bulls & Bears
- SEMI Market Symposium
- Test Vision Symposium
- imec
- SOI Industry Consortium
- SEMICON Southeast Asia
- Diversity & Inclusion
- TechTALKS
- SMART Pavilions

PLATINUM SPONSORS

APPLIED MATERIALS. make possible

Deloitte.

KLA

TEL

Get your All-In Pass for access to all the LIVE and On-Demand program content and more!

#SEMICONWest

@SEMIAmericas

www.SEMICONWest.org

MIKE BUETOW
EDITOR-IN-CHIEF

Bench Gets Vertical

HOW MANY GREENFIELD fabrication plants do you think have been built in the US in the past 10 years?

I can think of three, and two of them were designed and built by the same person and corporate parent. There's Whelen Engineering, the OEM that opened a captive shop in 2015. The brains behind that, Alex Stępiński, then designed and built GreenSource Fabrication, which launched in 2018. And perhaps we can count TTM's new plant in Chippewa Falls, built in a converted 20-year-old, 40,000-sq. ft. warehouse and officially opened last winter.

Now we can add one more to the list. More surprising, an EMS company built it.

Last month Benchmark Electronics opened the doors to its 122,000 sq. ft. state-of-the-art factory in Phoenix. The company, the fifth largest EMS in the US and 18th in the world according to the CIRCUITS ASSEMBLY Top 50, is known for putting components on boards, not making the substrates themselves. The new venture is a leap of faith, buoyed by the desire to control the product development from end to end.

"One of the elements that we recognize (customers) want to control is the ability to design, develop and locally fabricate high-performance circuits and interconnects here in the US," said Daniel Everitt, vice president, Benchmark Lark Technology, the company's RF and high-speed electronics unit.

Benchmark Lark appears loosely modeled after Jabil's successful Blue Sky centers, a foray merging advanced materials and assembly technology into a collaborative unit capable of highly integrated design through end-product development. What Jabil lacks, however, is internal fabrication capability. There, Benchmark has reimagined the vertically integrated manufacturer. Benchmark Lark's high-end target is RF systems that perform up to 110GHz and 3-D heterogeneous integrated (3DHI) circuit boards, all designed, built and tested under one roof. Benchmark Lark put in an MSAP line and can build 1 mil (25µm) lines and spaces with its laser-direct imager (LDI). The technology investment is there.

Everitt says the fab shop gives Benchmark "the opportunity to eliminate superfluous packaging, achieve high-reliability designs and performance for our customers, as well as mixed technologies where we mix an SMT and microelectronics assembly to create a hybrid module, which is commonly used in space, military and defense applications for the most highly demanding scenarios, as well as the highest reliability scenarios."

He adds that the fully vertically integrated design center, which extends from concept to prototype product development to volume production, features a custom-built state-of-the-art factory 4.0 lights-out SMT line.

I have several questions I was unable to get answered prior to the deadline for this month's issue: When was the decision made to add a fab line? How does the plant manage the water requirements and environmental regulations? Is it closed-loop? What drove the decision to implement MSAP vs. other plating processes? Will the bare boards be sold to other EMS or strictly as part of a "package" that includes EMS and other services (design, box build, etc.)? Will Benchmark fab boards it did not design? And that's just the start. Readers should check back to our website for the follow-up.

For many, the driving factor to onshore product is lead time and protection of intellectual property. Yet, while the US may want to reshore, what is left to bring back? Domestic companies no longer have large offshore holdings. MFlex is in Chinese hands. So is Multek. TTM's Mobility unit has been sold. Sanmina has plants in Wuxi and Singapore. TTM still has some six Chinese fab operations, and Amphenol has smaller plants in China and the UK. Several smaller companies have sister plants in India, but the cumulative value of those "imports" is perhaps $400 million. Measured against the worldwide figure of roughly $70 billion, that's a rounding error.

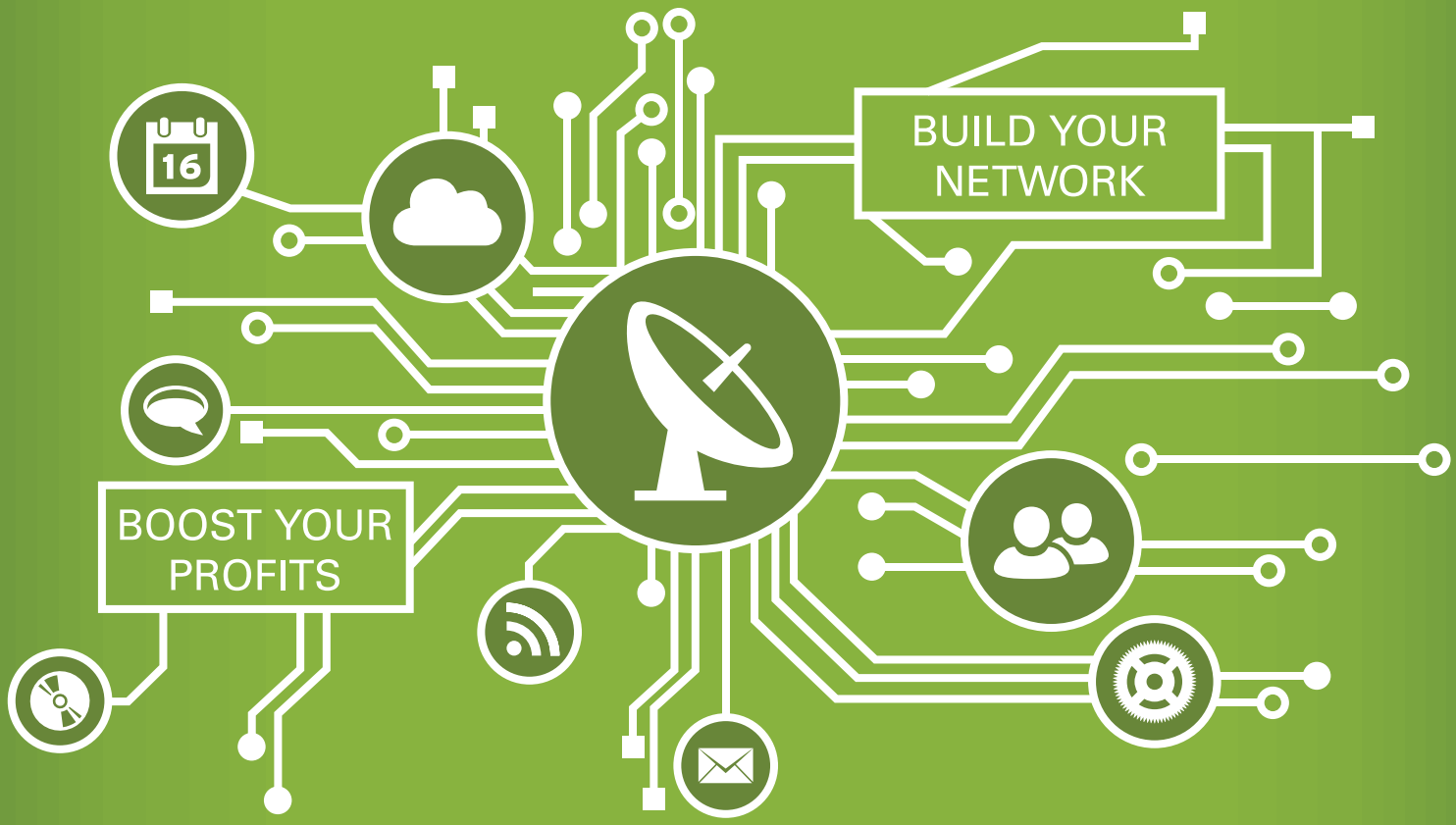
I am not suggesting a mass move to vertical integration is imminent. In fact, I see more movement the other direction. Foxconn spun out its fabrication operations. Flex shed its rigid board unit. Sanmina's bare board sales drop almost every year. Benchmark is going firmly against the grain.

It's audacious. But I like it.

mbuetow@upmediagroup.com
@mikebuetow

P.S. Thanks to Rick Hartley for his two-hour webinar on IoT PCB Design and Layout. As Rick notes, the market is set to explode with billions of devices. You can still view it on-demand at zoom.us/webinar/register/5315907776290/WN_bFuW1oUJQbyZVdLB7_GBjQ, or catch Rick's full-length version at PCB West in September.

The *Circuits Assembly* *Directory of EMS Companies*



- Build your EMS database
- 3,000+ facilities worldwide
- Sortable in Excel
- Unrestricted use
- Includes contact info, no. of lines, markets served and more!

CIRCUITS ASSEMBLY

circuitsassembly.com/dems

PCDF People

AIM Electronics named **Lenny Roach** to engineering sales.

Lenthor Engineering named **Dale Smith** chief technology officer. He has years of hands-on experience in advanced rigid-flex and flex processing technology and techniques, the past five at DuPont.

Mike Flatt, former chairman of Continental Circuits, has passed away at 81.

Ventec named **Socrates Gonis** OEM marketing manager for the US West Coast. He has more than 25 years' experience in electronics, most recently as a sales engineer with Rogers.

PCDF Briefs

KLA formed a new business group from its **ICOS, Orbotech** and **SPTS Technologies** units.

National Instruments signed a definitive agreement to acquire **OptimalPlus,** a global data analytics software company, in a deal valued at $365 million.

Price Circuits installed a **Miva** 2025L Di Trio LDI.

Production has begun at **Schweizer Electronic's** new EUR100 million ($113.4 million) printed circuit board plant in Jiangsu province. The Jintan plant, located about 200km east of Shanghai, has a high level of machine integration and automation, the firm said. Once complete, the Schramberg, Germany-based fabricator's new site will have a capacity of over 7,000 sq. m. per day, roughly five times that of the German plant.

CA People

AIM Solder named **Tim O'Neill** director of product management. He has been with Aim for nearly 23 years in a variety of technical marketing and business development positions.

Apex Tool Group promoted **Bernd Fruehwald** to senior vice president and president of its Global Power Tools business. He joined in 2014 as general manager, Weller Tools and most recently served as vice president and president, EMEA and ANZ.

Essemtec named **Jürg Schüpbach** director of sales.

Flex named **Mike Thoeny** president, Automotive Business Group.

Hensoldt, Nano Dimension 3-D Print 10-Layer PCB

MUNICH – Using a newly developed dielectric polymer ink and conductive ink from Nano Dimension, Hensoldt succeeded in using a 3-D printer to assemble a 10-layer PCB that carries high-performance electronic structures soldered to both outer sides.

"Military sensor solutions require performance and reliability levels far above those of commercial components," said Thomas Müller, CEO, Hensoldt. "To have high-density components quickly available with reduced effort by means of 3-D printing gives us a competitive edge in the development process of such high-end electronic systems."

"Nano Dimension's relationship with Hensoldt is the type of partnership with customers we are striving for," said Yoav Stern, president and CEO, Nano Dimension. "Working together and learning from Hensoldt led us to reach a first-of-its-kind in-depth knowledge of polymer materials applications. Additionally, it guided us in the development of Hi-PEDs (high-performance electronic devices) that create competitive edges by enabling unique implementations with shortest time to market."

Hensoldt has used Nano Dimension's DragonFly 3-D printing system since 2016. Last year, Hensoldt implemented DragonFly Lights-Out Digital Manufacturing printing technology. (CD)

Altium's Latest Cloud Collaboration Platform Links ECAD and MCAD

SAN DIEGO – Two years after it was teased at a series of worldwide seminars with key customers and media, Altium's cloud platform for PCB design has begun to reach the potential the ECAD company promised.

The latest update to Altium 365 now allows collaboration among PCB designers, mechanical designers, part suppliers and manufacturers. And Altium 365 provides a built-in co-designer capability that provides native integration with a trio of MCAD platforms: PTC Creo, Dassault SolidWorks and Autodesk Inventor.

According to Leigh Gawne, chief software architect, 365 provides a "full-on collaboration in that actual PCBs and components can be changed. The MCAD user can place and move an electrical part, define the PCB, and push the (update) to the PCB engineer."

"ECAD has really been confined to a desktop. With Altium 365, we are taking it off the desktop. Anyone with a web browser is now able to view and interact and collaborate on these designs. For those who want to open a schematic and cross-probe to a net on a PCB or a component in a 3-D rendering of the board, it doesn't require this heavyweight software to be installed. For people who want to consume and inspect and interact, this is possible anywhere, on any device, just through a browser."

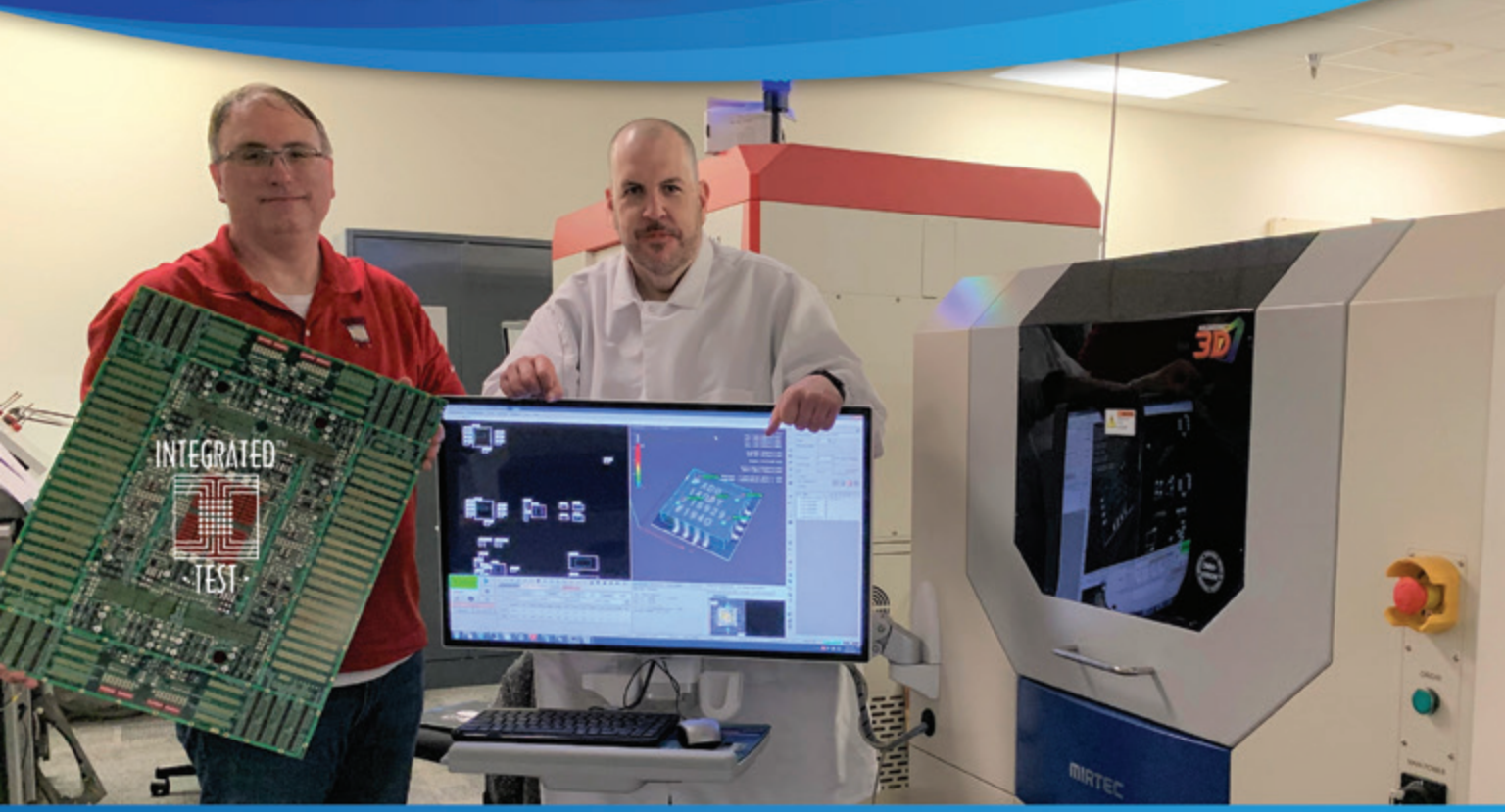
The latest rev leverages one of the great advantages of the cloud: ease of widespread access to a common file. It allows sharing, visualizing, and mark-ups of printed circuit board designs across a wide number of users. The latest version is known as Altium 365 Standard and is available to all subscribers.

What does this mean for the Concord Pro release – Altium's component management environment – from last October? That will become known as Altium 365 Pro, according to Gawne, and subscribers can upgrade from 365 Standard at any time. The distinction is that 365 Standard supports collaboration and sharing, while 365 Pro accesses component data in real-time, including lifecycle status from IHS Markit and pricing and availability from the Altium subsidiary Octopart. The data include "where used" for components, component templates, and parts alternatives.

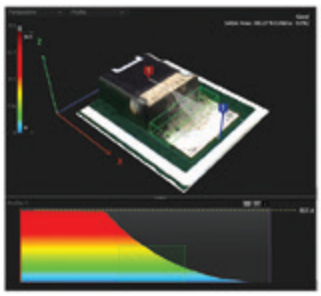
Altium 365 Pro will be synonymous with Concord Pro, Gawne said.

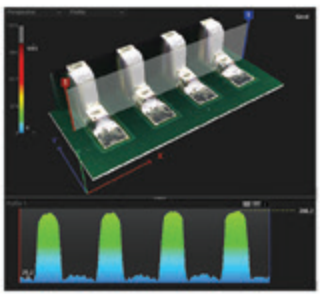
Another advantage, Gawne says, is accessibility. Designs can now be viewed via any internet-enabled device, such as a phone, expediting snap reviews where launching a PC might be cumbersome.

MIRTEC



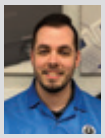
"Operating out of our 39,000 square foot manufacturing facility in Dallas, TX, Integrated Test Corporation offers turn-key design, fabrication and assembly solutions for leading-edge ATE test PCBs. The highly complex nature and size of these PCBs makes the need for Automated Optical Inspection (AOI) an absolute necessity. When we decided to purchase a new 3D AOI machine to fulfill our growing inspection requirements, MIRTEC was the obvious choice. With over 20 years experience in SMT manufacturing, I would highly recommend MIRTEC based on their state-of-the-art 3D Inspection Technology as well as their ease of programming and operation. We have been equally impressed with MIRTEC's fast and effective Technical Support. In the rare moments in which a problem is encountered, MIRTEC's Technical Service Team is lightning quick in both response and resolution." Tom Bruszak – Quality Manager





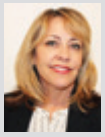
- OMNI-VISION® 3D Inspection Technology
- 15 Mega Pixel CoaXPress Camera Technology
- 10um Telecentric Compound Lens Design
- 10 Mega Pixel SIDE-VIEWER® Camera System
- Eight Phase COLOR Lighting System
- Full 3D Co-Planarity and Solder Fillet Inspection Capability

www.mirtec.com



Libra Industries promoted **Brian Whoric** (pictured) to manager for all production teams in Plant Two. He has worked in the rework department and as hand solder lead during his past 10 years with the company. Libra also promoted **Alex Lindsey** (pictured) to program manager at the company's Richardson, TX, facility, and **Megan Connolly** to supervisor.

Libra Industries added **Mike Dometrovich** to its independent manufacturers' representative team. He has been in the manufacturing industry for more than 36 years.



MicroCare named **Beth Silvia** assistant corporate controller, responsible for management of the company's accounting and finance functions in the United States and all its foreign subsidiaries.

Saki America named **Satoshi Otake** account manager.

Sono-Tek promoted **Robb Engle** to executive vice president.

Synapse named **Mathieu Kury** director of business development. He was previously head of business development at AsteelFlash.

ViTrox appointed **Richard Osborne** sales director, USA.

CA Briefs

Ability Tec has relocated to a new purpose-built EMS facility in Burk, UK.

Actia Electronics installed a **Takaya** APT-1600FD-A flying probe tester.

ALLPCB opened a self-operated SMT factory in Guangde, Anhui Province, China.

Apple is examining a proposal to shift nearly one-fifth of its production capacity from China to India, ramp up its local manufacturing capabilities through its contract manufacturers and achieve $40 billion worth of production over the next five years, *The Economic Times* reported.

Big Ass Fans installed a **Hentec Industries / RPS Automation** Vector 300 selective soldering machine, its third.

CE3 Electronics has selected a **Mirtec** MV-6 Omni 3-D AOI.

Critical Manufacturing appointed **E-tronix** manufacturers' representative in

Altium 365 is functional with the latest version of Altium's PCB design tool, Designer 20, and the previous rev, Designer 19. Valid Altium Designer subscribers have access to the range of features for Altium 365. There is no charge to view a design through the 365 browser, however. (MB)

Siemens Updates Data Exchange Format for Digital Thread

PLANO, TX – Siemens expanded its ODB++ data structure for transferring PCB designs into fabrication, assembly and test with open data formats for the digital thread.

ODB++Process data exchange format, previously known as OPM, helps enable the open exchange of process engineering information between disparate machines, software vendors, and standalone processes.

This free data exchange format helps users transfer machine programs from one machine type to another, such as a target machine from a different vendor or a machine on a different platform. ODB++Process provides the open exchange of process engineering information, which then converts the data for immediate use on any production machine or workstation.

"By using a single assembly format file output like ODB++Process, which standardizes machine package libraries with vShapes across the entire production line, Koh Young is able to minimize program variations between machines like inspection and mounters," said JD Shin, chief sales officer for Koh Young. "The enhanced approach to programming reduces human error and variation and significantly reduces the NPI programming cycle time. What's more, the single file assembly format output like ODB++Process is machine agnostic and easily enables moving production assembly data and process requirements between lines – and more importantly factories across the world."

With ODB++Design supporting full product design data representation, and ODB++Manufacturing, previously known as OML, neutralizing machines' shop floor data, the ODB++Process reportedly completes the open design-through-manufacturing digital thread for electronics.

Each intelligent data exchange module is designed to be neutral and open, supporting all SMT machine vendors and all EDA software providers.

"Siemens is an active member of the IPC, and we will continue to invest in our own data exchange formats to ensure quality and resources are available to the global community," said Dan Hoz, general manager, Valor Division of Siemens Digital Industries Software. "Our focus on multi-domain digitalization solutions will continue to be a critical advantage to our customers, so they can manufacture innovative products with minimal risk and faster time to profit." (CD)

3 Materials Suppliers Awarded US Patent for Solder Alloy

WATERBURY, CT – Three suppliers in electronics assembly materials received notice the US Patent and Trademark Office has issued a patent for their popular lead-free solder alloy formulation. The patent was granted an extended expiration to Jun. 11, 2029.

MacDermid Alpha Electronics Solutions, Henkel and Heraeus developed the Pb-free solder alloy known as Innolot and Loctite 90ISC for harsh environment electronics applications. The alloy is designed to tolerate the demands of high-temperature applications, while being solderable at standard Pb-free process temperatures.

"The issuing of this patent is of strategic and commercial importance," said Tom Hunsinger, vice president of marketing, MacDermid Alpha Electronics Solutions. "Coupled with patent protection in Europe and Japan, this will help drive new business opportunities not only in automotive but in other markets with harsh environment challenges." (CD)

Where Advanced Technology, Highest Quality & Fastest Delivery Are Standard

APCT Offers Printed Circuit Board Solutions from NPI to Mass Production

- Standard to Advanced HDI Technology
- Flex and Rigid Flex Technology
- Complete DFM Support
- Cycle Times Faster Than Industry Standards
- Defense & Aerospace Certifications
- Global Offshore Solutions

  Advantages Include:
  - *Ease of Use*
  - *Seamless Recipe Transfer*
  - *Inventory Management*
  - *Risk Mitigation*

Contact APCT Today 408.727.6442 | APCT.com

Printed Circuit Board Solutions

APCT.com

APCT Santa Clara HQ	APCT Anaheim	APCT Orange County	APCT Wallingford	APCT Global
408.727.6442	714.921.0860	714.993.0270	203.269.3311	203.284.1215

Minnesota, Iowa, North Dakota, South Dakota, Wisconsin, Illinois, and Indiana.

A new report from **Deloitte** asks how the manufacturing industry can prepare for the future workplace and ready its workforce to work beside robots and advanced technologies.

EG Electronics acquired **WEAB Wermlands Elektronik,** an EMS company in Torsby, Sweden.

Huawei says its $123 billion-a-year business is in jeopardy after Washington announced further restrictions on its use of American technology. China's commerce ministry called the measures an abuse of state power and a violation of market principles and says it will take "all necessary measures" in response.

Analysts are skeptical about **Intel's** idea to build a chip foundry in the US.

MicroCare has been acquired by **Capital Partners** in partnership with senior management. COO Tom Tattersall will assume the role of CEO.

Panasonic said that next year it will move its Thai-based production of white goods to Vietnam, laying off some 800 workers.

Phoenix Systems installed a **Unicomp** AX-8200HR x-ray machine.

Pillarhouse appointed **Performance Technologies Group** to spearhead sales in Virginia, West Virginia, Maryland, and Washington, DC.

Rocket EMS added conformal coating services.

SIA expressed concern over the new US export control rule changes.

Southwest Systems Technology entered into a representation agreement with **Thinky** for the states of TX, OK, LA and AR.

SQP International installed a **Boffotto** plasma treatment system.

Taiwan Semiconductor Manufacturing Co. said it will build a $12 billion semiconductor facility in Arizona.

Taiwan-based electronic component makers have come under pressure to move production lines out of China, but claim relocation is not easy because of the high cost incurred.

Tepcomp Group added a new SMT surface mount technology production line to its Turku, Finland, plant.

Universal Instruments' Advanced Process Lab appointed **Technical Marketing Company** channel partner in the Rocky Mountain US.

UL Debuts Supplier Cyber Trustworthiness Rating Program

NORTHBROOK, IL – UL has rolled out a new assessment program to help organizations minimize supply chain cybersecurity risk by focusing on the trustworthiness of suppliers' security practices.

UL Supplier Cyber Trust Level analyzes suppliers' security practices across multiple trust categories, resulting in a documented supplier trust level rating. This rating demonstrates the trustworthiness of a supplier's security practices across the software and hardware development lifecycle, hosted systems, information management systems and their third-party management.

UL Supplier Cyber Trust Level assessment enables a holistic view of supplier's security posture, while providing a consistent evaluation for organizations of the cybersecurity posture from supplier to supplier.

"Cybersecurity for connected technologies is a major risk that impacts manufacturers, service providers, suppliers and end product ecosystems," said Isabelle Noblanc, global vice president and general manager, Identity Management and Security division, UL. "A supplier's security-oriented culture, security processes and practices and secure R&D environments are all critical when validating supplier security. UL understands this significance and continues to help organizations with IoT cybersecurity offerings that address end products, ecosystems and now – with the launch of our Supplier Cyber Trust Level – supply chains."

UL Supplier Cyber Trust Level leverages security controls from many industry best practices, standards and frameworks, including National Institute of Standards and Technology cyber supply chain risk management, European Union Agency for Cybersecurity supply chain attacks, North American Electric Reliability Corp. Critical Infrastructure Protection (CIP)-013-1 standard, International Electrotechnical Commission 20243-1, 62443-4-1 and 62443-2-4 standards and International Organization for Standardization (ISO) 27001 standard.

"The Covid-19 outbreak has made it clear how vulnerable supply chains can be. Although the Covid-19 situation has exposed vulnerability related to the availability of supply chains, it has also raised further awareness that cybersecurity is another prominent threat to supply chains worldwide. The UL Supplier Cyber Trust Level solution will help companies globally to better secure their supply chains and help bring safer products to the market." (CD)

SigmaTron to Merge with Pet Tech OEM

ELK GROVE VILLAGE, IL – SigmaTron and pet tech company Wagz have executed a letter of intent to merge in an all-stock deal. The deal calls for SigmaTron to issue approximately 2.27 million new shares of stock, giving Wagz shareholders approximately one-third of the combined company.

The deal is expected to close by the end of August, subject to a material definitive agreement and SigmaTron's raising of $7.5 million in additional capital that it projects will be needed for the expanded operations.

Upon completion, Wagz will be a standalone operation of SigmaTron.

For the past two years Wagz has outsourced part of its product portfolio to SigmaTron.

"Over the last two years, we have become immersed in the pet tech market with Wagz as our customer," said Gary R. Fairhead, president and CEO, SigmaTron. "We have been impressed with the growth of the pet sector, and data show it is practically recession-proof. Recent reports indicate pet ownership during Covid-19 has increased, accelerating what was already a very strong market. Wagz would benefit from our ability to provide world-class manufacturing services through our global footprint and supply chain, and SigmaTron would benefit from new high-margin recurring revenue." (CD)

METALS INDEX

THE PANDEMIC STRIKES

Trends in the U.S. electronics equipment market (shipments only).	% CHANGE FEB.	MAR.	APR.	YTD%
Computers and electronics products	0.2	-0.7	0.6	1.3
Computers	-2.3	-4.1	-0.5	-12.7
Storage devices	-2.7	0.2	-1.8	61.0
Other peripheral equipment	-2.7	-3.2	0.0	3.1
Nondefense communications equipment	0.2	2.9	-0.3	6.4
Defense communications equipment	4.5	0.4	2.7	-4.7
A/V equipment	-5.6	-8.4	4.6	-18.4
Components[1]	0.7	-0.9	1.8	9.0
Nondefense search and navigation equipment	-1.8	-1.3	-0.3	-5.0
Defense search and navigation equipment	0.0	0.0	0.2	4.0
Medical, measurement and control	0.2	-0.9	-0.7	-3.6

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, June 3, 2020

US MANUFACTURING INDICES

	JAN.	FEB.	MAR.	APR.	MAY
PMI	50.9	50.1	49.1	41.5	43.1
New orders	52.0	49.8	42.2	27.1	31.8
Production	54.3	50.3	47.7	27.5	33.2
Inventories	48.8	46.5	46.9	49.7	50.4
Customer inventories	43.8	41.8	43.4	48.8	46.2
Backlogs	45.7	50.3	45.9	37.8	38.2

Source: Institute for Supply Management, June 1, 2020

KEY COMPONENTS

	DEC.	JAN.	FEB.	MAR.	APR.
Semiconductor equipment billings[1]	17.8%	22.7%	26.6%	20.1%[r]	17.2%[p]
Semiconductors[2]	-5.4%	-0.35%	5%	6.9%[r]	6.1%[p]
PCBs[3] (North America)	1.09	1.05	1.15	1.15	1.19
Computers/electronic products[4]	5.47	5.42	5.41	5.43[r]	5.43[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

Hot Takes

- **The worldwide bare board market** will fall 5 to 6% year-over-year this year. China, the US and some Taiwanese fabricators will beat the market. Fabricator sales in 2019 rose 1.4% to $76 billion worldwide. Excluding sales of assembled boards by fabricators, the bare board market was around $70 billion, and drop to around $66 billion in 2020. (Dr. Hayao Nakahara, N.T. Information)
- **Worldwide sales of passive components** declined 13.7% in dollars and 27.7% in units year-over-year in 2019. (ECIA)
- **Global shipments of PCs, tablets and mobile phones** are on pace to decline 13.6% in 2020, totaling 1.9 billion units. (Gartner)
- **More than half (53%) of electronics industry product launches** have been delayed or cancelled due to the pandemic. (Supplyframe)
- **Electronics manufacturing** directly supports more than 1.3 million US jobs, according to a new IPC report.
- **US imports of electronics** increased 8.4% in 2019.
- **A comprehensive ranking of 100 China-based PCB companies** increased 13.1% year-over-year to RMB237 billion ($33. billion), CPCA said, with Pengding Holdings, Dongshan Precision, Jianding Technology, and Shennan Circuit all topping RMB10 billion ($1.4 billion).
- **The 2020 smartphone shipment forecast** was lowered to 1.15 billion units, down 15.4% from 2019. (Digitimes Research)
- **The global tablet, notebook PC, desktop PC, and workstation market forecast** has been lowered to 361 million units, down 12.4% for the year. (IDC)
- **Global shipments of wearable devices** grew 30% year-over-year during the first quarter to 72.6 million units. (IDC)
- **Global PC and tablet shipments** will fall 7% year-over-year to 367.8 million units in 2020. (Canalys)
- **The worldwide smartphone market** is forecast to decline 11.9% year-over-year in 2020, with shipments totaling 1.2 billion units. (IDC)

Getting the Team Back Together

It's time to work with your employees toward reopening our doors to the world.

AS THE SECOND half of this most extraordinary year unfolds, I keep thinking of all the things I had planned, hoped or expected to accomplish during the first half that now are on the overly long "to do" list. As we try to get back in the proverbial saddle and focus on what we can do within the confines of various local and national government pandemic restrictions and reopening timelines, my priorities are reengaging with employees, customers, suppliers and industry events.

Each industry and company has issues to work through, whether it is bringing back furloughed or terminated staff, or just figuring out whether and how to integrate work-from-home into a long-term employment scenario. In all cases, employee reentry must be dealt with quickly to rebuild the sense of corporate community and possibly build an even greater sense of team.

People by nature want to be with other people. Collaboration requires a good smattering of face-to-face time. While Zoom, GoToMeeting and WebEx will continue to assume a bigger place in the business interaction mix, long-term success requires people being together at least some of the time. While we will reluctantly continue social distancing and wearing face masks at times, corporate management's number one challenge is how to bring the team together and get back to a more normal work environment.

Customers, too, have been neglected, and business needs to find a way to reconnect. Yes, the various communication tools mentioned, as well as the tried-and-true phone calls and emails have kept customers and suppliers in touch, but they do not replace face-to-face meetings where new products are discussed, problems are shared and collaboration best occurs.

The timeline to be able to meet in person will vary depending on locality, but reconnecting is high priority for all businesses. While I fully expect virtual communication tools such as Zoom to be used more than ever, walking a customer's plant, talking to engineers, and seeing the shop floor in person are still the best ways to get a feel for the opportunities and challenges.

For far too long suppliers, the mirror image of customers, have not been able to walk through the plants of customers to discuss new products and better ways to process product. With so much focus on social distancing in the manufacturing environment, it is more important than ever for the direct dialogue on the shop floor, so the best ideas can become the foundation of improvements. A fresh set of eyes, especially when short-staffed companies may have inadvertently let processes lapse or be truncated, has never been needed more.

Industry events, whether local, regional or global, have also been missed. These events are the catalyst for people from different companies and in different segments of industry to discuss common interests and hear the latest thinking, be it related to specific products and processes, or tied to future technology or market directions. Now that a pandemic has caused all businesses to rethink how they operate and deal with events that a few short months earlier would have been considered rote, personal interaction among business leaders is crucial. Industry events of all types have harnessed technology to provide basic information during the pandemic. Personal interaction among colleagues cannot be replaced simply by webinar, however.

With the "to do" list so long, and the uncertainty so pronounced, what to do?

As the Chinese proverb goes, "a journey of a thousand miles begins with a single step." Such is the case in our current times. Coming back from the stay-in-place pandemic mindset will take time and will require patience and flexibility. That first step may well be the most difficult, especially for companies and individuals in densely populated locations. The time is now, however, to think through, plan and put contingencies in place to successfully journey out of the Covid-19 cloud.

National and local governments across the globe may dictate "official" sequences or phases to "reopen" economies. Corporate policy, especially by the world's largest companies, will provide a second layer of signals for when various levels of social mingling may be appropriate. But the real arbiter of how fast we can return to the much-needed business travel and face-to-face interaction will most certainly be up to the individual. Some may want to dive back in immediately; others may want to take a far more conservative approach to stepping back into life as it was. The critical part of each organization's planning and contingency plans is to handle the many concerns individual employees have toward reentering work environments safely, compassionately and effectively.

Bringing the team back together, visiting customers, welcoming suppliers on the shop floor, and attending industry events will clearly seem different than they did six months ago. Having a game plan is necessary, as is flexibility. But the sooner we start to rebound, the more successful we will be. ▫

PETER BIGELOW
is president and CEO of IMI Inc.; pbigelow@imipcb.com. His column appears monthly.

What is Your PCB Pricing Game Plan?

Being ready to pivot offers flexibility and keeps vendors honest.

WHAT IS YOUR company's PCB buying strategy as we emerge from the confines of the Covid-19 pandemic shutdown? Do you have one?

Those responsible for corporate procurement need to understand supplier diversification is the key to remaining competitive in this challenging economy. Yet, many OEMs and EMS companies have invested too much of their annual PCB spend with only one vendor. That could prove to be a costly mistake.

I understand and appreciate vendor loyalty, but are you leveraging your vendor, or are you being leveraged by your vendor?

The truth is companies that stick with this one-vendor approach will have a harder time remaining competitive in the post-pandemic world. "We have used this vendor for years" is *not* a viable strategy.

It's not an excuse to say buyers are overwhelmed with too many other responsibilities. Keeping the vendor base on its toes is a core buyer responsibility. It's the job of upper management to ensure buyers are always working to bring prices down, for both new opportunities *and* existing business.

The PCB makes up eight to 12% of the bill of materials and requires over 100 different processes to manufacture. The pricing for this custom-made item can vary greatly, depending on technology required, as well as the volume and delivery schedule. But it's also subjective, tied to conditions at a particular manufacturing site at a particular time.

That's why PCB buyers should regularly seek offers from other vendors, especially on business already in-house somewhere else. Things change, and buyers should be ready to pivot to less expensive solutions, even for customers who only want to consider domestic suppliers.

Make sure you can offer a list of vetted suppliers, whether they are offshore or domestic. Your customers need to know you're always seeking the best pricing for them.

I understand we are all busy these days and that adding a new vendor to the approved vendor list (AVL) can be time-consuming. Many EMS and OEM companies make the process of moving PCB orders to new vendors too cumbersome. They are hurting themselves.

And the truth is adding qualified suppliers is not as hard as you may think. Here's a summary of how to evaluate a potential vendor:

Get a trial quote. On the buying side, it's all about the price. There's no need to get the quality or production departments involved if the only reason to move a board is for better pricing. Start with a trial quote *after you have an NDA in place* with a potential vendor.

Check references. If the trial quote looks good enough to justify moving an order, proceed to the reference checks. Ask for at least three references, preferably in the same industry. And make sure you actually call those references.

Money matters. If the references are good, it's time to check the vendor's financial stability. Run a D&B report. Call the vendor's bank and suppliers. Make sure they pay their bills. Getting financials from an offshore vendor can be difficult, so in that case, double-up on references instead, and hit harder on questions concerning timely communication and customer service.

Quality concerns. If pricing, financials and references look right, it's time to get quality involved. Make sure your prospective vendor has all the required credentials, such as UL, ISO, and anything specific to your customer's needs. Send out a vendor survey (you have one of those, right?) and create a vendor file.

Talk to production. Production departments are usually averse to change, understandably so. Don't cut your new vendor into the production schedule without involving your production people in the approval process. To help put production at ease, you can issue a contingency purchase order to the vendor (with tooling and test charges waived), with little risk to your company.

Henry Ford said, "Competition is the keen cutting edge of business, always shaving away at costs." That applies to PCB vendor pricing as well. Keep your vendor base on its toes because that lowers costs. You can do that with minimal risk to your manufacturing operation. And that will keep your customers happy. □

GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying; greg@boardbuying.com.

Understanding *High-Speed* Constraints

FREE new e-book!

pcdandf.com/pcdesign/constraints

> This fabulous treatise allows PCB designers and engineers to understand all the important constraints and determine their values.
>
> – *Rick Hartley*

written by

Charles Pfeil

Charles Pfeil has spent over 50 years in the PCB industry as a designer, owner of a service bureau, and in engineering management and product definition roles at Racal-Redac, ASI, Cadence, PADS, VeriBest, Mentor Graphics, and Altium. He was the original product architect of Expedition PCB.

Place and Route: The Art of PCB Design

Lessons learned the hard way.

I STILL REMEMBER a day back in the late '80s when an electrical engineer invited me into his office and showed me a CAD PCB layout on his monitor. How cool would it be to do that? Well, now I know. Pretty cool, but frustrating at times as well. Placing and routing are the meat and potatoes of PCB design. (If you don't like "meat," think of your own metaphor.) There are other things to do, but this is what holds it all together.

The basic framework is built around two disciplines: mechanical and electrical engineering. The two main features are the components and, of course, the board. An intelligent set of library parts is essential to getting the placement off to a good start. Over the years, schematic capture has shifted from the PCB designer's hands to those of the EE.

The schematic and component libraries are often outsourced or created by an in-house specialist. The goal in the larger outfits is to allow the PCB designer to focus on placement and routing. Startups will put more hats on your head. Either way, our time is a precious commodity not to be wasted.

When and where to begin. We start with a board outline and a netlist, both of which should be considered preliminary. Waiting for all the stars to align before beginning the layout is called a waterfall schedule. It's unrealistic to expect that to happen on a complex layout. Expect some churn along the way. Now, I just mentioned our time is precious, but it is worth it to get in early because it leads to a shorter overall schedule. That is the goal; time-to-market is one of the biggest factors in success.

When the goalposts are moved, it can seem like you did a lot of work for nothing. That can be one of the main frustrations. To keep things in perspective, it helps to consider all the early placement work as a placement study. It's the same sentiment for routing. You're finding the pain points and sorting out the power domains. A lot of that work will stick, although the neighborhoods may shift around on the map.

While you are floor-planning around the critical nets, it is wise to fan-out the chips but leave the interconnects from chip-to-chip for later. That makes moving a cluster much easier, while retaining the essential geometry for each device. How do you get the "essential geometry?" The first method is design reuse; don't reinvent the wheel if you can copy a working circuit.

Leverage the chip vendor. Next are the data sheets. Your chip vendors want you to succeed so you keep buying their product. They are always eager to show the best way to implement their chips. Expect them to be conservative with the reference designs, and do your best to capture the essence of the data while fitting it into your allocated space. Following the data sheet, if not verbatim then close to it, gives you a backstop when you defend your decisions at the design review. (For more on that, see the May 2020 issue.)

You'll wind up making a lot of decisions with no one looking over your shoulder. Share your work with the cognizant engineer(s) but don't expect them to be able to see the whole picture while you're still figuring it out. You'll build trust by executing the design, and they'll give you even more runway to make mistakes. At Microsoft, one of the slogans is "fail fast." Get those mistakes out of the way and make room for improvement. If the mechanical outline shrank while the electrical side grew, consider that an improvement. Everyone wants to buy more for less. You want everyone to be a buyer, right?

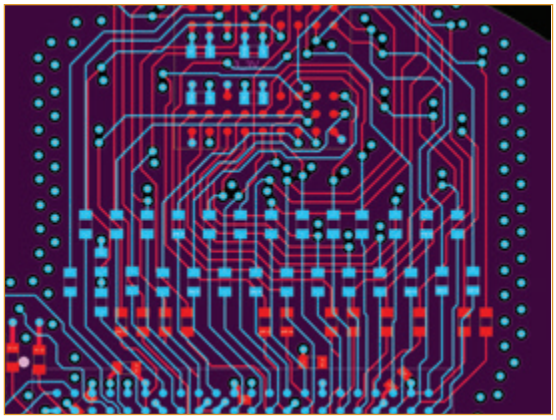


FIGURE 1. Placement of the series resistors was driven by the routing of this memory bus that only used the two outer layers. Note the ground via near every signal via had to be factored in.

Dealing with uncertainty. Starting at the gnarliest device on the PCB, work your way out, leaving a measured amount of slack here and there for both components and routing. I try not to slam everything together at first, even if the final iteration will end up that way. There are too many unknowns; call them unknown unknowns when you don't even know what you don't know. Risk management isn't easy but necessary if you don't want to design yourself into a corner.

The physical designer can and will need extra

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

clearance for a gusset or heat pipe. The electrical engineer means well when they add another filter cap. Who knew that one of the components would become obsolete or come with a 40-week lead-time? The fabricator will ask you to upsize the capture pads or add a little more space between the differential pairs. People you didn't even know were involved could show up at the design review with an agenda unknown to anyone but themselves. It happens.

Everyone in the room is under the same schedule pressure with a lot of things on their plate. I've said it before: consider any change an improvement, never a mistake. Show that attitude and they'll come back for more. There is no such thing as idle time once you're on a design. Future-proof the layout by making the most of the available area. Un-crowd the components and traces or learn to do so the hard way.

"While floor-planning around critical nets, fan-out the chips but leave interconnects from chip-to-chip for later."

PCB social distancing. Using local vendors requires a different approach than I'd use with overseas fabricators. My snowman pair of vias – a microvia and a core-via – had to be turned into more of a dumbbell than a snowman because I violated the same-net via-to-via rule from the vendor. I had no idea. What worked at Qualcomm way back about 10 years (!) ago is no longer good enough. Every core via is met by two microvias. Hundreds of them had to be adjusted to add 76µm of "social distance."

That was a rough day and a little more. I was fortunate to have completed the routing study ahead of time. The point is start with strong design rules and then back off a little if you can. It was the cumulative space that I left everywhere that made the extra spacing possible without basically starting over. Sending early data to the stakeholders has a lot of value. Had I not taken the time to generate a DfM document package earlier in the project timeline, the "last minute" would have a long day or two. I'm writing about this "improvement" so you don't have one of those days. □

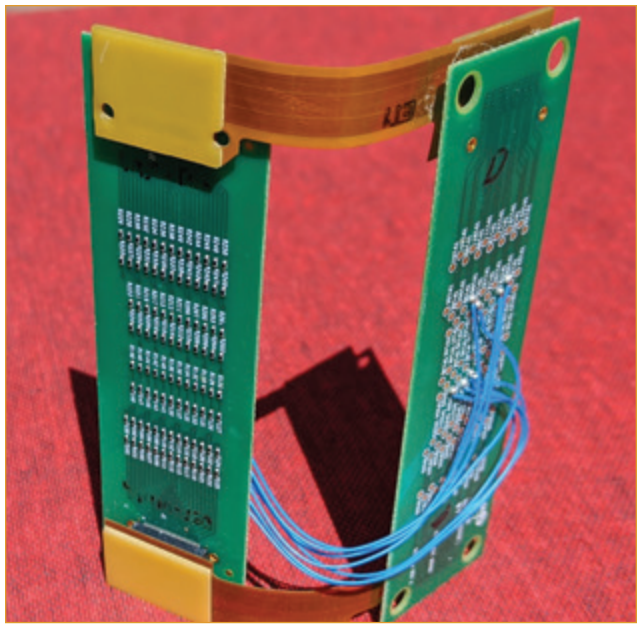


FIGURE 2. Ironic that a board supposed to cure a mis-wired flex needed eight blue wires and an X-acto knife in the build kit. We did it all in one day, but ....

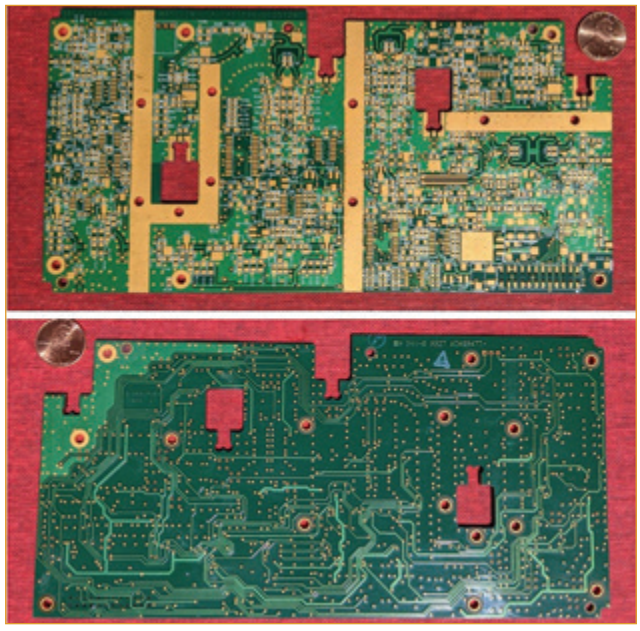


FIGURE 3. Populating only one side of the board and sticking to surface mount components helps the assembly team.

Coping with the March of Technology

And matching materials to the equipment that will advance our world.

WHATEVER WE MAY learn about the origins of Covid-19, and however inconclusive the information may be, we can be almost certain it had nothing to do with radio waves. I'm sure I'm not alone in feeling disappointed about the attacks made on mobile phone masts during this crisis, carried out in the misguided belief that this kind of vandalism can halt the virus.

Fortunately, instances of such extreme technophobia have been few. It seems every new technology wins vocal detractors, however beneficial its effect on peoples' lives. In recent years, our industry has had to deal with claims about grisly health risks associated with mobile phones, the effects of "wind turbine syndrome," and the evil propagated by 5G.

Advanced technologies will hold the key to our defense against Covid-19. We will need the know-how of pharmaceutical labs to create an effective and practicable vaccine, and engineering skills to develop new respirator designs better adapted to the needs of coronavirus patients than are conventional ventilators or CPAP devices. Moreover, effective virucides will be needed to enhance cleaning in places such as hospitals, waiting rooms, factories, warehouses, public transport vehicles, and aircraft. Irradiating at-risk areas using germicidal UV-C lamps could be an option and could easily be automated using mobile robots.

UV-C irradiation has been used successfully in applications such as water treatment for many years. The mercury-vapor germicidal lamp was commercialized in the 1930s, although the mercury's natural radiation wavelength of 253.7nm is not quite perfect for maximum germicidal effect, and, in addition, conventional UV-C light sources are a human health hazard, being both carcinogenic and cataractogenic. However, it is possible to fine-tune LEDs to emit far UV-C at the exact wavelength required to disrupt virus DNA, while not causing biological damage to exposed mammalian cells and tissues. On the other hand, the LED die temperature must be kept stable to ensure the emitted wavelength remains within a narrow range as close as possible to the ideal far UV-C wavelength.

In LED lighting, thermal management is usually designed from a reliability standpoint. Wavelength shift is a secondary concern. Automotive lighting customers, for example, may choose insulated metal substrates (IMS) to stabilize the die temperature at a level calculated to ensure the lamp lasts for the intended lifetime of the vehicle. When designing a germicidal source, in contrast, thermal management is primarily tasked with stabilizing the emitted wavelength. A temperature-related drift of just a few nanometers could be critical.

Far UV-C radiation kills living cells by disrupting the DNA to prevent the cells from reproducing. Clearly, we need to use this technology sensitively to minimize damage to the wider ecosystem. However, although highly effective against microbes, the threat to human health is less than skin deep. The energy contained, at a frequency of about 1360THz, is unable to penetrate the outer, nonliving epidermis.

Humans have nothing to fear from far UV-C or, indeed, our mobile phones and the various wireless networking infrastructures that operate at radio frequencies several orders of magnitude lower. We know radiation up to about 300GHz, which is far above the highest frequencies planned for 5G, is nonionizing and poses no health risks.

5G will employ a greater variety of frequencies than any previous system to support more services, provide greater connection capacity, carry more data, and at the same time handle the growing volume of machine-to-machine communications. Conceived to provide all-enveloping and pervasive wireless connectivity, its positioning means there is no such "thing" as 5G. Instead, it will be many "things," embodying an incredible diversity of technologies. In the future, it is likely to encompass Wi-Fi, as we know it today, to ensure optimized quality of service everywhere.

The first 5G networks will be non-standalone (NSA) hybrid implementations that combine 4G and 5G technologies. These will operate in the sub-6GHz range, aka 5G frequency band 1 (FB1). Given the rollout of 5G handsets is expected to take five to eight years to complete, the transition to full standalone (SA) 5G New Radio (NR) operating in FB2 (24GHz to 50GHz, eventually reaching into the V-band up to 77GHz) could take time.

Optimizing communication range, RF transmit power, and link margin becomes increasingly challenging at higher frequencies. In urban areas, closer cell spacing, combined with beamforming and antenna diversity, can overcome some of these limitations on communication distance. On the other hand, longer RF range is a must to serve locations such as rural areas. The reality is 5G will likely make full use of both FB1 and FB2 for the long term.

Designing equipment to operate at FB2 frequencies

continued on pg. 31

ALUN MORGAN
is technology ambassador at Ventec International Group (ventec-group.com); alun.morgan@ventec-europe.com.

PCB2DAY

Bringing workshops and webinars on design and assembly to you!

JOIN OUR WEBINAR FEATURING:

IoT PCB Design and Layout
Rick Hartley

$50 Now On Demand

Printed circuit boards for the Internet of Things are often driven by the need for low-power one-, two- or four-layer, low-cost boards. This combination can make PCB design a serious challenge. Low-layer count with excellent signal integrity, low noise and no EMI issues requires specific PCB design skills.

This special two-hour webinar will discuss the following:

- When line impedance control is needed
- Impedance control with a "zero" cost adder
- Keeping circuit energy from spreading
- Proper circuit grounding in low-layer-count boards
- Power distribution without the benefit of power planes
- Controlling ground bounce and crosstalk

Who should attend: PCB Designer/Design Engineer, System Designer, Hardware Engineer, SI Engineer

Target audience: Beginner, Intermediate

Sponsored by: EMA Design Automation®

Produced by: pcb2day.com

PCB2DAY

The No. 1 Weapon Against Crosstalk

Trace separation; length parallelism; stackup: Does one stand out?

IT'S BEEN SOME time since I've seen an article on crosstalk, so I decided to take the opportunity to walk through the subject in a soup-to-nuts overview for those in the PCB design community who may be interested in why crosstalk-savvy PCB designers and hardware engineers use various design rules for controlling crosstalk. In the process of doing so, we'll identify which design tweaks provide the most leverage for controlling far-end crosstalk.

Crosstalk is unwanted noise generated between signals. It occurs when two or more nets on a PCB are coupled to each other electromagnetically, (even though conductively they are not connected at all). Such coupling can arise any time two nets run next to each other for any significant length. When a signal is driven on one of the lines, the electric and magnetic fields it generates cause an unexpected signal to also appear on the nearby line, as shown in **FIGURE 1**.

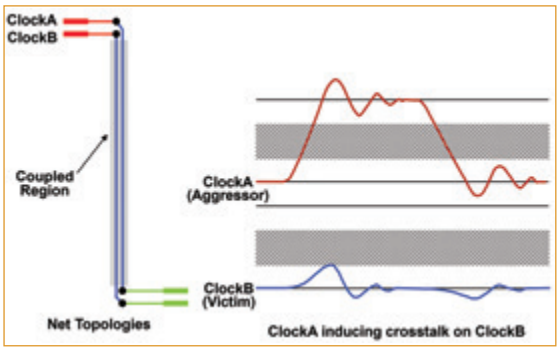


FIGURE 1. Crosstalk occurs when two or more neighboring traces couple together.

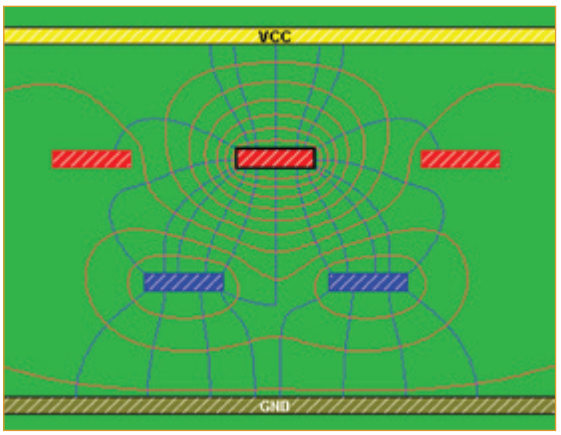


FIGURE 2. Victim nets can be above, below, or adjacent to an aggressor net.

A number of factors combine to create an unwanted crosstalk signal: the length over which the traces are coupled, the distance between the traces, their positions in the PCB stackup, what driver ICs are used on both the "aggressor" and the "victim" lines, whether the lines are terminated, and so forth.

Crosstalk is a particularly hard phenomenon to anticipate and control unless it is simulated, because there is almost no way of intuitively knowing how much crosstalk voltage and current will develop due to a given coupling. Nevertheless, semi-conservative design guidelines can be useful, although almost always at the expense of board real estate.

In crosstalk parlance, the "aggressor" signal or trace switches and causes crosstalk. The "victim" signal or trace responds by developing an unintended signal. The effect is three-dimensional in nature. Victims can be adjacent on the same layer or above or below the aggressor (**FIGURE 2**).

Actually, two coupled signals are imposed upon the victim net: a forward signal and a backward signal. The "forward" pulse travels along with the aggressor's signal, and a "backward" pulse travels back from the aggressor signal. Crosstalk at the victim's far end is called "far-end crosstalk," or FEXT, and coupled voltage at the near end is called "near-end crosstalk" (NEXT). **FIGURE 3** shows both forward and backward crosstalk. The backward signal often ends up traveling forward after reflecting off a driver.

Current is injected into the victim by electric fields (the lines that run orthogonal to the traces in Figure 2) caused by capacitive coupling interactions between the aggressor and victim nets. These interactions are affected by conductor surface area and distance, and generally terminate at adjacent conductors. *Voltage* is induced on the victim by magnetic fields. These are inductive (transformer) coupling interactions, which are somewhat circular – surrounding the aggressor and victim nets. These interactions are *not* generally stopped

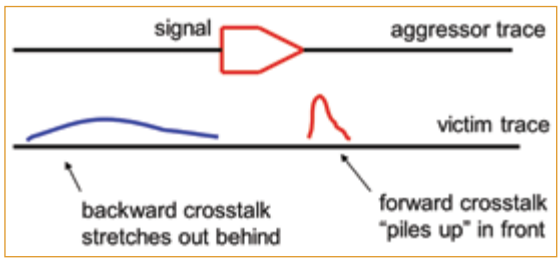


FIGURE 3. An illustration of both forward and backward crosstalk on a victim trace.

BILL HARGIN
has more than 25 years' experience with signal-integrity software and PCB materials. He is director of everything at Z-zero (z-zero.com); billh@z-zero.com.

by conductors and can therefore extend around multiple adjacent conductors.

Crosstalk guidelines. The most common crosstalk design rules involve trace-to-trace separation. A PCB designer might, for example, set an auto-router to 4-mil trace width and 4-mil spacing. This will, of course, maximize router completion, but the resulting design will incur 20 to 60mV of crosstalk. Adjusting noise-sensitive victims to more than 6-mil trace-to-trace spacing can help avoid this problem (FIGURE 4).

Because electric fields terminate at reference planes, traces close to reference planes have reduced crosstalk. Capacitive trace-to-trace coupling drops off quadratically with the distance from the reference plane(s), so traces within 4 mils of a reference plane will be much more immune to crosstalk than a trace 6 or more mils from the nearest reference plane. And symmetric striplines – because of their relative proximity to not one, but two reference planes – have relatively higher immunity than microstrip signals.

Moreover, there's a dielectric-constant effect to consider. High dielectric constants (Dk) concentrate the electric field, resulting in relatively poorer crosstalk performance, in a roughly linear relationship between Dk and capacitive crosstalk.

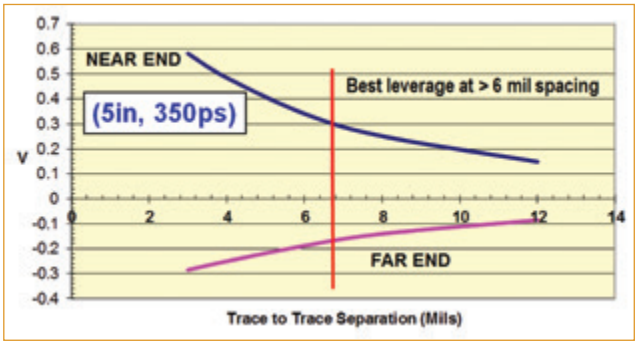


FIGURE 4. Using two parallel, 5-inch lines, the graph shows the curves for NEXT and FEXT beginning to flatten out at around 7-mil spacing between aggressor and victim nets. Tighter spacing, to the left of the vertical line, results in more crosstalk, and wider spacing to the right of the vertical line results in diminishing benefit.

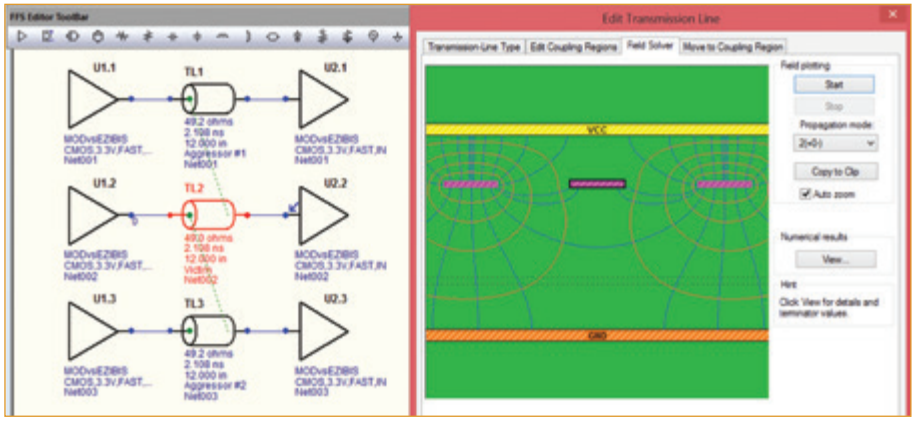


FIGURE 5. Crosstalk is easily illustrated with the aggressor-victim-aggressor example shown. (Shown with Mentor's HyperLynx LineSim.)

Example: Crosstalk on a bus. Suppose you're designing a bus and want to guarantee no more than 200mV of crosstalk can occur on any signal. Here is the process of developing the proper routing constraints to achieve it. A typical bus in a modern digital system contains many physically parallel traces – 16, 32, 64 – maybe even more signals. To analyze crosstalk on such a bus, however, you can narrow the scope to a single "victim" trace, with "aggressor" nets on either side.

Let's start with coupled, coplanar 6.0-mil-wide (W) striplines, running parallel for 12" with trace-to-trace separation of 8.0 mils (S), through a 4.3 Dk dielectric with a 5.0 mil height (H) (FIGURE 5). A simulation with HyperLynx LineSim (FIGURE 6) shows the far-end crosstalk to see how much crosstalk occurs with the initial arrangement. With 590ps (0.59ns) driver-switching speeds on the two aggressor nets, and no signal injected on the victim net, about 600mV on the positive side will be injected into the far-end victim waveform, and 660mV on the negative side – both well beyond our design criteria of 200mV maximum crosstalk.

Crosstalk is a complex effect influenced by many different geometric factors: e.g., driver-IC technology (Tr, Tf, output impedance, and drive strength), trace width (W), copper weight (T), parallel-line length (Lp), trace separation (S), PCB stackup [layer ordering, Dk, and dielectric thickness (H)], and line-end termination. (Crosstalk generally requires more complex termination than single-line reflections.) Rules-of-thumb

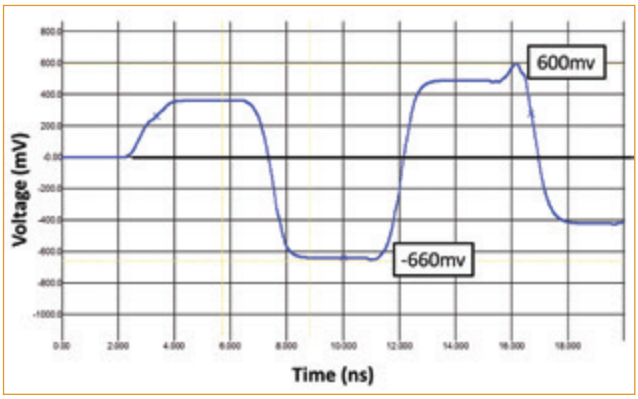


FIGURE 6. Far-end crosstalk (FEXT) on the victim net shown in Figure 5.

exist for controlling crosstalk, but to minimize crosstalk while controlling cost on a specific design requires a good simulation tool. In the following section, we'll go through an iterative process for dealing with crosstalk on the design in Figures 5 and 6 to see if some reasonable design rules emerge.

Crosstalk reduction techniques. A crosstalk lever that might be overlooked sometimes is the copper thickness. In the

TABLE 1. Simulation Results for Reducing Crosstalk Shown in Figures 5 and 6

Rank	Description	% FEXT Reduction
	Original configuration: W=6 mils; T=1oz.; Lp=12 mils; S=8 mils; Dk=4.3; H=5 mils	0%
	Reduce copper thickness (T) to 0.5oz.	~0%
	Reduce parallel length (Lp) to 6 mils	~0%
4	Increase trace separation (S) to 12 mils	33%
	Reduce capacitive crosstalk: Dk=3.8	~0%
3	T=0.5oz., Dk=3.8, H=4.5	60%
2	Reduce W to 5 mils and increase H to 3.75 mils	65%
1	Reduce W to 5 mils, H to 3.75 mils, and increase S to 9 mils	75%

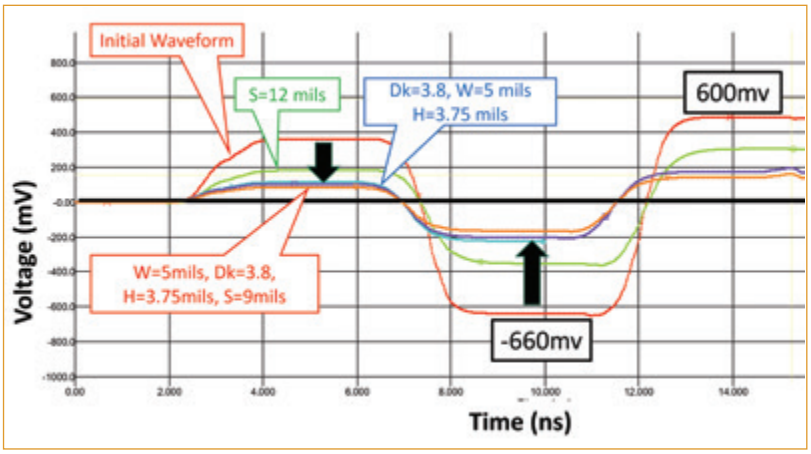


FIGURE 7. Top four ways of reducing crosstalk on Figure 5 bus design. Resulting design rule is W=5.0 mils, Dk=3.8, H=3.75 mils, and S=9.0 mils.

example above, signals have used 1-oz. copper. That's thick for a signal trace. One might think reducing copper thickness will reduce capacitive coupling, though simulation shows the result is not significant in practice. Nevertheless, for the remainder of this discussion, we'll use the more common 0.5-oz. copper.

One possible technique for reducing crosstalk is to reduce the length over which aggressors and victims run parallel to one another. This poses some practical problems on the routing side – those traces are parallel on a board for a reason – but it's instructive to see what happens when the parallel coupling region is reduced from 12.0" to 6.0". Surprisingly, this doesn't reduce crosstalk at all; it simply moves peak crosstalk amplitudes to the left in the time domain. Reducing parallelism alone, as a crosstalk lever, isn't quite as powerful as we might think.

Another common way to decrease the crosstalk is to increase the separation, S, between the traces. Increasing trace separation from 8 to 12 mils reduces crosstalk to 400mV on the positive side, and -400mV on the negative side – still well beyond where we would like, and in the process of making this change, we use a good bit more board space.

There are many ways besides trace separation and length parallelism to affect crosstalk. One that is sometimes overlooked is the PCB stackup. Recall we started with Dk=4.3. What happens if we try to reduce *capacitive crosstalk* by using a lower-Dk material, say D=3.8? Through simulation, it turns out the improvement from this change alone is negligible. In the process of using 0.5-oz. copper, and reducing the Dk of the dielectric, however, trace impedance increased from roughly 50Ω to just under 57Ω. (Remember: Impedance is inversely related to the square root of trace capacitance, which is tied to the Dk of the dielectric.) So, reducing the dielectric thickness (H) from 5.0 mils to 4.5 mils between the stripline layer of interest and the nearest reference plane increases the capacitance again, pulling the impedance back to around 50Ω. The combination of these factors gets us much closer to our goal, resulting in 211mV on the positive side down to about 230 mV on the negative side – more than 60% but still above our target of 200mV.

Reducing trace width (W), which *increases* impedance (Z_0), and then narrowing the dielectric thickness (H) to pull the impedance back down to around 50Ω is another potential way to reduce crosstalk. Reducing W to 5.0 mils and H to 3.75 mils results in roughly 200mV of both positive and negative crosstalk.

By narrowing trace width (W) by 1.0 mil, the overall bus width decreased in mils by the number of bits minus one. With an interest in gaining more margin, while keeping the overall bus width as in the initial design, adding another mil to the spacing (i.e., taking S from 8.0 to 9.0 mils) results in plenty of margin: 160mV on the positive side and 170mV on the negative side.

TABLE 1 summarizes effects on the topology in Figure 5, and their relative impact on FEXT, ranked by relative reduction in worst-case crosstalk.

FIGURE 7 shows the top four ways of reducing crosstalk on this particular bus design. The resulting design rule is to use W=5.0 mils, Dk=3.8, H=3.75 mils, and S=9.0 mils.

Parting thoughts. As I've been trotting around talking to engineers and PCB designers for the past 10 years, I've heard many references to the use of thinner dielectrics, so for some readers the contents of this article may be review. But I have yet to see an article that compares the different levers for controlling crosstalk, with emphasis on the fact that material selection and specifically laminate thickness play the most pivotal role in controlling far-end crosstalk (FEXT).

In a future column, I'll expand on the details of how tighter E-field coupling to the nearest reference plane works, with some accompanying visuals and perhaps a review of Maxwell's equations. □

REFERENCES

1. Bill Hargin, *Printed Circuits Handbook,* seventh edition, McGraw-Hill Education, chapter 20, 2016.

An Expectation of Collaboration

The PCEA and SMTA find common ground.

KELLY DACK, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). Read past columns or contact Dack; kelly.dack.pcea@gmail.com.

THIS MONTH, I share updates on the PCEA website and reports on some inspiring collaboration taking place between the PCEA and a well-known industry organization that appears to have a high potential for synergy for all engaged.

I'm always happy to mention that PCEA Chairman Steph Chavez has prepared a message as well, where he provides an overview of his take on adapting to the new normal by doing more with less.

Last, we are not able to provide any reports on local chapter activities due to continued social distancing requirements. However, we will share our most updated list of professional development opportunities and events, which we hope you might find useful. As always, stay tuned for more updates.

PCEA Updates

Words ending in "ation" can affect our mission. Stay positive!

Throughout the week, I lap up a lot of evening news. Like you, I'm tired of so many negative news reports about "frustration in the nation regarding the presentation of some information regarding an observation that it is a violation to meet together in an organization without six feet of separation until after there is an indication of a successful vaccination declaration." In effect, I've become oversensitized to words ending in "ation." They cause me to itch. But a brief conversation I had with PCEA Chairman Steph Chavez quickly desensitized me to these "ation" words.

PCEA and SMTA. Steph briefed me on an exciting meeting he had with PCEA vice chairman Mike Creeden and global executive director of the Surface Mount Technology Association Tanya Martin. Over an hour, the three spoke about potential collaboration between SMTA and PCEA.

Wow, a realization! Steph employed some "ation" words in a positive conversation, which offered me some inspiration. I then decided the focus of this month's column would be collaboration. Steph, Mike, and Tanya also discussed future goals and how the two organizations might work together beyond the Covid-19 pandemic.

SMTA is headquartered in Eden Prairie, MN. It is volunteer-driven and relies on its members for leadership. The SMTA membership is filled with many electronics industry corporations and individuals who have just about everything to do with the processes, materials, and services essential for sustaining the electronics industry. The PCEA was formed to organize, collaborate, educate, and inspire an already sizeable, established community of PCB designers who sought to include and encourage fellowship with anyone involved in printed circuit engineering: stakeholders and representatives of manufacturing, materials and processes.

Before the formation of PCEA, these professionals had been basically functioning on their own at local levels for years. They were moving into the new decade, largely unrecognized and underrepresented in the electronics industry. Local functions often involved local leadership soliciting experts from the outside PCB manufacturing and engineering communities to educate and inform the design-based chapters about new design software, materials and manufacturing processes.

Steph Chavez said the three spent over an hour discussing their goals for the near future. "It has been pretty much a one-way street," Steph said of the flow of awareness of process and materials. "People in our chapters have been engaging and learning about our engineering stakeholders for decades to design better." But he also pointed out, "Still, today, due to limited representation, very few stakeholders in our industry understand what a PCB designer does or how a designer fits into the engineering and manufacturing puzzle."

Steph makes a good point. When communicating with most anyone other than PCB engineers, designers get blank stares when defending their design response to management during a project. It can be vexing for designers who attempt to explain their reasoning for stackup and line width for a controlled-impedance PCB stackup solution to HR and management during a job interview. Management is included in the list of PCB project stakeholders, yet they appear to not understand what a PCB designer does and fail to see the value of the knowledge.

SMTA executive director Tanya Martin

Tanya Martin acknowledged SMTA's desire to engage more with the design community energy coming out of the PCEA. "The SMTA is pleased to support PCEA, as we've

long recognized the importance of more collaboration in areas that affect PCB design, manufacturability, cost drivers, etc." The goals of electronics industry stakeholder awareness between the two associations appear to fit well, according to Tanya. "Working together will expand SMTA's breadth of technical topics, as well as provide the PCEA with an established platform to share tribal knowledge and education, creating additional member benefits for both organizations."

In a short period of time, new fruit from blossoms of collaboration between the SMTA and the PCEA will be ripe for harvest, and the electronics industry's supply chain of PCB engineering knowledge and awareness will certainly be strengthened. Tanya summarized the meeting well: "SMTA has outstanding representation at the chapter level that will pair well with PCEA's chapters to drive the mutual mission of technical education, dissemination of knowledge, and industry connection, which will build upon the grassroots efforts that both associations were founded on."

PCEA website launch. Good web authors are hard to find. Our PCEA executive staff has been working with teams from a commercial web authoring business to provide the printed circuit engineering communities with top-rate, rich content of which we can all be proud. Unfortunately, the commercial authoring service we contracted with was not cutting the mustard.

Our meetings to move forward with them on our content started looking like a bad PCB design review: What are all those extra holes for? How will my differential pairs couple when spaced an inch apart? And what are all those splits doing in the reference planes? Design reviews can be like that for any type of design. The good news is the input data our team provided were complete and clearly defined. The bad news is there appeared to be a lack of comprehension and education on the part of the web designer regarding the input details, resulting in poor layout.

What can we learn from this? Other design communities – including web design – are not immune to a lack of collaboration, education or inspiration in their roles. Ironically, while the PCEA is specifying a website to foster these attributes within the electromechanical industries by creating and leveraging a prime website, the web authoring industry is failing to "meet spec" due to lack of the same attributes. It is a vicious circle, which I exaggerate slightly here for emphasis.

Visit our new website at pce-a.org (**FIGURE 1**). We want our website to help our members in the best way possible.

FIGURE 1. The PCEA's new website is up and running.

Message from the Chairman

by Stephen Chavez, MIT, CID+

We're in a world of quarantine, isolation, and social distancing. Many are finding it mentally and emotionally challenging to deal with this new normal these days. This Covid-19 pandemic has definitely changed our "normal" workday and environment. This is taking its toll on all of us one way or another. Days have drifted into weeks, and weeks have drifted into months as we continue to maintain our isolation or social distancing.

In this "new normal," with most finding ourselves working from home, the separation of work life and home life has morphed together, which can be a double-edged sword. In many cases, we find ourselves doing more with less, as our new normal workday seems to have simply gotten longer. Those 9 to 10-hr. workdays before Covid-19 are now 12 to 16-hr. workdays, due to all the additional virtual meetings or teleconferences taking place.

As I talk to many friends and colleagues, all agree I am not the only one feeling like we are participating in a three-ringed circus as a result of all these virtual meetings, working on designs and presentations, and having a family life. Without even realizing it, by the time we walk away from our computers at the end of our "workday," we worked much longer than 9 am to 5 pm. In some cases, we've even lost track of whether it is a weekday, Saturday, or Sunday; they've morphed together.

On the flipside, we may be adapting, evolving and collaborating at a much higher level. Because we're isolated with fewer "walk-up" interruptions or that simple "5 to 10-minute water cooler" chat that is actually more like 20 minutes, we're able to focus longer and get more done with fewer distractions.

Due to Covid-19, most if not all in-person expos, conferences and seminars have gone virtual. This has led to more collaboration with less in-person time. For many of us whose business travel has come to a stop, "in-transit" time or "return back to the office and settle back in time" has been replaced with online opportunities, such as webinars and global virtual events related to this industry. Again, we are finding ways to adapt, collaborate, and do more with less.

Our PCEA executive board members are good examples of those doing more with less. Our day jobs have intensified over these past few months as Covid-19 has changed the industry, and the required effort needed to solidify the foundation of PCEA has been a challenge. Nothing ever goes as well as we'd like, and we have our share of hurdles. Murphy's Law always seems present, yet we adapt and overcome. We have crazy days where we feel as if we are in a double-dutch jump rope contest, while juggling multiple tasks at the same time.

In the end, what we are doing and creating is awesome. We have started collaborating and strategically planning with other great industry associations, such as the SMTA, for the

betterment of the industry as a whole. We are identifying ways to fill the educational gap in our respective associations, as we see the PCEA and the SMTA being a one-two punch combination for success in our industry. Mike Creeden and I will collaborate as we represent the PCEA in an SMTA webinar scheduled for Jul. 9. The PCEA will also have a presence at SMTA International, held later this year. We will offer an educational track at this event. Stay tuned for more details.

We launched our official website Jun. 1. The website was one of our hurdles, as we had expected it to be online by mid-May. With much hard work, collaborative effort and passionate determination, we adapted and overcame. We'll follow the website launch with our virtual grand opening scheduled for Jul. 14 at 11 am PST, featuring a presentation from Rick Hartley on the topic "PDN Tips: Successful Power Distribution."

Now that our official website is active and online, and with our upcoming virtual grand opening, you will see more industry activity come from the PCEA, both virtual and hopefully in person in the near future. Our focus is slowing shifting from our PCEA structure and foundation, to collaboration, education and inspiration through industry content and activities.

As always, I highly encourage you all to get involved! Join PCEA by visiting our website (pce-a.org) and registering as a member to become part of the PCEA collective. You can always reach out to me (stephen.chavez.pcea@gmail.com) or Kelly Dack (kelly.dack.pcea@gmail.com) to get more information as well.

Professional Development and Events

It has been our custom to highlight all upcoming industry events. We will continue this; however, with the challenges brought upon our industry by Covid-19, we can only remain hopeful these events will not be affected. If you have an interest in any of these events, please search and contact the event coordinators directly for the latest event status.

- Jun. 25: IoT PCB Design and Layout webinar, with Rick Hartley (pcb2day.com)
- Jul. 14 (11 am PST): PCEA's Grand Opening Webinar – Virtual
- Aug. 11-13: CadenceLive 2020 (Virtual)
- Sept. 8-11: PCB West (Santa Clara, CA)
- Sept. 16-17: Del Mar Electronics & Manufacturing Show (San Diego, CA)
- TBD: AltiumLive 2020 (USA)
- Nov. 11: PCB Carolina (Raleigh, NC)
- May 11-13, 2021: IPC High-Reliability Forum 2021 (Baltimore, MD)

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Conclusion

How are we to collaborate within our organizations, companies, offices, and homes while staying socially distanced and staying at home? We do the best we can with what we have. Just watch; the world seems to be adapting before our eyes and ears. Advancements in conference trends are astronomical.

Within our local PCEA community, it is a good time to plan and reach out. This pandemic will not last forever. It is prudent for all of us to keep looking forward to ways we can hit the ground running when things get back to "normal."

Eat, drink and be merry; collaborate, educate and inspire. Soon, some of us may go back to the office. As always, have hope for the future, and plant your happy seeds now. ▫

The Evolution of FOUR-LAYER Printed Circuit Boards

And why not to cut the ground or Vdd plane. by LEE RITCHEY

Speculation abounds over what a designer should do when making the stackup and design rules for a four-layer PCB. Much of this speculation or rules-of-thumb came about when those not familiar with the reasons for arranging the layers in a four-layer PCB tried to explain what they saw or heard. This article explains how four-layer PCBs came into existence and guides readers on how to create a set of design rules and stackup that results in a solid, functional design with minimum constraints.

Early logic designs were done with two layers. Power was distributed using traces to connect all the power and ground pins to the power supply rails. Logic devices were packaged in 14- and 16-lead dual inline packages (DIPs). FIGURE 1 is an example of such a two-layer logic design. Logic speeds were slow enough that connecting power with traces instead of planes was "good enough." Figure 1 is a design the author did using Bishop Graphics tape to create the artwork in the early 1970s.

As logic speeds (clock rates and rise times) became faster, it was not possible to achieve stable logic operation with such a high inductance power distribution network. To go up the speed curve, it was necessary to add two power planes: one for Vdd and one for ground. For the planes to do their job, they needed to be intact. As a result, these planes were placed in the middle of the PCB, yielding a stackup like that shown in FIGURE 2. (If the planes were on the outer layers, they would be interrupted by component mounting structures and cease to function properly as planes.) Until recently, virtually all PC motherboards and motherboards for gaming consoles were built to this stackup.

For signal integrity reasons, the trace layers are close to the planes over which they run: in this example, 4 mils or 102µm. This thickness is chosen to minimize crosstalk and produce an impedance at or near 50Ω for good transmission line management.

Most of the industry has aimed at an overall thickness of 62 mils (1.4mm) as a presumed standard thickness.[1] Usually trace layers were 2 mil-thick (51µm) copper, and plane layers were 1-oz. copper, which is 1.4 mils thick (36µm). This leaves the thickness of the core at between 48 and 50 mils (1.24 and 1.27mm).

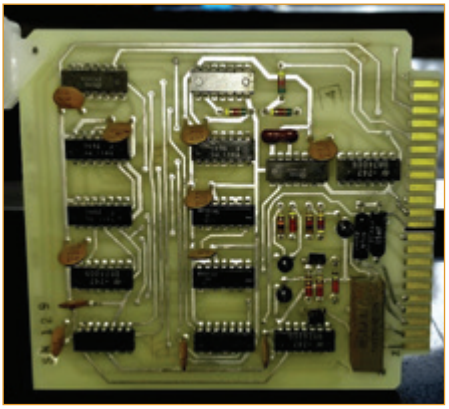


FIGURE 1. Typical two-layer logic PCB.

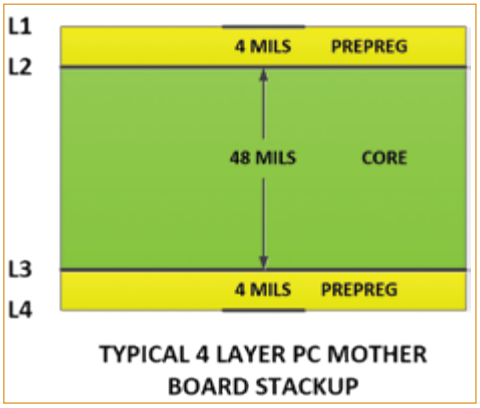


FIGURE 2. The classic 62-mil-thick (1.4mm) four-layer PCB stackup.

Power delivery. A large body of published information demonstrates high-performance logic circuits require the high-quality capacitance created by the Vdd and ground planes placed very close to each other, 4 mils or less (102µm). This is often referred to as power or interplane capacitance. In the stackup in Figure 2, the planes are so far apart there is virtually no interplane capacitance. How do very high-performance PCs and video games func-

tion with a stackup like that in Figure 2? The answer is the manufacturers of microprocessors and other ICs intended for this kind of product have all that capacitance built into the ICs and their packages. The only capacitors needed on these designs are those required by the switching power supplies. It follows components that do not have this capacitance designed in will not function properly on a four-layer PCB.

Signals changing layers. In high-layer-count PCBs, the ground vias connecting all the ground planes together and the interplane capacitance needed by the power delivery system tie the power planes tightly to the ground planes and provide the path for the return current when signals change layers. This interplane capacitance is missing in a four-layer PCB. What happens when a signal changes from layer 1 to layer 4 in a four-layer PCB? The signal quality is compromised enough that the circuits may not perform properly. To avoid this problem, all the signals must begin and end on the same layer (**FIGURE 3**) so there is a continuous copper path under the signal from end to end.

Consequence of cutting a ground or Vdd plane. It can be tempting to cut either the ground or Vdd plane in a four-layer PCB. Cutting the Vdd plane might be considered to permit two different supply voltages to share the same plane. Cutting the ground plane might be considered to separate two groups of circuits from each other such as analog and digital.

When either plane is cut for the above reasons, they cease to function as planes, and the return current path for signals traveling across the cuts will likely have signal integrity problems and may also create EMI. For these reasons, these two planes should never be cut.

If more than one Vdd is required by a design, the primary Vdd should be assigned to the full plane, and the other voltages should be supplied with copper fill in either layer 1 or layer 4. Such fill is visible in Figure 3.

Managing EMI. It is well established that traces running over intact planes are not a source of EMI.[2] Ensuring the two planes in the PCB are not segmented satisfies this requirement. Flooding unused space on outer layers does not affect EMI, as these layers are not sources of EMI. EMI may leave the PCB on wires connected to it. This is prevented by surrounding these wires with shields.

Conclusions

Very high-performance products can be designed using low-cost four-layer PCBs. Success requires the plane layers to be continuous across the entire PCB. The "high-frequency" capacitors needed to support logic operations must be built into the ICs that are part of the design. A stackup similar to Figure 2 is the best compromise between signal integrity and manufacturability. ❑

REFERENCES

1. Lee Ritchey, "Is 63 Mils a Standard PCB Thickness?" Speeding Edge company notes, 2002.
2. Doug Brooks, "90 Degree Corners, the Final Turn," *Printed Circuit Design,* January 1998.
3. Lee Ritchey, *Right the First Time: A Practical Handbook on PCB and System Design,* vol. 2, 2003.

LEE RITCHEY is considered one of the industry's foremost authorities on high-speed PCB and system design. He is the founder and president of Speeding Edge (speedingedge.com), an engineering consulting and training company, and will speak at PCB West in September; leeritchey@earthlink.net.

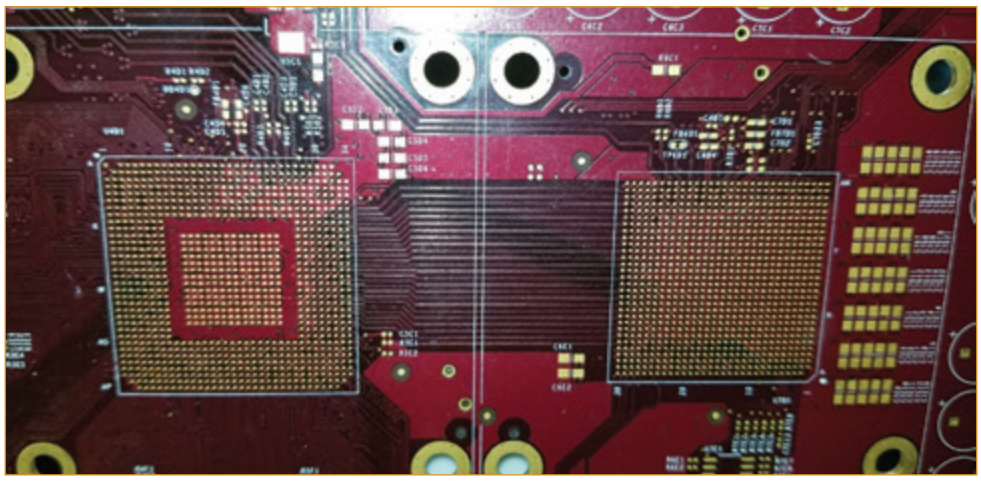


FIGURE 3. Signal routing on a four-layer PCB.

PCB WEST 2020

Conference & Exhibition

Conference: September 8 - 11
Exhibition: Wednesday, September 9

See you in September!

Register Now

Conference Catalog Online

*More than 35 sessions, plus 11 free classes!

*All the hot topics, including grounding, power distribution, signal integrity, flex circuits, and RF circuits

*Training for designers, fabricators and assemblers, from novice to pro

*Rick Hartley and Lee Ritchey

*Professional Development Certificates

*One-day FREE Expo with 100+ leading suppliers

PCBWEST.COM

SANTA CLARA CONVENTION CENTER, CA

PCB WEST 2020

Conference & Exhibition

Connecting Design to Fab to Assembly

Conference: September 8 – 11

Exhibition: Wednesday, September 9

WHO'S EXHIBITING

Accurate Circuit Engineering
Aculon, Inc.
Advanced Assembly
Advanced Circuits
AGC Chemicals Americas, Inc.
AGC Nelco America Inc.
All Flex Flexible Circuits & Heaters
Altium LLC
American Standard Circuits, Inc.
APCT
Arlon EMD Specialty
Bay Area Circuits, Inc.
Beta LAYOUT
Bittele Electronics Inc.
Bowman XRF
Cadence Design Systems
Cicor Group
Clear Blue Engineering
dalTools
Dino-Lite Scopes (Big C)
DownStream Technologies, Inc.
DuPont
DYCONEX AG
Dynamic Electronics Co., Ltd.
Elgris Technologies, Inc.
Elsyca
EMA Design Automation
EM Solutions Inc.
Firan Technology Group - FTG
Fischer Technology, Inc.
Flex Interconnect Technologies
Flexible Circuit Technologies
Freedom CAD Services, Inc.
Fujipoly America
Goal Searchers Co., LTD Zhuhai
Green Circuits
GS Swiss PCB AG
GTS Flexible Materials Ltd.
HIE Display Limited
HSIO/Ironwood
ICAPE Group
Imagineering, Inc.
Integrated Technology Ltd. (ITL Circuits)
IPC-2581 Consortium
Isola
JetPCB USA
JS Electronic Co. Ltd.
Kinwong Electronic Co., Ltd.
Krypton Solutions
Kyocera International, Inc.
Leader Tech, Inc.
LPKF Laser & Electronics
Medcadtron GmbH
Mentor, A Siemens Business
MicroConnex
Minco Products, Inc.
Multek Technologies, Inc.
MV Circuit Technology Co., Ltd.
MVINIX Corporation
NTS
Oak-Mitsui Technologies LLC
Ohmega Technologies, Inc.
Oki Printed Circuits Co., Inc.
Optiprint AG
Panasonic Electronic Materials
PCB Power Inc.
PFC Flexible Circuits Limited
Polar Instruments, Inc.
Polyonics
Printed Circuits
Pulsonix PCB Design Software
Quadcept
RelianceCM
Risho
Rogers Corporation
Royal Circuits
San Diego PCB Design
San-ei Kagaku Co., Ltd.
Sanmina Corporation
Screaming Circuits
SEP Co., Ltd.
Shenzhen Danyu Electronics Co. Ltd.
Shenzhen JDB Technology Co., Ltd.
Shin Yi PCB Co., Ltd.
Sierra Circuits, Inc.
Slingshot Assembly
Somacis Inc.
Summit Interconnect
Sunshine Global Circuits
Sunstone Circuits
SVTronics, Inc.
Taiyo America Inc.
Tempo Automation
Ticer Technologies
Ultra Librarian
Varioprint AG
Vayo Technology
Ventec International Group
Victory Giant Technology (Huizhou) Co., Ltd.
VYCOM Global Sources Ltd.
Xiamen Bolion Tech. Co., Ltd.
Zuken USA Inc.

PCBWEST.COM

SANTA CLARA CONVENTION CENTER, CA

DIFFERENTIAL SIGNAL Design Rules – Or Not

A common assumption is differential signals are "equal and opposite." Is it true? by DOUGLAS G. BROOKS, PH.D.

Periodically, questions about differential trace design rules come up. There is always confusion over whether it is necessary to route differential traces close together, whether a plane needs to be underneath differential traces, or whether to consider differential impedance design rules with differential traces. In one sense, the answers to these questions are difficult, but in another sense they are simple. In fact, if we are not concerned about signal integrity issues, there are no design rules at all. Here is my way of trying to clarify things.

First, what are differential signals, and why are they different? FIGURE 1 illustrates a single (sometimes referred to as a single-ended) trace connecting a driver and a receiver (a) and a differential trace pair (b). Let's say the signal amplitude (with respect to the reference voltage) in Figure 1a is V = +1. In Figure 1b, there are two signals, V+ = +1 and V- = -1. What the receiver in Figure 2 sees is the difference between these two signals, V+ - V- = +1 – (-1) = +2. The first, and most obvious, difference between the two configurations is that differential signals offer twice the signal level to the receiver. Usually, this translates into twice the signal-to-noise (S/N) level. This is a clear advantage over the single-ended case, and is the primary advantage of differential signals, especially when signal levels are low (as with many sensors).

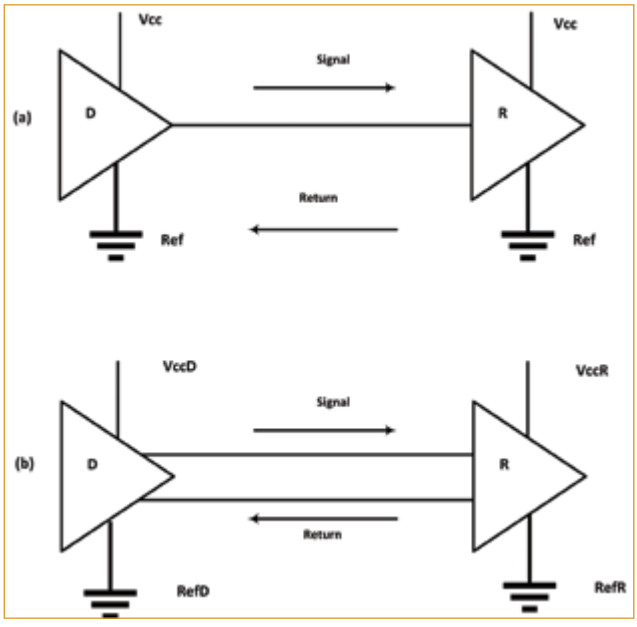


FIGURE 1. Single-ended (a) and differential (b) signals.

There are a few other advantages to differential circuits:

- Every signal has a reference. Single-ended signals are typically referenced to something we show as Ref in Figure 1. This means the references for the driver and receiver must be equal. Differential signals, on the other hand, only reference each other (we will show later this is not necessarily true!) so RefD and RefR can be different. In fact, since the references do not matter, at least in theory, they can both be noisy without degrading the signals.
- Since the receiver only looks at the difference between V+ and V-, any (common mode) noise that gets on the traces is canceled out.
- Further, the switching point between logic levels (between, for example, a logical zero and a logical one) is the precisely defined point where the polarity of the differential signal changes. This is usually much more precise for difference signals than is the switching point for single-ended signals.

So, there are a lot of advantages to differential signaling. The only disadvantage is geography; i.e., twice as many signal traces must be routed.

What design rules are required for differential signals?

In many situations minimal or no design rules are required for single-ended traces. In fact, if there are no signal integrity issues, there are really no design rules required. The same is true for differential signals: *If there are no signal integrity issues, there are no design rules required.* There is nothing inherent in differential signals that requires any special design rules. Let's look at some common "rules" occasionally offered.

A. Do differential signal traces need to be equal length?

A common assumption is differential signals are "equal and opposite." If they are equal and opposite, then the sum (V+ + V-) will always be zero, everywhere. This condition is met if the driver is perfect (i.e., no offset) *and* the trace lengths are exactly equal. But what if the trace lengths are not exactly equal, or the driver is not perfect? Then there will be a difference signal (**FIGURE 2**). Figure 2 illustrates two cycles (720°) of a differential signal pair. V+ is shown in red, and V- is shown in black. If the signals are exactly equal and opposite, there is no net difference signal. But if there is a slight offset either in the driver or in the trace lengths, there can be a net difference signal (blue) that now becomes an uncontrolled common mode signal somewhere in the circuit.

That difference signal is a common mode signal (current) that will exist in an uncontrolled manner in the circuit. Uncontrolled common mode signals are the source of most EMI problems we face and are to be avoided. Therefore, if EMI is a concern, *differential trace lengths need to be exactly equal.*

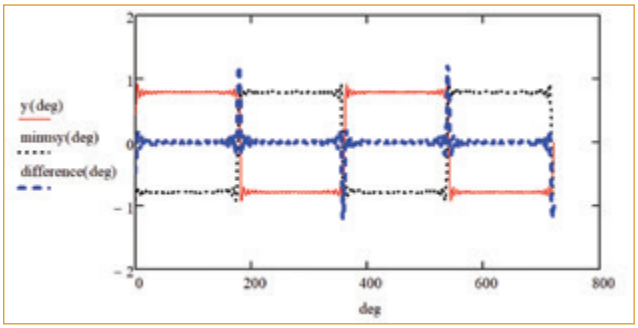


FIGURE 2. If differential signals are not exactly equal and opposite, there will be a net common mode signal somewhere.

B. Do we need planes underneath differential traces?

Assuming it is not practical to find perfect drivers and design exactly equal length traces, and *if* we are concerned about common mode EMI, then we must face the reality that these common mode signals may exist and must be controlled. The easiest way to control them is to provide a plane directly under the traces, so they may return to the driver as close as possible to the signal traces, thereby minimizing the potential for EMI.

Note: In this context, we are not talking about a plane required for impedance control or trace impedance. We are talking about the control of EMI by "routing every trace close to a continuous, related, underlying reference plane."[1]

If there is an underlying plane, the next question is where do we connect it? Normally, we connect it between the reference voltages, Ref. If we do that, then RefD and RefR must be equal. Otherwise significant ground loops will occur. Also, presumably we lose the differential trace advantage (i) referenced above – that the reference voltages need not be well-controlled. One might argue that a bypass capacitor can be used here, but that goes beyond the scope of this article.

C. Do differential traces need to be routed close together?

The signal on each trace *may* radiate away from the trace and cause a coupled signal problem somewhere else in the circuit (crosstalk), or it may radiate off the board and cause an EMI problem. *If* this is a concern, it can be mitigated somewhat by routing the traces close together. Since the signals are equal and opposite, if the traces are close together, the radiated signals will be (approximately) equal and opposite and (approximately) cancel at the victim trace. This cancelation becomes less effective the farther apart the traces are.

Traces that are good radiators of EMI are also good receivers of radiated noise. If differential traces are routed close together, each trace will receive approximately the same amount of noise, and that noise will cancel out. But this effect is less beneficial as the trace separation widens.

So, *if* radiated or received noise may be a problem, the effects can be minimized by routing the traces closer together.

D. Do impedance design rules need to be followed?

The reason we use controlled impedance (transmission line) traces is to control reflections. If reflections are not an issue, then controlled impedance traces are not an issue. *If* reflections might be a problem, each individual differential trace needs to be treated as a transmission line and properly terminated. This usually means we must provide a plane under the trace and then control the impedance. We control the impedance by geometry; i.e., by controlling the relationship between the width and thickness of the trace and its distance above the plane (and the relative dielectric coefficient of the dielectric between the trace and the plane). The question remains how and where do we connect the plane? (See discussion above.)

E. Do differential impedance design rules need to be followed?

If we are concerned about reflections (D), we need to be worried about controlled impedance traces. And *if* we are concerned about radiated and/or received noise (C), then we want to route the differential traces close together. Under these two conditions, the differential traces will couple together, and differential impedance rules must come into play. Understand there is nothing inherent about differential signals that requires differential impedance control. But under the conditions defined under (C) and (D), differential impedance rules become important.

TABLE 1. Signal Integrity Concerns

If this is the concern:	...use these rules:
1. None	None
2. Common mode EMI	A or B
3. Radiated EMI or received noise	C
4. Signal reflections (a)	If NOT C, then B & D
5. Signal reflections (b)	If C, then B & D & E & F

continued on pg. 41

IoT Suffers from a Lack of STANDARDS

What the electronics industry must do to change that.

by JOANNE FRIEDMAN, PH.D., and BARBARA GOLDSTEIN

Ed.: This is the seventh of an occasional series by the authors of the *2019 iNEMI Roadmap*. This information is excerpted from the roadmap, available from iNEMI (inemi.org/2019-roadmap-overview).

To realize the benefits and potential of the Industrial Internet of Things (IIoT) or move toward Industry 4.0, the industry must overcome several challenges ranging from securing the factory equipment used to produce secure IoT-ready products to defining the cobotic dialogue so collaboration between humans and machines can be used to drive innovation, while providing efficiencies with minimal workforce displacement in this industry and those of its customers.

Aside from technical issues, ethical, geopolitical, economic and regulatory issues may affect the current and future state of the industry.

Hackers have already wreaked havoc by infiltrating connected IoT devices. Paradoxically, they usually aren't targeting device owners, who often remain unaware of security breaches. Instead, the hackers may simply use IoT devices as starting points for attacks directed against another target. For instance, the 2016 Mirai attack, which used IoT devices to launch a distributed denial of services against gaming servers, ended up attacking the Internet infrastructure, causing shutdowns across Europe and North America that resulted in significant economic damage. As the IoT base continues to show double-digit growth rates, security is simultaneously a major industry challenge and a significant opportunity.

To some industry customers, the semiconductor companies are obliged to develop solutions that strengthen IoT security. However, research suggests that four major challenges may prevent them from capturing the opportunities:

Gaps in technical sophistication. By nature, a complex system of connected devices opens the potential for many new attack vectors, even if each device is secure when used independently. Thus, any part of the overall system can be a target — from the ethernet cable to every jack, port, API connection, or stream of data.

Further, attacks may target the least sophisticated or least protected element of a system or may use a multipronged approach. As a result, innumerable permutations and combinations of vulnerabilities and the risks they pose must all be considered when implementing a security strategy.

Although several electronics industry segments may have a role to play in developing the robust, comprehensive security solutions needed for IoT or IIoT, it is not yet clear which segment will take the lead.

Standards are absent or immature. IoT and IIoT lack well-established overarching standards that describe how the different parts of the technology stack should interact. By example, some industrials still rely on a small set of proprietary, incompatible technology standards issued by the major players, while other segments, such as automotive or smart buildings, have at least rudimentary standards. This lack of standards and a standards architecture is likely slowing IoT and IIoT adoption or discouraging manufacturers from developing new technological solutions.

Customers and end-users view IoT security as a commodity. Although electronics producers and their customers consider IoT security essential, at this point in the maturity of mobile devices, like smartphones for example, security is often perceived as a commodity – a basic feature that does not merit higher prices. This creates a fundamental disconnect between the desire for security and the consumers' willingness to pay for it. Unlike challenges that can be addressed solely with technology or standards, this issue also requires changing customer mindsets: in other words, convincing them security is worth additional cost.

Industry verticals. Since IoT industry verticals differ in many respects, their security challenges also vary by industry. Insufficient security technology in industrials, for example, relates to the large variety of legacy systems in the field, as well as a lack of standards. In many businesses, operations largely depend on older computer systems and dated machinery. When companies connect those legacy systems to the Internet, they often struggle to maintain security or find it impossible.

To resolve the issues with legacy systems, leaders might

Are you getting to the bottom of your via?

Prevent connection failures in thick PCB substrates with plasma treatment

New **VIA™ Series 2.5** cleans deep, narrow vias where other processes can't go

VIA™ Series 2.5
Plasma System

Contact us now to learn more
+1-925-827-1240 / info@nordsonmarch.com

nordsonmarch.com

Nordson MARCH

consider implementing compensating controls, such as ring-fenced networks or redundant sensor networks. Within niche applications for specialty equipment, OEMs typically create tailored solutions for their customers. In many cases, however, they have little incentive to provide IoT or IIoT security features that may drive up the cost of their solutions. Thus, the situation will not change until end customers specifically demand such applications and the security that goes with them – a trend that will take time to gain momentum.

In summary, the IoT security challenge is complex, providing opportunities within the middle layers of the technology stack and between application and hardware, such as software infrastructure, gateway communication, and communication protocols.

Architectural Framework Needs

Although there are different schools of thought on why digital initiatives so often fail, the consensus seems focused on two areas: human capital, where fear of change and organizational structure are the root cause, and/or the "shiny new object" syndrome, mismatching the desired outcome (use case) with fragments of emerging or immature technologies.

Aside from the above, evidence suggests that in the case of electronics manufacturing, what is really missing is the means to create and pull the digital thread from concept to consumer (ideation to product disposal): in short, an architectural framework that supports the four design principles of Industry 4.0 (interoperability, information transparency, technical assistance and decentralized decisions) and provides the pathway to phase in the capabilities for advanced manufacturing.

FIGURE 1 is a diagram of what such an overarching IIoT framework might look like.

An Industry 4.0 architecture could address another critical issue: the need to support the bidirectional flow of information between maker and user, as well as accommodating data streams from customers and suppliers. Without this cohesive framework across the industry's segments or sectors, no digital thread can be pulled across the electronics ecosystem by any stakeholder group. This leaves the electronics industry and the sectors it supports digitally fragmented, creating an opportunity for those sectors, some of which are returning to vertically integrated manufacturing models to reap the benefits of digitalization from within (**FIGURE 2**).

The step from digital to physical – or connected, digital technologies to the creation of a physical object – are the essence of Industry 4.0. While it is said it takes a village to raise a child, it also takes an ecosystem to realize the benefits of IIoT and Industry 4.0. Thus, it's vital to use digital information from many different sources and locations to drive the physical act of manufacturing with the desired flexibility, production, quality and cost-efficiencies. To accomplish this objective requires unifying the information technology (IT) and operations technology (OT) silos. This problem is far from new: OT, such as manufacturing execution systems (MES), factory automation and shop-floor systems, has been siloed and somewhat separate from IT for decades. □

JOANNE FRIEDMAN, PH.D., is CEO, Connektedminds. BARBARA GOLDSTEIN is program manager, NIST on a Chip, and associate director, Physical Measurement Laboratory, NIST. They are chair and co-chair, respectively, of the iNEMI Industrial Internet of Things product emulator group.

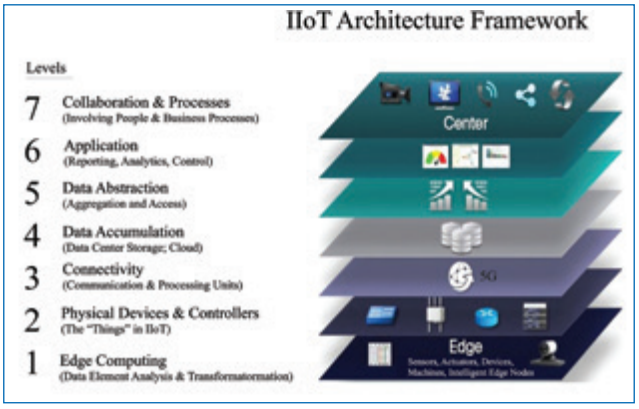


FIGURE 1. Diagram of an overarching IIoT framework. Source: PWC adapted.

FIGURE 2. The bridge between IIoT and IoT. Source: Connektedminds.

Material Gains, continued from pg. 19

places stringent demands on materials. Signal loss in antennas becomes a huge issue, and conventional substrate materials, which tend to have a large dipole moment that results in excessive dissipation of high-frequency signal energy, are unsuited to the task. Ceramic materials have an extremely low dipole moment that helps maximize the signal-to-noise ratio (SNR) at the receiver. Ceramic-filled organic polymers are thus valuable in the search for greater SNR. Ultimately, I expect substrates incorporating PTFE, which is inherently non-polar, to become widely adopted as we search for ultimate signal performance at high frequencies.

Advanced materials represent just one technology among the many being brought together to unleash the full desired performance of 5G across FB1 and FB2. The end-user experience should be unified, uniform, and homogeneous. Under the surface, it will be fascinatingly complex and intricate. □

PRODUCTION AREA Reorganization Pays Many Dividends

A new layout marries staff resources to immediate demand.

by CLINT HANSON

In the fourth quarter 2019, the team at Milwaukee Electronics' headquarters began looking at ways to improve throughput by eliminating customer-focused cells and enhancing worker responsibilities. The goal was to make it easier to shift cross-trained employees among work cells to support variances in demand.

The electronics manufacturing services (EMS) facility was divided into five areas, each headed by a supervisor with direct responsibility for the team in that area. This put resource allocation in the hands of the people who work with those resources. Instead of dedicating space and team members to specific customers, each supervisor now has the flexibility to move their team around based on that day's demand. They can also request additional training for any team member if they feel additional skills are necessary. Additionally, one supervisor was assigned as an assistant to the production manager. A production manager has finite bandwidth. The assignment of a roving supervisor to address day-to-day challenges helps ensure tactical issues don't sidetrack the production manager from focusing on more strategic issues.

FIGURE 1. Production operators in Milwaukee Electronics' SMT area.

The five production areas are:

- SMT, which includes all activity associated with SMT placement and reflow.
- First assembly, which includes component preparation and all through-hole insertion processes.
- Second assembly, which includes post-wash operations, addition of non-wettable components, conformal coating and potting.
- Test, in which a team of test technicians now repairs test failures where they happen with debug data.
- Final assembly, which includes box build, labeling and any additional value-added activity.

Additionally, purchasing now "owns" material from the buy signal to the kit on the production floor. The final inspection area team now reports to corporate quality.

This streamlined the processes, focusing each area on a business view where material flows in and completed assemblies flow out. Employees in each area now focus on eliminating roadblocks associated with the overall throughput in their area and are empowered to address those bottlenecks.

The process also has benefits at the individual employee level that have evolved substantially since inception. Initially, the major benefit was added skills. The company obtained a Wisconsin state training grant that funded courses developed by Milwaukee Area Technical College that were customized to defined requirements and included Lean manufacturing principles, basic electronics training and technician training and are delivered during normal work hours at the Milwaukee facility.

The course structure was designed to offer a career path. The training provides the skills needed for employees to move to higher levels of responsibility and compensation over time. The company has also found that having a production team with enhanced critical thinking skills improved productivity. As a result, the facility has been able to support business growth without having to hire a proportional amount of people. Where increasing process automation reduced headcount, personnel were redeployed to other jobs. During the Covid-19 pandemic, this facility has continued to work at normal capacity, as much of its production involved essential products, and several of those compa-

nies have increased orders. Area school closures did create a potential issue. Teams worked together to figure out how to move impacted employees among shifts to address childcare issues. Employees who did switch shifts also continued to support their prior team members with knowledge transfer where needed. Additionally, at a time when many workplaces were experiencing high absenteeism related to fear of Covid-19, the combination of the company's safe work practices and work hour flexibility resulted in minimal absences. Employees felt the company was prioritizing their needs and recognized the need to help the company also follow through on its commitments to customers.

From a manufacturing efficiency standpoint, many lessons were learned. First, when employees were associated with dedicated work cells, they tended to work through inefficiencies, keeping a machine running or nursing a process recipe without making a permanent change. The combined result of job enhancement, additional training and focused kaizen events has eliminated this behavior, plus instilled a sense of greater ownership of results at all levels. Machine operators are programming machines and "owning" their metrics. Since operators now have a greater understanding of process elements that drive good quality, machines are cleaner and require less maintenance. This has freed manufacturing engineers to focus on process optimization. In the test area, technicians also own their results. Their training now includes electronics, circuit analysis, debug and usage instructions on all test equipment. As a result, they are now better able to troubleshoot and repair test failures, plus communicate trends to the production team.

Within the first two quarters of implementation, results included elimination of 70 bins of work-in-process (WIP). WIP queues between processes have shrunk as each process now works solely to actual demand. Covid-19 also created unanticipated variances in demand during the second quarter 2020, as essential customers stepped up orders to ensure they would have adequate inventory should the facility be shut down. Cross-training made it easy to shift employees to areas with expedited production requirements. ▫

CLINT HANSON is vice president of engineering/Milwaukee plant manager at Milwaukee Electronics (milwaukeeelectronics.com); chanson@milwaukeeelectronics.com.

MES-Based PROCESS CONTROL of Test Machines Using IPC-CFX

Lights-out manufacturing mandates a standard communication protocol. **by RANKO VUJOSEVIC, PH.D., and MATTHEW FISCHER**

Electronics assemblers often assume an MES solution is all they need to gain complete control of all processes and traceability for SMT, manual assembly, box build, test, and rework processes. But even if an MES solution provides interfaces to a wide range of equipment, the plant needs to purchase interface options for the equipment. Often, the investment is so large, they choose not to do it. A vendor's proprietary interface to control and collect data from their machine in real-time can cost up to $5,000/machine. For a plant with 50 machines that need such interfaces, that is a significant investment that often exceeds the cost of the entire MES solution.

For companies that develop and sell MES, developing proprietary machine interfaces is a major resource, cost and time expense. Doing so involves constant updates and attempts to work with companies that often perceive MES vendors as competitors and are not willing to share interface information and data. Electronics manufacturers evaluate machines more and more on the type of communication interface they provide and their additional cost, and often buy machines from vendors that do not charge extra for communication interfaces. A standard interface always has been needed. Attempts to create one failed because of shortsighted interests of equipment vendors and a misunderstanding of the benefits to be gained from a standard interface.

The IPC-CFX standard aims to provide interconnection between equipment and systems and to simplify and lower the cost of Industry 4.0 implementations. It is not our goal to introduce the IPC-CFX standard here. For a good overview of the standard and possible applications, see Ford.[1]

An industry-wide implementation of IPC-CFX on machines, manufacturing execution systems, and ERP systems would benefit:

- Electronics manufacturers, for whom it would simplify and reduce the cost of Factory 4.0 integration projects. Companies could select equipment based on its process capabilities and not worry about how it will integrate with other equipment and systems. Replacing equipment in the future will be seamless.
- Equipment vendors, whose customers will demand all equipment is CFX-compliant. The work presented here is the result of a major automotive electronics manufacturer demanding CFX interfaces from its test equipment suppliers. Equipment vendors will not be able to sell unless they provide CFX interfaces.
- MES vendors, which can focus on developing advanced production scheduling and control features, instead of resource-draining proprietary interfaces.

Here, we describe the role and real-life applications of IPC-CFX for control of test processes.

IPC-CFX Applications for Test Process Control

As of this writing, IPC-CFX has not been widely adopted. Outside of a small number of select vendors and multivendor demos at trade shows, very few real-life applications have been implemented. Not many pieces of equipment support CFX on a level needed for real production and Industry 4.0 integration. Here, we discuss integration between test machines and an MES for real-life process control applications. We will use our experience developing CFX-based integration among MES, ICT and AOI to discuss two scenarios:

- The test machine does not support CFX. A CFX adapter middleware is needed to translate messages from machine (formatted in machine native interface) to CFX and from CFX to the machine. Although this provides a standard interface for the MES, especially useful when a company has its own MES, it still requires an interface on the machine side and the development of the CFX adapter.
- The test machine supports CFX. The machines communicate directly to the MES using CFX.

The test process control by an MES can be summarized by the following list of features that must be provided on the test machines:

- Send details of the active recipe when a recipe is activated.
- Receive requests to activate recipes.
- Indicate whether the requested recipe was activated.
- Send the panel barcode when one is scanned.

PCB Chat

Recent Chats:

Audrey McGuckin on corporate talent development strategies

John Davignon on the HDP User Group

Christopher Tang, Ph.D. on supply chain changes in the Covid era

Ted Conrad on the PCB bake/buy decision

upmg.podbean.com

The PCB Podcast

- Wait for permission before running a test.
- Receive an indication of whether permission is granted.
- Display error messages to the user.
- Indicate when the test is completed.
- Provide the test results in machine-readable format.
- Indicate when the panel has left the machine.

The first case, when the test machine does not support CFX, is more complicated. We will describe a real application for MES-based process control of an ICT. We will use the case when the test machine requests permission to perform the test from the MES.

Routing enforcement is a fundamental feature of an MES. A machine can perform an operation only if the MES verifies the correct recipe is loaded and the PCB is supposed to be at that operation; i.e., none of the preceding enforced operations has been skipped, and no defects are still open. The overall system architecture is summarized in **TABLE 1** and illustrated in **FIGURE 1**.

TABLE 1. System Components

Test machine	The machine (e.g., ICT or AOI)
CFX adapter	Module that translates between the machine and CFX network. This module is necessary if the machine does not natively support the CFX standard.
AMQP broker	Part of the CFX network. Its job is to route CFX messages. Most messages go through the AMQP broker, but some bypass it and go directly to the MES or CFX adapter.
MES	MES system that controls the test process

FIGURE 1. System architecture.

Communication between the test machine and the MES proceeds as follows:

Whenever a recipe is activated on the machine, the machine informs the CFX adapter. The CFX adapter relays this information to the MES. The MES stores this information and uses it later for route validation.

When the machine scans a panel/PCB barcode, it sends it to the CFX adapter and waits for permission to continue.

The CFX adapter sends messages to the MES to announce a panel has arrived in the machine and to request permission to run via route validation.

The MES uses information in its data store, including knowledge of the active recipe on the machine, which was announced earlier, to determine whether the panel is ready to be tested. It returns a message indicating the result to the CFX adapter. If the validation failed because the wrong recipe is currently active at the machine, the MES will also send a message to request the correct recipe be activated. The CFX adapter informs the machine the validation failed and requests a specific recipe be activated if the MES requested it.

If the route validation failed, the machine takes appropriate actions to inform the operator and prevent the test from occurring.

If the MES requests a new recipe, the machine attempts to activate that recipe. It informs the CFX adapter whether it can activate the requested recipe. The CFX adapter relays the result of activating the recipe to the MES.

If the machine successfully activates the recipe, the CFX adapter also sends a message to the MES requesting route validation. When it receives a response, it informs the machine whether it may proceed.

If the route validation failed, the machine takes appropriate actions to inform the operator and prevent the test from occurring. At this point, the panel must be removed from the machine.

If the route validation succeeded, the machine begins its test. Meanwhile, the CFX adapter informs the MES the test is starting.

When the test completes, the machine informs the CFX adapter. The CFX adapter then reads the test results from the machine (e.g., from XML files or a database) and sends them to the MES. It also informs the MES the test has completed.

The CFX adapter requests confirmation from the MES that the test results have been received and are acceptable. The MES gives its response. The CFX adapter informs the machine of the result.

At this point, the CFX adapter informs the MES the panel is leaving the machine.

CFX Messages Implemented

- CFX.Production.RecipeActivated
- CFX.Production.UnitsArrived
- CFX.InformationSystem.UnitValidation.ValidateUnitsRequest (Validation Types: UnitRouteValidation, UnitStatusValidation, and UnitTraceValidation)
- CFX.InformationSystem.UnitValidation.ValidateUnitsResponse
- CFX.Production.ActivateRecipeRequest
- CFX.Production.ActivateRecipeResponse
- CFX.Production.WorkStarted
- CFX.Production.WorkStageStarted
- CFX.Production.TestAndInspection.UnitsTested (ICT) or CFX.Production.TestAndInspection.UnitsInspected (AOI)
- CFX.Production.WorkStageCompleted
- CFX.Production.WorkCompleted
- CFX.Production.UnitsDeparted

FIGURE 2 shows the primary message sequence. All features summarized above for the full control of the test process are implemented in a similar way. If the machine supports CFX, as was the case with an AOI vendor, the CFX adapter is not

continued on pg. 38

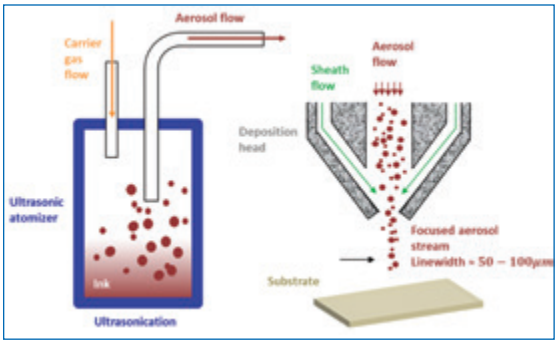
State-of-the-Art Technology Flashes

Updates in silicon and electronics technology.

Ed.: This is a special feature courtesy of Binghamton University.

Photovoltaic cell works at night. University of California researchers have developed a photovoltaic cell that can function at night. The cell can generate up to 50W/sq. m. at night, about 25% of what conventional solar cells generate in daytime. They currently are improving the output power and efficiency of the devices. The cell operates in reverse to a normal solar cell. An object that is hot compared to its surroundings will radiate heat as infrared light. The device can work during the day by blocking direct sunlight. Hence, this new solar cell could potentially operate around the clock. *(IEEC file #11548, Science Daily, 1/29/20)*

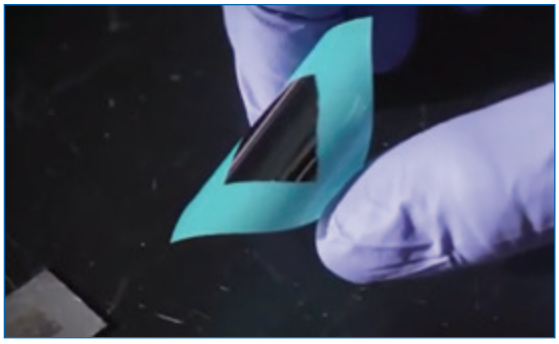
"Stretchy battery" for wearables. Researchers at Stanford University have developed a stretchy battery useful for wearable electronics. The battery can be stretched to twice its original length without any power loss. The polymers in lithium-ion batteries that conduct negative ions toward the battery's positive pole are in the form of gels housed in a rigid casing. By providing a power source that could stretch and bend, wearable electronics can be more comfortable. *(IEEC file #11547, Electronics Weekly, 1/29/20)*



"Tattoos" with active electronics. Researchers from Duke University have developed a process to "print" flexible electronic patches with embedded TFTs directly onto the skin. This "print-in-place" technique for electronics can work on delicate surfaces, including paper and human skin. Unlike other printed electronics that require multiple layers supported by special treatment after each layer, this approach is much more direct. The breakthrough could lead to tailored biosensors for biomedical applications, including patient-specific biosensors. *(IEEC file #11551, Electronic Design, 1/31/20)*

Bionic chip to treat chronic diseases. Researchers from the University of Bath have developed the first artificial digital neuron (Bionic Chip) with the aim of restoring lost brain functions by repairing nerve circuits. They plan to use these chips to treat neurodegenerative diseases such as Alzheimer's disease. The electrical properties of biological cells have long been studied to understand intracellular dynamics. The difficulty of measuring microscopic parameters that control the dynamics of ionic currents and the nonlinearity of ionic conductance has so far hindered efforts to construct quantitative computational models. The growing attention to implantable bioelectronics for the treatment of chronic diseases is driving technology toward low-power solid-state analog devices that accurately mimic bio-circuits. Analog asynchronous electronics is the most promising way to integrate raw nerve stimuli instantly, regardless of the size. *(IEEC file #11571, EE Web, 2/6/20)*

CMOS IC integrates quantum dots with conventional electronics. Leti researchers have developed a CMOS IC that integrates quantum dots on conventional electronic devices and elements. The chip was fabricated on a 28nm FD-SOI process, which integrates analog and digital functions. The target applications are instrumentation needs for a quantum accelerator. Beyond the need to obtain reliable, entangled and coherent quantum bits (qubits) on silicon, the goal is ultimately to produce electronics capable of routing numerous signals to address a matrix of several hundred qubits. The results can also be used for non-silicon quantum devices. *(IEEC file #11589, Electronics Weekly, 2/19/20)*



Low-cost manufacturing of flexible electronics using "remote epitaxy." MIT researchers have developed a low-cost process called "remote epitaxy" to manufacture flexible electronics. The process

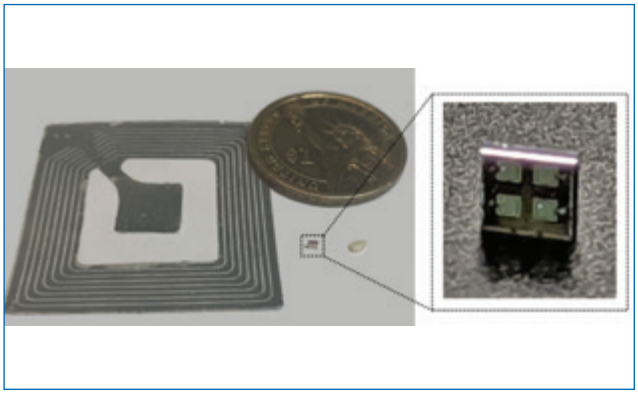
BINGHAMTON UNIVERSITY currently has research thrusts in healthcare/medical electronics; 2.5-D/3-D packaging; power electronics; cyber-secure hardware/software systems; photonics; MEMS; and next-generation networks, computers and communications. The S3IP Center of Excellence is an umbrella organization comprising five constituent research centers.

INTEGRATED ELECTRONICS ENGINEERING CENTER (IEEC) is a New York Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging. Its mission is to provide research into electronics packaging to enhance partners' products, improve reliability and understand why parts fail. More information is available at binghamton.edu/ieec.

involves growing thin films of semiconducting material on a large, thick wafer of the same material that is covered with an intermediate layer of graphene. After manufacturers grow the semiconducting film, they can peel it away from the graphene-covered wafer and then reuse the wafer. Hence, they can copy and peel away any number of thin, flexible semiconducting films, using the same underlying wafer. *(IEEC file #11566, MIT News, 2/5/20)*

3D-printing of perovskite nanostructures. University of Hong Kong researchers have developed a method to print perovskite nanostructures in three dimensions. The method uses a femtoliter meniscus of precursor ink formed on a nanopipette to localize and guide solution-mediated perovskite crystallization in mid-air, enabling nanoscale and freeform 3-D printing. Organic–inorganic metal halide perovskites have emerged as a promising optoelectronic material with exceptional structure and property tunability. This new generation of functional materials possesses excellent properties such as large optical absorption, long carrier diffusion length, high carrier mobility, and a low-cost solution production process. The ability of this method to tailor such nanostructure's dimensions with an on-demand, minimalist manner could contribute to scientific research for fundamentals of perovskite-based material. *(IEEC file #11575, Nanowerk, 2/11/20)*

Stress-relief substrate helps OLED stretch. Researchers from KAIST (Korea Advanced Institute of Science and Technology) have created stretchable, compliant OLEDs that maintain their performance, even under high-strain deformation. The stress-relief substrates utilize pillar arrays to reduce the stress on the active areas of devices. The substrate also has relief island structures that relieve the stress at the bridges in the devices. A patterned upper substrate with bridges makes the rigid substrate stretchable, while the pillars decentralize the stress on the device. *(IEEC file #11608, Science Daily, 2/28/20)*



Battery-free ID chip combats counterfeiting. Researchers at MIT have invented a tiny cryptographic ID tag to verify authenticity in products, including integration into larger silicon chips. The millimeter-sized ID chip integrates a cryptographic processor, an antenna array, and photodiodes for power. Counterfeiting is a huge problem, estimated at $2 trillion worth of counterfeit goods. The new ID tag solves many of the challenges that come with today's wireless ID tags. Examples include RFID tags too large to fit on small products, such as medical components, automotive parts, or silicon chips, with limited security measures. *(IEEC file #11611, Electronics Products, 3/2/20)*

Turning colored pigments into electronics. Queensland University researchers have developed a family of organic pigments set to drive the future of electronic devices. The organic pigments called diketopyrrolopyrrole (DPP) are carbon-based organic materials used for their color as dyes and for their charge transporting and optoelectronic properties. Another class of an orange dye called anthanthrone (ANT) could be used in the future for "perovskite" flexible solar cells built into curtains, sail shades or clothing. One of the advantages of pigments with electronics is they can be printed on a large array of materials, such as materials for solar cells, transistors, and sensors for medical devices inserted in the body to technology products designed to break down. *(IEEC file #11610, Printed Electronics World, 3/4/20)*

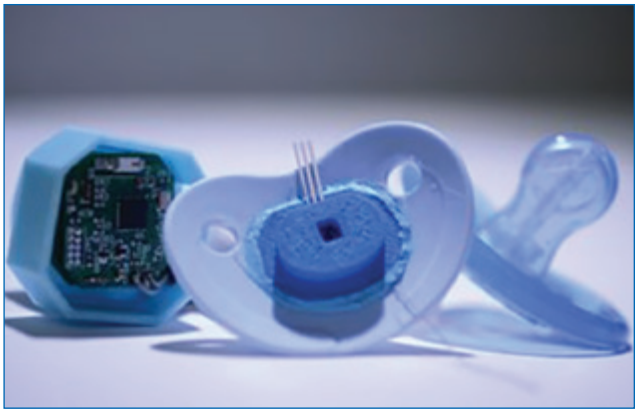
Market Trends

Phase-change and MRAM market forecasts. Market research projects 3-D XPoint (Intel-phase change material) and STT-MRAM (spin-transfer torque MRAM) will lead a $6 billion market for emerging memory technologies in 2025. The NVM (non-volatile memory) market will grow to over $4 billion in 2025. Two key segments will drive it: low-latency storage (enterprise drives) and persistent memory such as NVDIMMs (non-volatile dual inline memory module). The embedded emerging NVM market is projected to grow at a CAGR of 118% between 2019 and 2025 and reach more than $2 billion by 2025. *(IEEC file #11605, Electronics Weekly, 2/27/20)*

Printed sensor market forecast. The printed sensor market is projected at $8.63 billion at a CAGR of 6.62% during the period of 2020 to 2025. Printable sensors are a low-cost alternative to the silicon sensors due to the increasing demand application areas for flexible, stretchable, mass-manufacturable, and versatile printed sensors. Europe is the largest market for printed electronic sensors owing to increasing demand for medical industry printed technology. Adding to demand is the growing development toward human-machine interface, nano-dimension materials, and point-of-care devices. *(IEEC file #11564, Research and Markets, 2/4/20)*

Pacifier to monitor infant health. University of Alcalá and University of California researchers have created a sensor for baby pacifiers. The prototype is made to test glucose levels. The sensor and electronics are kept on the outside of the pacifier, so there's no risk to the baby or sensor. A small channel in the nipple collects saliva and gets pumped up to the glucose sensor. To prevent the saliva from reentering the baby's mouth, plastic valves keep the flow unidirectional. Other metabolic diseases such as phenylketonuria and tyrosinemia can be

monitored as well. *(IEEC file #11611, Mechanical Engineering, 3/3/20)*



Biometrics market to exceed $37.2 billion by 2024. The global biometrics market was $16.7 billion in 2018 and is projected to exceed $37.2 billion by 2024, a CAGR of 14% from 2019-2024. Biometrics refers to a technological authentication method utilized in information assurance for secure entry, data or access. It relies on scanning physical or biological characteristics, such as the face, DNA, fingerprint, iris, retina, etc., which are difficult to forge. It provides more accurate identification and lowers the risk of unwanted intrusion. As a result, biometrics technologies are widely used in schools, colleges, banks, public libraries, corporate and government offices, and consumer electronics including smartphones and tablets. *(IEEC file #11618, Global SMT & Packaging, 2/26/20)*

Recent Patents

Semiconductor device assembly with pillar array (assignee: Micron Technology), patent no. 15/830,839. A semiconductor device assembly and method of forming a semiconductor device assembly includes a first substrate, a second substrate disposed over the first substrate, at least one interconnect between the substrates, and at least one pillar extending from the bottom surface of the first substrate. The pillar is electrically connected to the interconnect and is located adjacent to a side of the first substrate. The pillar is formed by filling a via through the substrate with a conductive material. The first substrate may include an array of pillars extending from the bottom surface adjacent to a side of the substrate that is formed from a plurality of filled vias.

PCB that provides a direct thermal path between components and a thermal layer (assignee: Adura LED Solutions), Pub. no. US10531556. A method of assembling a component to a printed circuit board that includes a thermal layer and a circuit layer separated by a dielectric layer. The circuit layer includes circuit pads that correspond to terminal surfaces on the component. The dielectric layer includes an aperture that exposes a portion of the thermal layer that corresponds to a thermal pad on the component. Solder paste is applied to the circuit pads and the exposed thermal layer. Lower surfaces of the solder paste are in contact with the circuit pads, and the thermal layer and upper surfaces of the solder paste are substantially coplanar. The component is placed on the solder paste.

Heat-activated conductive spinel materials for PCB via overcurrent protection (assignee: IBM Corp.), patent no. 10,531,562. A process of utilizing a heat-activated conductive spinel material for PCB via overcurrent protection includes forming a PCB laminate structure that includes a spinel-doped insulator layer having a heat-activated conductive spinel material incorporated into a dielectric material as a spinel-based electrically non-conductive metal oxide. A sensing via is formed in the PCB laminate structure at a location that is proximate to a power via in the PCB laminate structure. The sensing via is electrically isolated from the power via by a region of the spinel-doped insulator layer and is electrically connected to a monitoring component configured to detect current flow through the sensing via.

Methods of forming a vertical semiconductor diode using an engineered substrate (assignee: QROMIS Inc.), patent no. 10,535,547. A semiconductor diode includes an engineered substrate, including a substantially single crystal layer, a buffer layer coupled to the substantially single crystal layer, and a semi-insulating layer coupled to the buffer layer. The semiconductor diode also includes a first N-type gallium nitride layer coupled to the semi-insulating layer and a second N-type gallium nitride layer coupled to the first N-type gallium nitride layer. The first N-type gallium nitride layer has a first doping concentration, and the second N-type gallium nitride layer has a second doping concentration less than the first doping concentration. ▫

Lean and Covid-19 Supply-Chain Challenges

System strategies and the visual factory can handle rapid changes in demand.

SUPPLY-CHAIN DISRUPTION and Lean philosophy rarely go hand-in-hand. In some cases, however, systems created to support Lean manufacturing or principles themselves help mitigate the chaos the pandemic has created in the global supply chain.

SigmaTron has operations in the US, Mexico, China and Vietnam. As a result, we had a bird's-eye view of the initial impact on manufacturing operations in China and used that as a roadmap for preparing operations in other locations for disruption, along with best in-plant practices for disease mitigation. While the ways different jurisdictions reacted to Covid-19 varied, the issues were somewhat similar. This column looks at some lessons learned in that process from this contract manufacturer's perspective.

There was a four-to-eight week gap in component supplies from China due to the national shutdown in late January/early February. But, the combination of inventory produced/stored in anticipation of the normal Lunar New Year shutdown, combined with decreased demand as the virus disrupted production outside of China, enabled most China component manufacturers to catch up. Consequently, the shortages present in previous unanticipated supply disruptions were not as severe this time. That said, some spot shortages are developing as the US Defense Production Act constrains components needed for essential products such as ventilators.

Issues also arose with trans-Pacific shipments, as the combination of shutdowns and reduced demand/travel impacted shipping and air freight. This is an area where Lean philosophy has a solution. We chose to ship freight less-than-load (LTL) in both directions as soon as parts became available, rather than consolidating in large shipping containers. Reducing shipment "lot size" eliminated bottlenecks taking place at most freight forwarders that were consolidating shipments into large container loads.

Visibility became critical as multiple variables were changing simultaneously. While we build several products deemed essential in all locations, some had temporary factory shutdowns as local governments issued blanket stay-at-home orders, which were then modified for essential product manufacturing. Most of these orders were put in place with little or no warning, and suppliers needed to be notified immediately to hold in-bound freight while the facility's essential production status was appealed. Some customers reduced demand based on trends in their industries, and production was put on hold for products deemed nonessential. Material associated with those orders needed to be addressed. Finally, some customers saw increases in demand for essential products, necessitating increases in incoming raw material.

Just as visual factory techniques help personnel on the factory floor better understand bottlenecks in production driven by unanticipated variation, systems strategy is integral to mitigating the impact of this level of demand variation.

SigmaTron uses a combination of proprietary and internally developed systems for enterprise and shop floor management. All facilities utilize a common ERP system, plus third-party product lifecycle management (PLM) tools. An internally developed manufacturing execution system (MES) supports traceability and enforced routing.

The combination of an industry-standard ERP software with an internally developed suite of supply-chain management tools enables all stakeholders to track demand, material on order, inventory, work-in-process, finished goods and shipments. An MRP share program provides suppliers with complete customer forecast visibility, plus current inventory and material on order. When customers began to process pushouts with SigmaTron, our team could see that in our system and adjust the schedule with suppliers immediately. Additionally, the system highlighted any shortages in raw material for essential production that wasn't being pushed out.

Customers had visibility into inventory status via a customer portal that includes:

- The ability to track product through the manufacturing process, with order, manufacturing and shipping status available 24/7
- Real-time data that show changes as they happen
- Direct email links to the program manager
- All details of shipped orders with a single click.

This level of visibility enabled customers to integrate real-time product status into their inventory planning.

Kanban stocking strategies also played a role. In the case of one customer with an essential product whose demand unexpectedly tripled, a stocking program designed to keep a combination of one month's worth of raw material and two months' worth of finished goods inventory helped fill the pipeline. The one gating item was an LCD display. Although the customer thought they had followed the best practice of specifying multiple manufacturers for this item into their approved materials list (AML), it turned out one factory was supplying under its name, plus providing subcontracted units to the other two named suppliers. SigmaTron's purchasing office in Taiwan used its relationships to convince the supplier to deliver the bulk

JOHN SHEEHAN
is vice president – director of materials and supply chain at SigmaTron International (sigmatronintl); john.sheehan@sigmatronintl.com.

of the required sub assemblies a month earlier than they were originally willing to commit to. The available inventory in the stocking program helped mitigate what otherwise could have been a significant shortfall as this shortage was addressed.

Another area where Kanban played a role was temporary facility closures. As various regions saw Covid-19 infections increasing, program managers were able to contact customers with essential products to determine if they wanted to take early delivery of consigned finished goods inventory to avoid any delays should a warehouse be shut down on short notice. This ability to pull in inventory enabled customers to eliminate the risk that a short notice shutdown or trucking disruption would lock down their product.

One other area where Lean principles ultimately came into play is workforce safety. The company's facility in Suzhou was the first to shut down and restart during China's infection. In restarting factories, Chinese inspectors did a good job of sharing best practices for mitigating infection as they inspected different factories. The result was a more robust process for all factories. While each of SigmaTron's factories complies with the regulations in the area in which it operates, its China facility held weekly and later daily conference calls discussing which core best practices it felt should be standardized and implemented as core practices throughout the company. Examples included employee temperature screening, cardboard dividers between workstations (later replaced with plexiglass as that became available), a mask sterilization process that increased disposable mask life when supplies were limited, frequent use of hand sanitizers and soap, and social distancing for meals/breaks through an increase in staggered break times to reduce headcount in break areas at any one time. Employees were also allowed to make their own washable masks following CDC guidelines. By sharing the lessons learned by the China facility, other facilities were able to be ready ahead of infections utilizing practices developed in a facility that has had zero Covid-19 cases.

The Covid-19 pandemic created unprecedented disruption. However, in SigmaTron's case the foundation laid in support of Lean manufacturing philosophy has provided tools for navigating this chaos. It is also important to note the willingness of customers and suppliers to pull together and work through challenges that are not well covered contractually has made solutions possible. ▫

Machine Interfaces, continued from pg. 38

needed, and the machine itself sends CFX messages to the MES via the AMQP broker.

Conclusions

Historically, electronics manufacturing has not been successful in achieving and sustaining a standard communication protocol between machine and software systems. For lights-out electronics manufacturing without operators, it is absolutely necessary. The IPC-CFX standard is needed for machine-to-machine and machine-to-software systems communication. Most vendors and customers still don't know what to do with CFX. The success of its implementation for Factory 4.0 integration will depend on the level of pressure the largest manufacturers apply toward equipment vendors to provide CFX support. We are witnessing the beginning of such demand, and we hope that will intensify soon. All factors in factory automation: companies, vendors and software providers will benefit from a wide and successful CFX adoption and implementation.

More specifically, we expect the process (routing) control in the future will be performed by equipment itself through machine-to-machine communication, provided by CFX. We need support from equipment vendors to achieve that goal. ▫

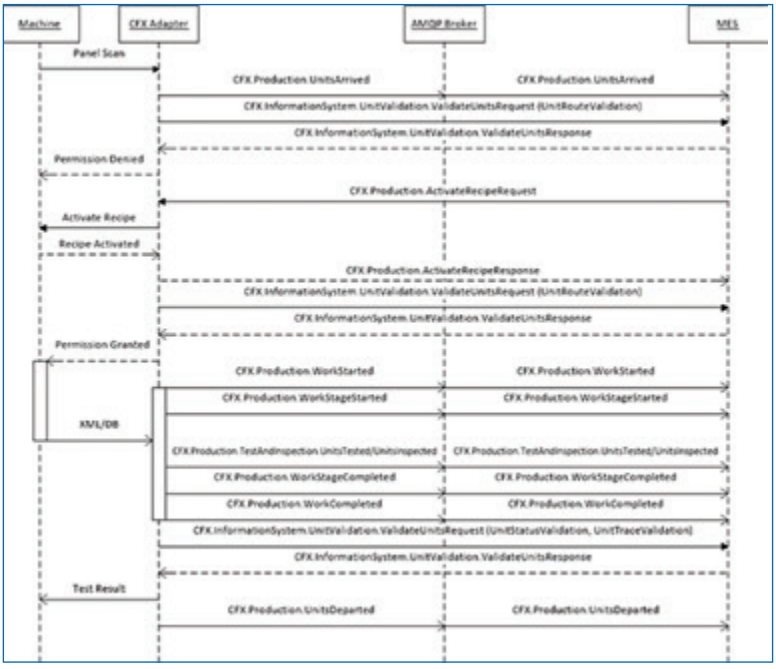


FIGURE 2. Sequence diagram for requesting permission to test.

REFERENCES

1. Michael Ford, "How Do I Get Smart with IPC CFX? (Part 1 and Part 2)," SMT Interconnect 007, July 2019.

RANKO VUJOSEVIC, Ph.D., is CEO of Optel Software (optelco.com); ranko@optelco.com. **MATTHEW FISCHER** is senior software engineer at Optel.

SMTA International

September 27 - October 1, 2020
Donald E. Stephens Convention Center
Rosemont, IL, USA

VISION | INNOVATION | CLARITY

Time to Reconnect

clar-i-ty

/ˈklerədē/ - noun

1. the quality of being coherent and easy to see.
   "You will experience clarity of solutions at SMTAI 2020."

2. the quality of being transparent.
   "The industry needs clarity now more than ever before."

Experience Clarity at SMTA International

smta.org/smtai

Why Was My PCB Job Put on Hold?

A walkthrough shows why you can't "guess" success.

WHEN A CUSTOMER learns their much-needed PCB job has inexplicably gone into the dreaded "hold" basket, the instinctive response is indignation. Let's take a moment to examine the possible reasons. After all, the fabricator doesn't want an unhappy customer, nor a pause in work volume. Yet, a great deal of precise data is needed to build a printed circuit board. As layer count and complexity increase, so does the volume of correct information needed by the fabricator to properly manufacture the job. If some necessary data are missing, the CAM operator will hand the file back to sales to sort out the problems.

The one steadfast rule all PCB manufacturing facilities hold dear is "we don't guess." Never. Break that rule and the consequences will bite back hard. To ensure no one is guessing, every question must be answered. If you failed to specify a tolerance on a set of holes, the job will go on temporary hold until the CAM operator can get a suitable answer. If you have an electrical short between ground power layers due to a misplaced via, the job goes back to sales to sort out. When a job is on hold for a serious problem, the result can be days of delay. If there are one or two small issues, however, in many instances the CAM operator or sales will call and sort it out. They might be able to move a trace or two to prevent a short, for example, or change a pad size to correct a problem with an annual ring that is too small. However, the CAM operator must meet a quota of jobs each day to keep the manufacturing facility fully loaded. They do not have an abundance of time to fix a multitude of problems in an individual customer's data. Other jobs are waiting! In that case, the CAM operator hands the file back to sales to reject the data. The customer can then fix it and resubmit it through the whole process of price quote, DRC (design rule check) and setup.

As printed circuit requirements become more complex, missing information and technical items become even more important. A common customer error is to specify an impedance that cannot be met due to the laminate thickness or Dk.

What other kinds of mistakes are we talking about? What are some of the common mistakes that cause jobs to go on hold? Here is a short list:

- Missing data; e.g., a drill file
- Solder mask or nomenclature white marking file not in the CAD package (very common)
- Missing or wrong information on drawing of outside dimensions
- Missing specifications of laminate in hole plating and surface finishes (very common)
- Shorts or space violations in trace spacing (difficult for the CAM engineer to fix easily)
- Hole size relative to pad size too small, violating clearance spacing between pads
- No specification for laminate (typically, nothing or just FR-4-specified, whereas a fabricator may carry literally hundreds of different types of laminates)
- Spacing violations of clearance of solder mask around pads (common)
- White identification nomenclature marking across pads (all the time)
- Improper sequence of drilled holes in a buried via multilayer
- Hole sizes too small or too large relative to pad size ring requirements (common)
- Through-via holes short out ground planes to power planes (a popular one)
- Specifying a square inside corner in final routing (the fabricator may only have round router bits).

These items, and many others, can put a job on hold. Then the emails fly! But in truth, this isn't a rant about customer mistakes. (We love our customers!) Rather, it emphasizes the importance of working closely with the fabricator. Keep communication open and detail-oriented.

In an actual example, one customer seemed to always be in the "rejected-on hold" bin at the sales desk. After a stressful initial meeting, they asked why their boards were always on hold at our facility and yet another board shop just simply built them. Our engineering team walked through what was missing on the drawing package. One observation was PCBs bought from various manufacturers performed in different ways. Because their specification sheet was so lacking, the other printed circuit manufacturers gave them different laminates they had in excess in stock. Different plating thicknesses were produced because they were not specified, and different solder masks were used. These are small changes a printed circuit manufacturer can make if not specified. During the lengthy meeting, it was illustrated to the buyers and designers that a simple change in laminate, solder mask, and plating thickness could change the impedance by a considerable degree. They agreed to specify a laminate that had a stable supplier known for consistent quality on the manufacturing drawing. The CAD manager showed them how a change in specified plating thickness would affect their yield and future reliability, and if they specified a minimum plating thickness of 1.2 mils copper in the hole, it would greatly improve yields out of wave soldering

AKBER ROY
("Roy") is chief executive officer of Rush PCB Inc., a printed circuit design, fabrication and assembly company (rushpcb.com); roy@rushpcb.com.

and increase thermal cycling life. This alone, hopefully, would solve one of their major problems. As the meeting progressed, we asked for well over 20 additions and changes to the technical specifications of the build sheet and for them to add more technical data to their technical drawings to ensure a tighter set of specifications.

Our plant manager then took them on a tour of the facility and showed why we don't guess. They were shown the lamination storage area, with hundreds of different laminate types, each with 20 different thicknesses and copper weights. During the show-and-tell tour of the rest of the facility, the engineers and buyers witnessed many ways to build the same product. It was an eye-opener. From that point, they understood why so many tight specifications are needed when a critical board is required, and the need to provide such a large volume of information. Subsequent orders never saw the dreaded hold basket. Communication is key, because, in the end, the customer and fabricator are really partners in achieving a successful build, solid product, and fostering a long-term mutually beneficial relationship. ▫

PCB Layout, continued from pg. 29

F. Does differential trace separation need to be constant? *If*, under (E), differential impedance design rules need to be followed, trace separation needs to be constant. The reason is the differential impedance must be constant to prevent reflections at impedance discontinuities. (Or, trace geometries must be modified where the trace separation changes.)

So, the question of whether we need differential design rules depends very much on several conditions. As a way of trying to summarize those, I offer the following.

These differential design rules:

A. Equal trace length
B. Planes underneath differential traces
C. Traces routed close together
D. Controlled impedance design rules
E. Differential impedance design rules
F. Equal trace spacing may apply, depending on our signal integrity concerns. ▫

REFERENCES

1. Douglas G. Brooks, *PCB Currents: How They Flow; How They React,* Prentice Hall, 2013, p. 287. Differential signal and design rules are described in Chapters 12 and 22.

DOUGLAS BROOKS, PH.D., has a master's in electrical engineering from Stanford and a Ph.D. from the University of Washington. For the past 27 years he has owned a small engineering service firm (ultracad.com) and written two books and numerous technical articles on printed circuit board design and signal integrity. He published *PCB Trace and Via Temperatures: The Complete Analysis, 2nd Edition,* with Johannes Adam in 2017.

NEPCON MICROELECTRONICS ASIA
亚洲电子生产设备暨微电子工业展览会

NEPCON ONLINE Electronics Exhibition

2020.8.26-28 | SHENZHEN CONVENTION & EXHIBITION CENTER

ORGANISED BY:

CCPIT Electronics&Information Industry Sub-council
中国国际贸易促进委员会电子信息行业分会

Reed Exhibitions®
励展博览集团

Just simply scan the QR code to do pre-registration.

A Sudden Captive's Journal

So rampant was coronavirus, it even infected accounting systems.

DAY 1: Today the authorities announced local shelter-in-place restrictions. All employees of nonessential businesses must stay home or be subject to fines if caught at the workplace. What to do? Set priorities: define whether we are essential and be prepared to back it up if we are. There is no Essential Business Department in California, like the DMV, to which one can apply and get a Certification of Essentiality. No tests one takes. It depends on one's OEM customers and flows down to their suppliers. For those of us not named Elon Musk, we are not a law unto ourselves.

Day 2: Met with the crew. Game plan time. Henceforth, the old guys (the "over 60s") will stay home. That includes (gulp) me. Aging and mortality in one poignant bite. A small crew will remain at our facility, handling day-to-day essential business. (In the preceding 24 hours, we established our corporate essential bonafides.) Headcount will fluctuate daily, depending on happenings. Some will stay home today; others will do likewise tomorrow. I stay home every day pondering the Darwinian way of the world, and my humbling new lot in life as a high medical risk individual. Regardless of work site, all employees will continue to be paid for the foreseeable future. As if we can foresee it. No one will burn PTO if they must stay home. Engineering work will be conducted from home to the extent possible. No onsite customer visits will be allowed until further notice. Living a paradox: keeping it all together, while dispersed. Here we are.

Day 3: To document our essential designation, we set up a logbook. We may need to prove it one day to somebody wearing a badge and a sidearm. Best to be prepared. The book contains letters from OEM and EMS customers, affirming the Federal Government considers them to be essential – and therefore so are we. Pride of place in the book goes to those letters addressed directly to us. (They value us! They really, really value us!) It's the little things that perk one up and put a spring in one's step during a plague.

Day 5: Our nation has been impacted by an economic asteroid. Where traffic jams proliferated a week ago, the freeways are now empty. At certain times, a thrill-seeking pedestrian could saunter across the 280 Freeway on the San Francisco Peninsula – where 80mph is the unpoliced norm – and not get hit. I am not exaggerating. This may be teeming, industrious Silicon Valley, but the dearth of vehicles suggests it contains many people who can work, or attempt work, at home. Traffic density doesn't lie.

Day 6: War footing. Ordered extra masks and (lucky us!) hand sanitizer. Fortunately, our janitorial service has us well-stocked with toilet paper and paper towels. The Quartermaster Corps has nothing on us. Should amoebic dysentery show up, we are ready.

Day 8: Evidence abounds that stupidity is not sheltering in place and lacks a vaccine. Super-spreaders are everywhere: customers pushing their imagined entitlement and jostling for their assumed rightful place in the flying probe queue. Many are waving readily marketable and useful acronyms, like DPAS. Someone has them convinced it is DoD-speak for cudgel. As in browbeat your supplier within an inch of their contractual life. Or cut to the head of the line. Opportunism is like slime: it flows wherever gravity and low resistance permit it.

Day 11: A customer today tried to use his DPAS rating to skip over other worthy, qualified clients that were there before him. His righteous lectures about privileged placement are worthless. You can't push the flying probe onto an incline to speed it up by gravity. Get in line and take a number. In his case, number 12. Some are more DPAS'd than others. Let the DoD sort 'em out and learn your lesson.

Day 12: Trade shows are vaporizing. Everything prior to Jul. 1 has been either cancelled or postponed to the fourth quarter. Our travel expenses have gone from substantial to nearly zero in the space of two weeks.

Day 13: Today we were flattered with a "Dear Trusted Supplier Partner" letter. In it the esteemed client thanked us for our efforts and sacrifices, then segued nicely into the hammer: an imposition of yet another effort and sacrifice; effective immediately all invoices would be paid in 60 days, due to the situation with Covid-19. Dr. Fauci never mentioned the virus infected accounting systems. As with humans, there appears to be no known cure other than patience and social distancing from one's accounts receivable. Don't bother to protest because no one will answer. Naturally, no mention was made in the letter about this client's history of ignoring stated terms, going back long before most of us knew the definition of "pandemic." Covid conveniently masks a preexisting condition.

ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.

Day 16: County Health Department publishes protocols for safe operation and social distancing at essential businesses. We conduct awareness training for all staff and post copies of the county protocols at the front and back doors, next to our new hand sanitizer dispensers. Several suppliers request copies of our protocols prior to sending service technicians to us. Several ask multiple times; the pandemic has made them forgetful. They are large, not especially common sense-burdened companies. They know who they are.

Day 19: Time to shift from passive to active when it comes to videoconferencing. Bought Zoom subscription and we're prepared to use it. Yikes! Now we're part of the problem.

Day 20: What is so hard to learn about mute buttons? No, we don't want to hear your dog barking or your kid screaming during our contract negotiation. The button is big and red when off, and big and green when on. Just like a Fisher Price toy from childhood, the screen draws wholesome memories. For ease of use! So all of us three-year-olds can do this!

Day 25: Received an earnest inquiry from a service that helpfully offers to provide attendee lists from the SMTA Dallas Expo. The service will gladly furnish thousands of "sales leads" on its proprietary list. Properly vetted, sanitized, and socially distanced. Thousands of P.O.-ready names attending a tabletop show with 50 to 60 tables. One inconvenient problem: the show was postponed because of the pandemic. But they still have a list.

FIGURE 1. All the sanitizer in the world might not clean this mess.

Day 31: Received a query from a customer that wishes to flying probe-test 2,000 boards per week. Consumer product. Wants to start immediately, as in next week. No problem. Sent them an email asking that they document their essential status. Nothing but the sound of crickets chirping.

Day 35: A guy calls wanting CT-scanning of musical instruments. Customer wants to create a digital archive of an entire orchestra. Can do. First, he wants to prove our capabilities by means of a test case. French horn. Piece of cake. Free, naturally, is his expectation. Having some digestion problems with that piece of cake. We do it anyway, in our downtime.

Day 41: Received my fifth webinar invitation of the day. It followed my third daily sales pitch from a Chinese circuit board fabricator. So much flattering attention. So much useless, time-filling noise. Everybody is so caring and concerned. Send your dollars to C.A.R.E.

Day 48: French Horn Man is anxious for his images. He lectures me about deadlines. Indignation compels me to remind him that his product is not exactly, ahem, essential; that we're doing it for free; and we insert his project discreetly and as time permits around somewhat more pressing aerospace and medical life support projects. He is not-so-subtly urged to count his blessings that we make time available for him in the first place. He gets quiet. He should get quiet.

Day 53: We send French Horn Man a set of sample images. He's ecstatic, in an intensely self-regulating, classical music kind of way (stiff upper lip). We are thanked for our time and effort and off he happily departs. Despite several follow-up emails, we never hear from him again.

Day 57: Videoconference with a medical instrument EMS customer to go over gage R&R results from preliminary x-ray inspection. They made the mistake of inviting their OEM to the meeting, who promptly hijacks it, questioning every measurement and the premise behind each one. Which is perplexing, considering the OEM wrote the spec we measure to, which this engineer clearly had not read. At minute 90 of a 30-minute meeting, I pull the ripcord and bail out. Something about another Zoom meeting with the mother ship, or the pending apocalypse, or something more important. We clearly aren't charging enough.

Day 64: Conference call with a quality engineer from a longstanding aerospace customer. He wants to visit our facility to qualify our x-ray processes, which have been validating and troubleshooting and generally passing judgment on his boards for 11 years. (What took them so long?) He's new, eager to impress by checking his boxes, and needs to be brought up to speed by his colleagues. After the conference call, we never hear from him again either. All is well.

Day 69: Personal facial hair running riot. The 1880s pioneers (you know, the ones in the tintype pictures with their stout prairie wives and 14 equally stout, sullen children, not counting the four lost in childbirth) have nothing on my beard. Gonna need a machete to hack through the facial underbrush when the time comes to look respectable again. Avoid melted cheese. Meanwhile I'll channel Father Time on Zoom and

continued on pg. 44

Component Body Lifting

Get the right stencil for the job.

BOB WILLIS
is a process engineering consultant; bob@bobwillis.co.uk. His column appears monthly.

THIS MONTH WE illustrate an example of what appears at first glance to be poor lead solderability. When examined, however, it is a combination of component and pad design.

FIGURE 1 shows the lead to be floating in the solder joint, suggesting poor wetting. When we examine the component lead and plastic body, however, the lead is not parallel, so it always sits off the pad surface, even if perfectly soldered. The lead sits in a cavity in the component body to maintain its position. But with the size of the pad used in the design and a full solder paste print, the component body will always lift.

To improve the component, the position of the pin should be parallel with the body. Ideally the opening of the body of the lead should be wider or angled to permit solder to wet without lifting the part. A simple shop-floor fix is to order another stencil and reduce the width of the paste print, decreasing the lift during reflow.

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at youtube.com/user/mrbobwillis. ▫

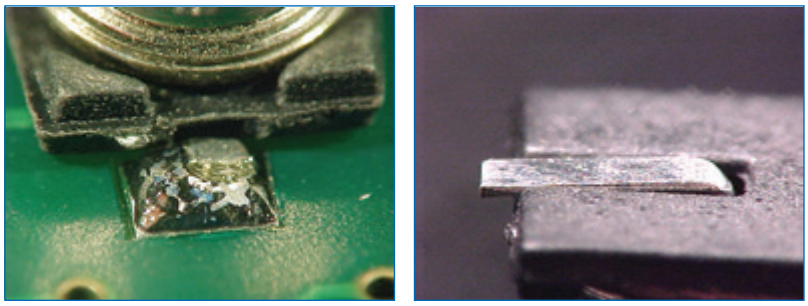


FIGURE 1. The lead at left appears to show poor wetting, but the pad design is such that the pin is not parallel to the component body.

Seeing is Believing, continued from pg. 43

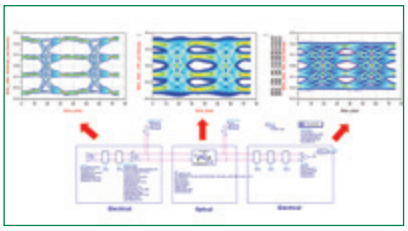
look inscrutable behind the white-haired façade. Kind of the low-rent wise man look, sans wisdom.

Day 71: Protests going on throughout our area. Justified but scary at the same time. Hope they don't metastasize into something worse. We reap what we sow. In management school, they don't teach overcoming pandemics, economic calamity, and civil unrest simultaneously. No textbook for this.

Day 77: The world is emerging from its cocoon. Just as belligerent as the world we plunged into 77 days ago. What have we learned? Video technology is now our friend, or at least our constant annoyance. Plus, we now wear masks. And Elon Musk is, well, Elon Musk.

Day 78: As we emerge, it is clear the world most assuredly is not going back to "normal" as we knew it on Feb. 1, 2020. What does it mean? And will the DPAS exemption-wavers stop shouting to move up in line? This has been one extended masterclass in making things up as we go along. Getting all our social ills on the table in one blast. Put that in your Industry 4.0 spreadsheet. Short spurt intensity for which American technologists are uniquely qualified.

And exhausted. ▫



DESIGN PARAMETER SIMULATION

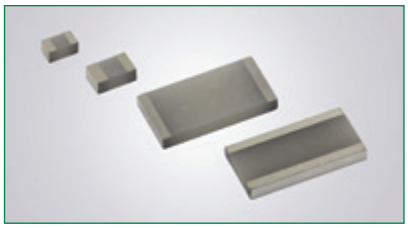
VPI Optical Link simulation workflow capability connects PathWave Advanced Design System with VPI Design Suite from VPIphotonics. Predicts signal integrity of electrical-optical-electrical data links. Simulates and optimizes design parameters concurrently in electrical and optical domains. Investigates electrical channel design, including trace routing and design of PCB vias.

Keysight Technologies
keysight.com

PCB ROUTER

EasyRouter Plug & Play depaneler comes with cables, hoses, instruction video and 10-step setup guide. For offline use. Comes with milling tool featuring speed up to 60mm/s for top routing of PCBs. Electrical fixture ID, detection of correct position before placement on milling fixture pins and automatic bit clamping/unclamping are optional. Optional acquisition system for production and operation data to record depaneling procedures.

IPTE
ipte.com



SMT JUMPER CHIP

ThermaWick THJP thermal jumper chip transfers heat from electrically isolated components by providing a thermal conductive pathway to ground plane or common heatsink. Features aluminum nitride substrate with 170W/m°K thermal conductivity. Reportedly reduces temp. of connected components more than 25%. Capacitance down to 0.07pF. Comes in case sizes from 0603 to 2512.

Vishay Intertechnology
vishay.com

OTHERS OF NOTE

FLAME-RETARDANT PET FILMS

Melinex FR32x clear PET (polyethylene terephthalate) polyester films have achieved UL's VTM-0 flame rating classification and are halogen-free. Provide low haze of approx. 1%. Are produced on large assets with thickness range of 75µm-175µm and roll widths up to 1600mm and beyond. Applications include flexible printed circuitry.

DuPont Teijin Films
dupontteijinfilms.com

FINE-LINE VIA FILL

Microfill EVF-III electroplating is for via fill and through-hole plating for fine-line HDI circuit boards. Provides surface uniformity, reduced scratch mark sensitivity, and wider operation latitude for a reported 20% productivity improvement at up to 20ASF.

DuPont Electronics & Imaging
dupont.com

BTB/BTC SMT CONNECTORS

SMT PCB connectors have horizontal orientation for parallel board-to-board or board-to-component options for power or signal transferring. Low-profile circuit linkage and minimal footprint for high-density, high-current PCB packages on power and aluminum backplanes. Withstand all PCB soldering applications. Tape-and-reel parts packaged per ANSI/EIA-481.

Keystone Electronics
keyelco.com

TIME-TO-FAILURE SOFTWARE

CalceSARA software uses physics-of-failure-based reliability principles to assess time to failure of part/system/failure site. Develops customized test plans and compares competing designs. Identifies failure modes and ranks failures by time to failure under different loading conditions. Evaluates life expectancy of electronics hardware under anticipated lifecycle loads and assesses expected time to failure under elevated stress tests to establish acceleration factors. Uses these simulation results in conjunction with physical test results to confirm failures and assess field reliability. Now free of charge.

CALCE
calce.umd.edu

IC SUBSTRATE RDL BUILDUP

Systek SAP buildup processes for IC substrate RDL have a four-step desmear process that can be calibrated to prepare multiple substrate materials, imparting minimal roughness, while ensuring clean via side walls and copper target pads. Subsequent conditioner process ensures adsorption of palladium catalyst into substrate. Copper metallization process includes ionic palladium activation system, zero-stress electroless copper metallization process, and optional anti-tarnish. Semiadditive processes provide toolset for creating RDL with dimensions down to 5/5µm line/space.

MacDermid Alpha
MacDermidAlpha.com

CERAMIC CAP. FOR 5G

GRM011R60J104M features max. capacitance of 0.1µF in 008004". Features capacitance tolerance of ±20%, usage temp. range of -55° to 85°C, and rated voltage of 6.3Vdc. For devices supporting 5G. Applications include wearables, smartphones, and any electronic device featuring miniaturization and increased functionality. Uses ceramic and electrode material atomization and homogenization technology.

Murata Manufacturing Co.
murata.com

INDUCTIVE SOLDERING STATIONS

GT90 and GT120 use inductive heating technology and have adjustable temperature. GT90 single-port soldering station uses 90W power supply and performance vs. 75-120W systems. Compatible with ultrafine and standard tips. Is for single iron applications on production line. GT120 single-port soldering station uses 120W power supply and reportedly offers performance equivalent to 250W systems. Compatible with ultrafine, standard and high thermal demand tips; is for any single iron soldering application. External power supply.

Metcal

info.okinternational.com/gt90-gt120

3-D SPI

TR7007DQ Plus comes with improved motion controller (EtherCat) and enhanced 2-D light module. Motion controller achieves real-time measurements and processing on the fly, while light module realizes higher uniformity inspection, less shadow, and improved imaging. Inspects low solder bridges and compensate board warpage for eliminating local PCB deformation. Is equipped with up to four projectors to ensure shadow-free inspection. Eases data exchange between production line and MES of choice to enable data traceability for connected factory.

Test Research Inc.

ecd.com tri.com.tw/en

EXPANDABLE PICK-AND-PLACE

Fox2 modular pick-and-place technology is now expandable in any direction. Combines jetting/dispensing, 2.5-D placement, electrical testing, inventory control and traceability. Has machine footprint of under 11 sq. ft. and can accept PCB sizes up to 16" x 12". Components with sizes from 01005 up to 3.15" x 3.15" can be placed. Machine achieves 10,800cph at 50µm with a two-nozzle head. Can be configured with up to 180 feeders. Can be fitted with jet valve for SMD glue or solder paste for manufacturing 2.5-D assemblies or micro-screw valve. Features ePlace software.

Essemtec

essemtec-usa.com

OTHERS OF NOTE

STRETCHABLE CONDUCTIVE INKS

ECI 8000 E&C inks can be processed into surface of automotive interior, making it possible to integrate motion sensors, heating or charging devices directly via smart surface. Can be printed on almost any surface to create uniform, self-regulating heater that will never overheat. Stretchable conductive inks can be thermoformed, matching requirements of in-molded electronics, which are processed in automotive interiors.

Henkel

henkel-northamerica.com

8-ZONE CONVECTION OVEN

GoReflow-plus has active heated area of 2,980mm and soldering in ambient atmospheres or with local nitrogen. High volume of circulated process gas, generated with axial fans and slot nozzles, ensures homogeneous heat distribution over transport width at simultaneously moderate gas velocities; good heat transfer rate is realized, permitting set temperatures of oven at low level. Three-stage cooling area cools assemblies after reflow. Flux management system (process gas cleaning) with stainless steel filter is integrated in peak and cooling area.

Seho

seho.de

BTB STENCIL PRINTER

MPM Momentum II BTB is back-to-back configurable for dual-lane processing without increasing line length. Has larger window and wider access inside printer. Quick-release squeegee requires no tools; takes less than 30 sec. to change blade. Jar or standard cartridge dispenser. Paste temperature and roll height monitors.

ITW EAE

itweae.com

IPA/DI CLEANER

MultiClean MultiTask provides high-purity cleaning in almost any production environment. Cleans work surfaces, including tables, tools, machinery, gauges, keyboards, mobile phones and more. Features 70% high-purity IPA and 30% DI water mixture that evaporates more slowly, permitting cleaning fluid to remain on surfaces longer. Removes flux and white residue from PCBs, solder paste and uncured epoxy residues from stencils, fingerprints, grease and light oils found in medical device and electronics manufacturing. Safe on metals and plastics.

MicroCare

microcare.com

4X VACUUM SOLDERING OVEN

CondensoX-Line Quad Core permits four parallel vacuum soldering processes. Chambers can be operated independently; preventive maintenance can be performed on process chamber without causing line stop. Process chamber is loaded simultaneously on upper transport level. On lower transport level, further assemblies are transported to next available chamber module via independent transport system. Process chambers contain vapor phase process and complete vacuum process. Cycle times range from 12 sec. per unit to 60 sec. per unit, including use of vacuum to reduce product voiding.

Rehm Thermal Systems

rehm-group.com

M0402 SOLDER PASTE

S3X70-G811 type 5 solder paste is for micro-pattern applications that can be reflowed in an air atmosphere. Adopts new flux formulation optimized for type 5 solder powder and enables air reflow soldering of 0402 metric components. Shows meltability and wettability at micro-patterns in air reflow; reduced stencil issues from newly developed lubrication technique; reduced voids with various board surface finish treatments. Good melting properties.

Koki Co.

ko-ki.co.jp

In Case You Missed It

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

Component Technology

"Ultra-High Areal Number Density Solid-State On-Chip Microsupercapacitors via Electrohydrodynamic Jet Printing"

Authors: Kwon-Hyung Lee, Seong-Sun Lee, *et al.*

Abstract: Microsupercapacitors (MSCs) have garnered considerable attention as a promising power source for microelectronics and miniaturized portable/wearable devices. However, their practical application has been hindered by the manufacturing complexity and dimensional limits. The authors developed a new class of ultra-high areal number density solid-state MSCs (UHD SS–MSCs) on a chip via electrohydrodynamic (EHD) jet printing. This is, to the best of their knowledge, the first study to exploit EHD jet printing in MSCs. The activated carbon-based electrode inks are EHD jet-printed, creating interdigitated electrodes with fine feature sizes. Subsequently, a drying-free, ultraviolet-cured solid-state gel electrolyte is introduced to ensure electrochemical isolation between the SS–MSCs, enabling dense SS–MSC integration with on-demand (in-series/in-parallel) cell connection on a chip. The resulting on-chip UHD SS–MSCs exhibit exceptional areal number density [36 unit cells integrated on a chip (area = 8.0mm x 8.2mm), 54.9 cells cm^{-2}] and areal operating voltage (65.9V cm^{-2}). (*Science Advances,* Mar. 6, 2020, advances.sciencemag.org/content/6/10/eaaz1692)

"Non-Reciprocal Electronics Based on Temporal Modulation"

Authors: Aravind Nagulu, Negar Reiskarimian and Harish Krishnaswamy

Abstract: In general, reciprocity requires signals travel in the same manner in both forward and reverse directions. It governs the behavior of most electronic circuits and components, imposing severe restrictions on how they operate. Components that violate reciprocity, such as gyrators, isolators and circulators, are, however, of use in many different electronic applications. Non-reciprocal electronic components have typically been implemented using ferrites, but such magnetic materials cannot be integrated in modern semiconductor fabrication processes, and magnetic non-reciprocal components remain bulky and expensive. Creating non-reciprocal components without the use of magnetic materials has a long history but has recently been reinvigorated due to advancements in semiconductor technology. Here the authors review the development of non-reciprocal devices and the development of non-magnetic non-reciprocal electronics, focusing on devices based on temporal modulation, which arguably exhibit the greatest potential. They consider approaches based on temporal modulation of permittivity and conductivity, as well as hybrid acoustic–electronic components, which have applications including high-power transmitters for communications, simultaneous transmit and receive radars, and full-duplex wireless radios. They also explore superconducting non-reciprocal components based on temporal modulation of permeability for potential applications in quantum computing and consider the key future challenges in the field. (*Nature Electronics,* May 4, 2020; nature.com/articles/s41928-020-0400-5)

Laminates

"Sandwiched Graphene Clad Laminate: A Binder-Free Flexible Printed Circuit Board for 5G Antenna Application"

Authors: Rongguo Song, Xin Zhao, *et al.*

Abstract: Metal substitution has always been the focus of scientific research in printed circuit board (PCB) and 5G communication technology. It has been proved the high thermal conductive carbon-based materials can be potential alternatives. However, the relatively low electrical conductivity and the difficulties in integrating carbon-based materials to functional substrates limit their further and industrial applications. Here, the authors developed a method to fabricate large-scale, binder-free, flexible graphene clad laminate (GCL) by hot pressing assistant under vacuum to achieve excellent electrical properties and well-connected interface for PCB application, thus accomplishing metal substitution. GCL is a sandwich structure constructed of top and bottom layers of high-conductivity graphene-assembled film as conductive layer and a dielectric substrate layer. A 5G millimeter wave antenna array based on GCL PCB operated at 26GHz is designed, fabricated and characterized. The GCL antenna array has a reflection coefficient of -20.98dB and realized gain of 11.05dBi, comparable to the metal antenna array made of commercial copper-clad laminate PCBs. All measurement results show the flexible and lightweight GCL can be used as a new-generation PCB for flexible electronic devices and RF devices. (*Advanced Engineering Materials,* Jun. 5, 2020; https://doi.org/10.1002/adem.202000451)

30 Years of Science and Care.

The right solutions happen when you care enough to ask the right questions.

KYZEN® E5631

Next Generation Stencil Cleaner

At **KYZEN**, we have the **SCIENCE** and expertise to solve any cleaning problem, and the **CARE** to find the perfect solution for your individual cleaning process. When science and care converge, your cleaning process succeeds on every level.

Request expert cleaning advice and technical support at KYZENcares.com!

KYZEN
Where Science and Care Converge.

KYZEN.COM

WORLDWIDE ENVIRONMENTALLY RESPONSIBLE CLEANING TECHNOLOGIES

UPGRADE YOUR KNOWLEDGE

FREE DOWNLOAD

Learn about POWER SUPPLY DESIGN in our latest e-book and view our growing library of resources created by the PCB design experts at EMA Design Automation.

Download the FREE e-book at:
go.ema-eda.com/LearnPowerSupply

EMA Design Automation®