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October 2020

6 Ways to ID Counterfeit Parts

And 1 Question Why We Still Have To

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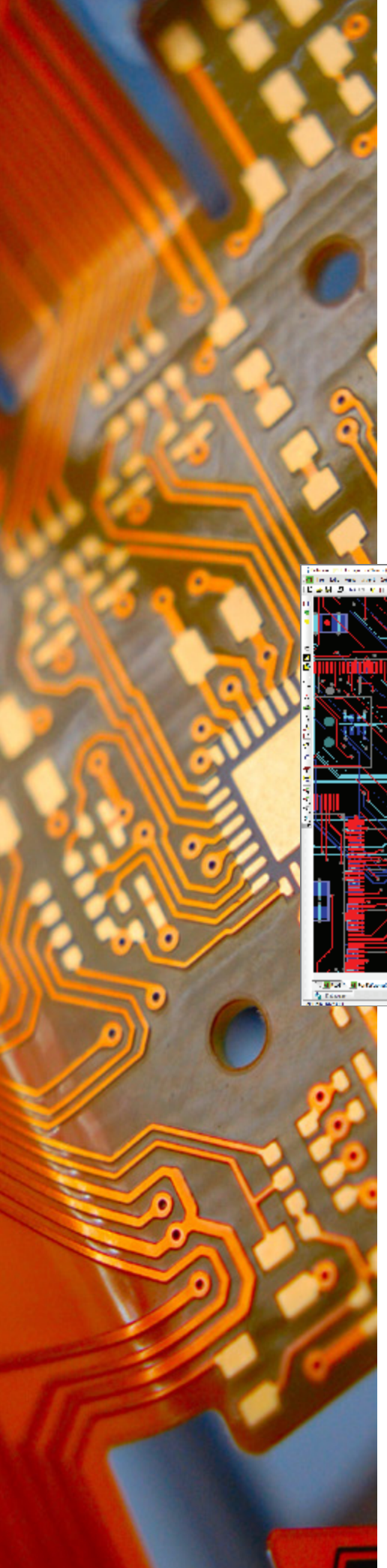
Design for *Rework*

5 Ways to Ensure *Seamless* Program Transfer



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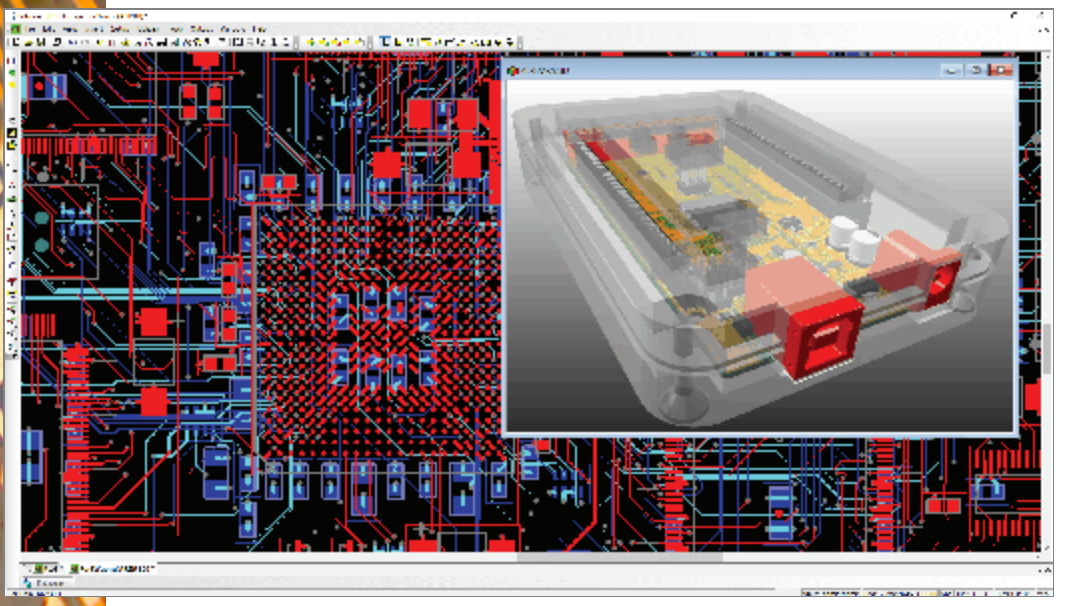

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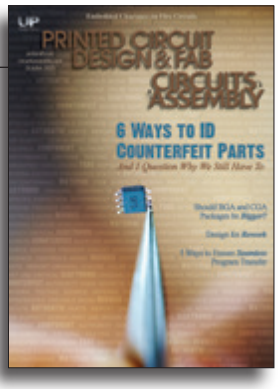
MONEY MATTERS

TECH TALK

DEPARTMENTS

FEATURES



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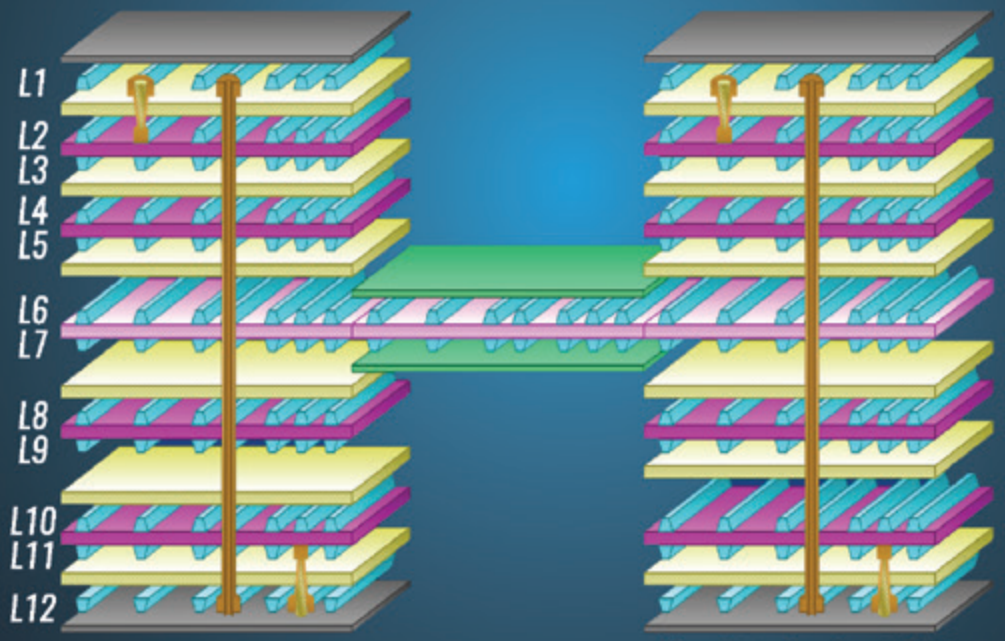

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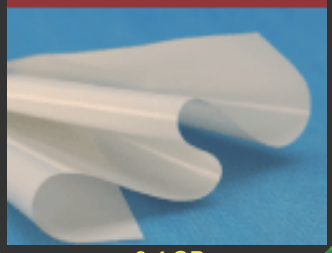

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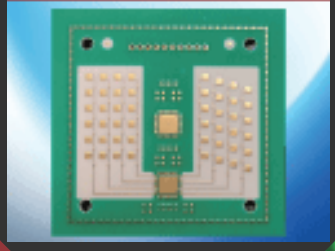

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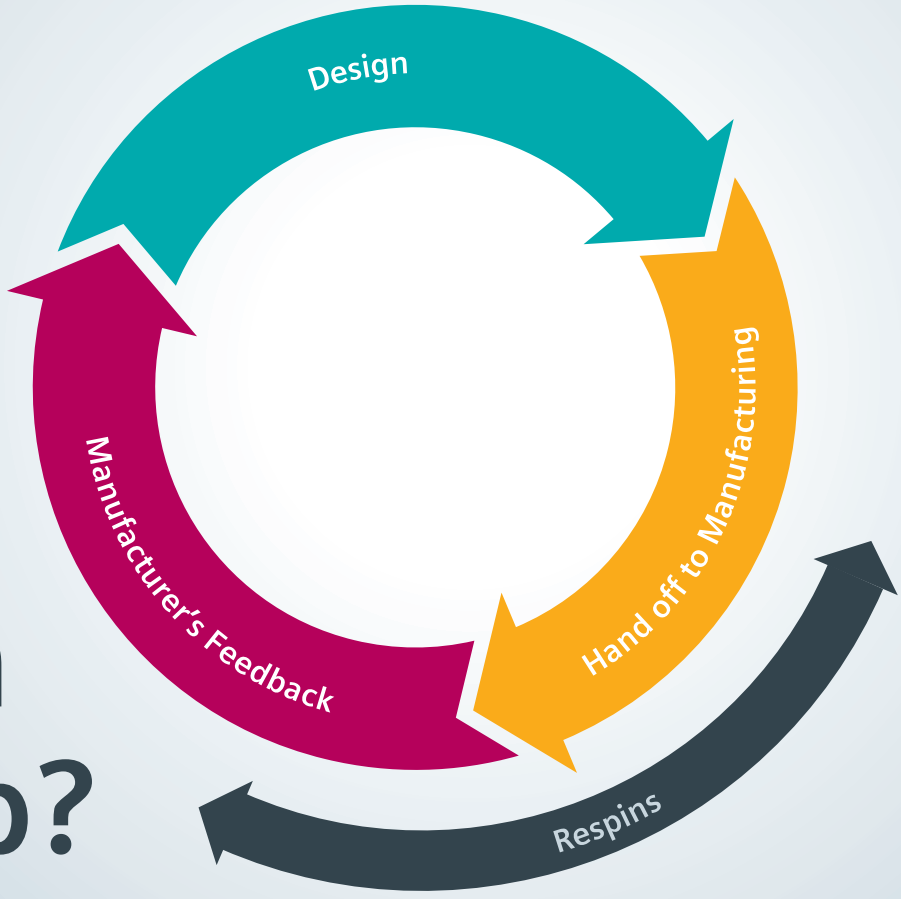

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MIKE BUETOW
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Fake Parts Still a Real Problem

IF THERE IS one takeaway from the Symposium on Counterfeit Parts and Materials sponsored by SMTA and CALCE that took place in August, it is that the problem is getting worse. This should be alarming, given the amount of attention that has been paid to the presence of "fake" parts in the supply chain.

Discussion of counterfeits in the supply chain usually starts with the military. It's the one sector that has both the budget and the concentration of sourcing to effect change.

It was less than a decade ago that the US found fake electronic parts in military aircraft. The discovery spurred a yearlong investigation resulting in bipartisan legislation (remember what that is?) establishing new policies and practices for counterfeit avoidance.

Today, the annual US defense budget bills contain language requiring the Department of Defense, the Department of Homeland Security and their contractors monitor supply-chain risks for counterfeit parts, although previous language requiring buyers to "detect and avoid counterfeit parts in the military supply chain" has been softened.

Still, we've been battling the problem for at least two decades now, yet most experts feel 1) the volume of fake parts has increased, and 2) the counterfeiters are better than ever.

Methods for detecting fake parts over the years have included visual and optical inspection, XRF, chemical or laser etching, and even DNA marking. Our cover story this month centers on MLCCs, whose lack of markings and presentation, the authors note, "give unscrupulous vendors opportunities for fraud." The authors offer electrical (bias) testing, capacitance temperature characteristics, high voltage testing of dielectric withstand voltage and insulation resistance, and electron microscope (EDS) material analysis as possible nondestructive tests for separating authentic from fake.

The latest DoD proposals, submitted in August, focus on the Supplier Performance Risk System (SPRS), essentially an analytical tool for reviewing quality and delivery data from government systems. The proposed policy would tighten language above "item risk" to use SPRS to determine the probability that a product or service, based on intended use, will introduce counterfeit or nonconforming material to the DoD supply chain. In short, the Defense Department wants to continue down its path to basing supplier conformance on empirical data instead of subjective assessments.

There's nothing wrong with modeling risk; we do it all day long. But wouldn't a trusted supply chain, one inherently domestic, be a more predictable and authentic route?

And does Covid-19 pose an opportunity? Most experts finger China (who else?) as the source for the vast majority (70% or more) of counterfeit electronics and related materials. Yet China remains the go-to for electronics materials.

Certainly, while the pandemic has brought about the most drastic global disruptions in memory to the supply chain, regional disruptions are commonplace. A new report from McKinsey Global Institute, the policy arm of the consulting agency, says there's inherent risk on so many depending on so few: "Interconnected supply chains and global flows of data, finance, and people offer more 'surface area' for risk to penetrate, and ripple effects can travel across these network structures rapidly." Their analysis of 37 industries ranks communications equipment as the one most exposed to value chain risks. Computers and electronics are seventh, and semiconductors are tenth. What these sectors' value chains have in common is their high value and relative concentration.

We are all aware how the supply chain became so concentrated in a single geography. The economies of scale only heighten the near-term costs involved in breaking China's grip on the electronics value chain. And it may be a stretch to overlay MGI's research into abrupt disruptions on a chronic pain point like counterfeits.

But the similarities are there. The presence of counterfeit parts is an ongoing disruption to an efficient chain. No one really knows how much is spent in mitigation and field returns, but all agree the figure is huge.

A McKinsey survey of supply chain executives conducted in May found some 93% plan to take steps to make their supply chains more resilient. Steps under consideration include building in redundancy across suppliers, nearshoring, reducing the number of unique parts, and supply chain regionalization.

If we are moving supply chains, we open the door to change. Western governments – and industries – should capitalize on the moment to beef up their local supply chains.

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P.S. The PCB West Virtual 2020 technical conference is available on-demand through the middle of this month. Visit pcbwest.com for access.

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PCDF People

Cadence named **Patrick Davis** product manager director. He has nearly 25 years' experience as a PCB designer and manager with Rocket EMS, Summit Computer and Millennium Design.

PCDF Briefs

Aotco Metal Finishing has acquired **Plating for Electronics,** a provider of specialty anodizing, electroplating, and laser marking services based in Waltham, MA.

All Flex has developed etched foil heaters for medical diagnostics, DNA testing, P.O.C. instruments and cancer diagnostics.

Board Shark PCB hired **ER North** as manufacturers' representative in North Dakota, South Dakota and Minnesota.

Sabic intends to boost production capacity for its proprietary resin to support growth of PCBs used in 5G base stations and high-speed servers.

Sanmina added **RoBAT** RCI backplane testing technology to its facilities in California and Mexico.

Schweizer Electronic named **Varikorea** sales representative for South Korea.

Sumitomo Electric Industries has succeeded in mass production of Fluorocuit, fluororesin-based flexible printed circuits for 5G applications.

Sun Chemical named **Icaro** to distribute its conductive and dielectric inks, as well as other electronic materials, in Mexico.

Taiwan-based PCB fabricators, now with 60% of their production capacity in China, are feeling more pressure to relocate their production plants to Taiwan, Southeast Asia and India.

TPCA is studying PCB factory smart manufacturing planning.

Trackwise installed a roll-to-roll direct imaging system and roll-to-roll flexible circuit laser drill.

Unimicron Technology sustained a fire at its PCB plant in Kunshan, China. The cause and extent of the damage are under investigation.

Ventec appointed **Spectrum Marketing Associates** sales representative for the US West Coast region and Mexico.

IPC Task Group Edges Toward Finish of OSP Spec

BANNOCKBURN, IL – An IPC task group is making progress on a new standard for organic surface protectants for printed circuit boards.

The committee is developing a series of test methods to enhance the assessment of an OSP's ability to meet performance requirements of high-temperature soldering. The latest document is in draft form and should be ready for a membership vote by spring, the task group chairman said.

IPC-4555, *Performance Specification for High Temperature Organic Solderability Preservatives (OSP) for Printed Boards,* is a reboot of an effort begun more than a decade ago. In 2008, the task group attempted a similar standard, but was undone when a key OEM disputed the results of the solderability data. Unable to reach consensus, the task group disbanded the effort.

Last year, a new task group made up of major companies, including Continental, Bosch, Raytheon, TTM and Sanmina, embarked on a new draft. IPC tapped Michael Carano, vice president of technology and business development at RBP Chemical, to chair the task group.

OSPs are commonplace, which makes the lack of a performance standard notable. According to Carano, 62% of world's boards use OSPs. "They are in medical devices, tablets, airbags, engine controls, and telecom," he said, and used in combination with other final finishes in advanced packages.

The goal is to develop performance specifications for high-temperature OSPs, defined as capable of withstanding up to two IR reflows in conjunction with tin-silver-copper (SAC) or tin-bismuth (SnBi) alloys at a peak temperature of 245°-250°C and showing the same wetting balance results at three reflows as zero, with a maximum 20% drop.

The new spec calls for all classes of high-temperature OSP to have a minimum shelf-life of 12 months when left in original packaging and following recommendations of IPC-1601. Solderability must meet J-STD-003 category B. SIR will be measured per IPC-TM-650, Method 2.6.3.5, GR78-Core, and electrolytic corrosion per IPC-TM-650, Method 2.6.14.1.

Multiple round-robin studies were conducted to generate data to support the requirements in the pending specification, the task group said.

The issue that killed the spec a decade ago has been resolved. Back then, the task group could not agree on the allowable range of coating thickness. According to Carano, the current task group has agreed that coating thickness is not a determinant in the performance of the coating. "We don't need one big range," he said. Instead, the thickness requirement will be per the chemical supplier data sheet.

"OSP is difficult to test through the coating because the coating is hard, and, depending on the pin probe, you might bend the probe," Carano allowed. "Suppliers are working on ways around that."

"The thicknesses of most finishes can be measured with XRF. OSP uses a spectrophotometer. Or, we can verify the empirical data from a focused ion beam. The task group compared thickness with spectrophotometer with FIB cut, and they correlated very well. It's like accelerated corrosion testing."

For rework, the task group notes multiple methods exist for removing the immersion gold deposit to evaluate for the presence of hyper-corrosion of the nickel. Cognizant of the possibility of false positives for hyper-corrosion, the committee is working on the release of a specific test method to cover appropriate methods for gold stripping, which will be incorporated as an amendment upon release. (MB)

Ucamco Releases Gerber Job Format Specification

GENT, BELGIUM – Ucamco released a Gerber job format specification that includes a schema that provides support for Gerber job format software developers.

The schema provides a definition of what can and cannot be inside a Gerber

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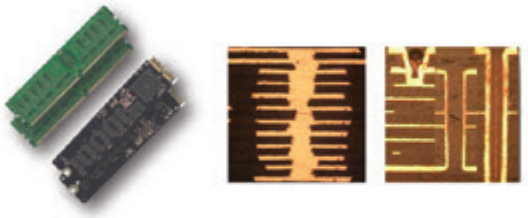
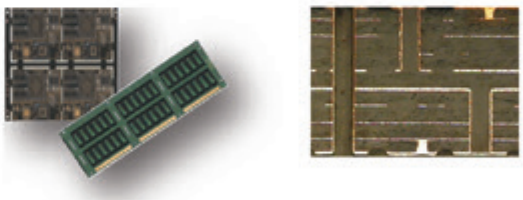
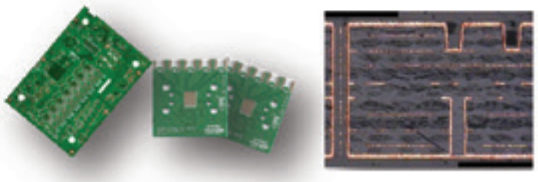


IOT / Build-up Board



Semiconductor TEST B'd & 5G Network System



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CA People

Cogiscan appointed **Sandipan Halder** key account manager. He previously worked for NuEnergy.ai as an account executive, and also spent nearly three years in channel sales at Honeywell.

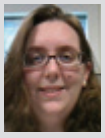
Dan Oh, Ph.D., vice president of engineering of Samsung's Test & System Package (TSP) unit, will keynote the International Wafer-Level Packaging Conference and Expo in October.

Enics named **Mahmut Bertan** chief business officer and **Rami Aro** director, services.

Indium promoted **Andy Mackie** to principal engineer and manager, thermal interface materials applications.

Inovar named **Kent Johnson** senior director of quality assurance. He has significant experience in defense, medical, aerospace, and nuclear power across a range of industries and a technical MBA from the University of Utah.

Intervala named **Eric Sicard** senior business development manager. He spent the past seven years at TT Electronics, most recently as market development manager, and was previously vice president of supply chain for API Defense and director of sourcing for OnCore Manufacturing.



Knowles Precision Devices named **Brook Sandy** applications engineer, RF and Microwave. She previously was technical conference program manager at IPC and spent 11 years in engineering support at Indium and Henkel.

Meridian Adhesives Group appointed **Brandon Willis** president of the company's Electronics division.

Nortech Systems CFO **Connie Beck** resigned to pursue an executive position at a private company. Corporate controller **Alan Nordstrom** will serve as acting CFO.

Part Analytics appointed **Jim Robinson** head of sales, responsible for all new OEM sales and support initiatives in the US. Most recently, he was chief commercial officer for Sleek Fleet, and held management positions at Microsoft and Google.

job file. It can be used programmatically to check a Gerber job file for errors and is mainly intended for reading or writing Gerber job files.

Any JSON schema reader that can parse a draft-07 schema can be used to read it and check Gerber job files against it for errors. (CD)

US PTO Publishes Apple Patent Application on Smart Fabrics

CUPERTINO, CA – The US Patent and Trademark Office published a patent application from Apple that discusses the manufacture of smart fabrics with specialized equipment that could be used to form fabric with integrated electrical components, according to reports.

Apple's patent application notes it may be beneficial to incorporate electrical components into fabric, but since fabric is flexible, new techniques are required. The company's invention covers interlacing equipment: for example, weaving equipment, knitting equipment, and braiding equipment.

Woven fabric may include insulating and conductive material, and conductive strands may form signal paths through fabric, coupled to electrical components such as light-emitting diodes and other light-emitting devices, ICs, sensors, and haptic output devices.

End products for next-generation fabric intertwined with electronics could relate to smartphones, computers, or other portable electronic devices, Apple says in the application.

Apple's patent application was filed in March, but some of the original work dates to 2019. (CD)

East West Goes North, Buys Universal Electronics

ATLANTA – East West Manufacturing in September announced the acquisition of Universal Electronics in a deal between privately held contract electronics manufacturers. Terms were not disclosed.

Whitewater, WI-based Universal Electronics builds printed circuit board assemblies, box-build assemblies, and performs testing and new product introduction. It was founded in 1980. It has nine SMT lines across its 87,000 sq. ft. plant in Whitewater and 40,000 sq. ft. plant in East Troy. It has estimated sales of more than $60 million, according to the CIRCUITS ASSEMBLY Directory of EMS Companies.

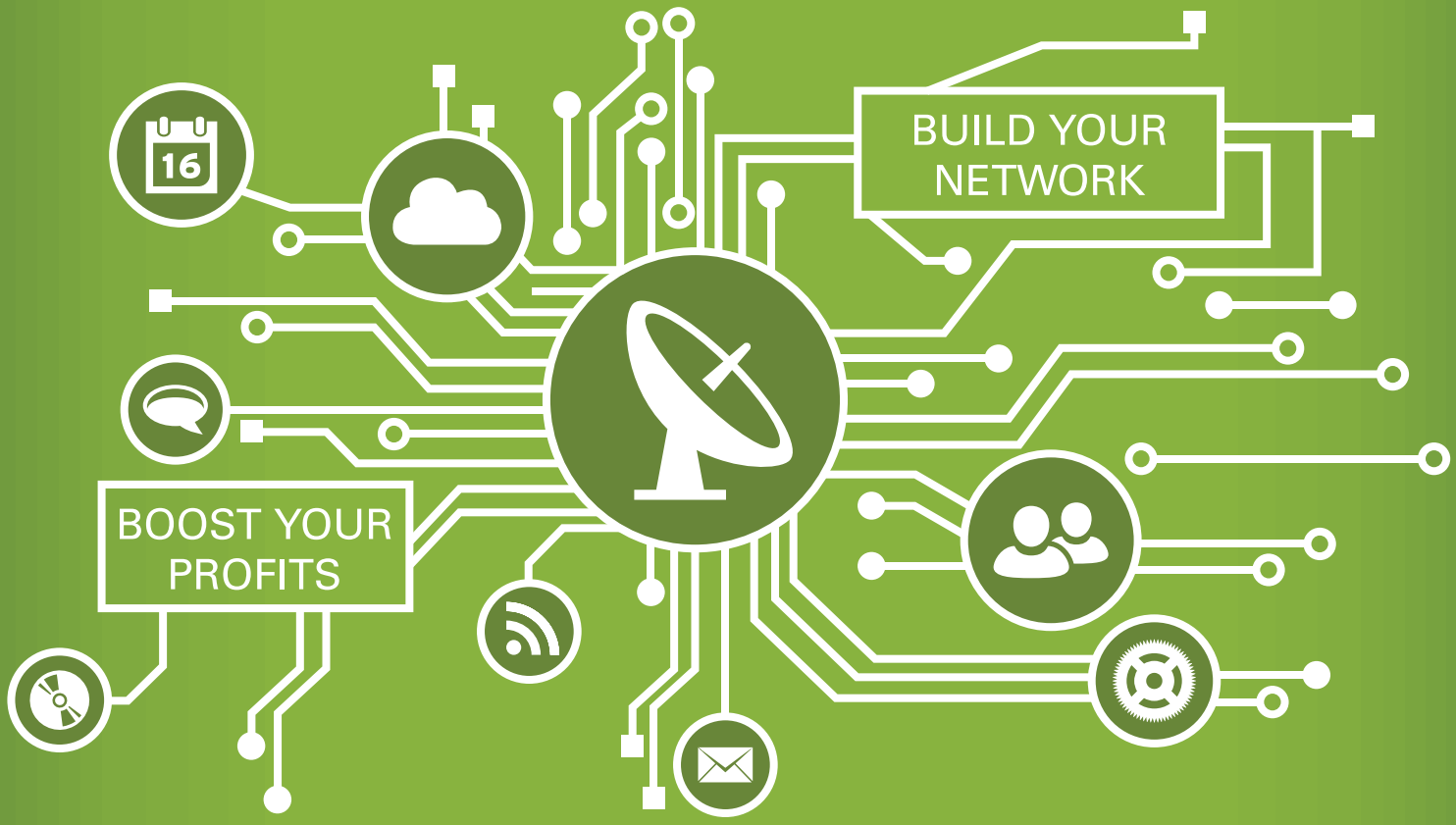
UEI advances East West's strategic focus on growing its domestic electronics manufacturing capabilities and expanding its US manufacturing operations, the company said in a press release. The acquisition extends East West's geographical reach in the Midwest, where the site is close to many current customers.

The purchase of UEI continues an acquisition plan by East West that includes prior buys of Team Manufacturing in 2018 and General Microcircuits and Adcotron in 2019.

"We are excited to partner with UEI to expand our manufacturing operations to the Midwest," said Scott Ellyson, cofounder and CEO, East West. "UEI has an incredible reputation for putting its customers first and has an established presence in a variety of high-growth sectors such as medical, industrial, telecommunications and defense. This acquisition allows us to offer greater domestic, higher mix, lower volume, quickturn electronic manufacturing services. Our collective design, manufacturing and supply chain capabilities will enable us to provide even greater levels of service and support to customers on a global basis."

"The leadership team and associates here at UEI are excited about becoming part of the East West family. Our culture, capabilities and customer-first focus align perfectly," said Rick Jensen, owner and president, UEI. "We expect the new combined company to help our customers continue to grow." (MB)

The *Circuits Assembly* *Directory of EMS Companies*



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SVI Public Co. named **Angkana Sornsakarin** chief accountant.

Tempo Automation named **Ryan Benton** chief financial officer. He has nearly 30 years of financial, operational and strategic experience, most recently as CFO of Revasum, a publicly listed semiconductor capital equipment company.

CA Briefs

Apple is expected to see a sharp rise in purchases of server components in 2020 and 2021 due to expansion of internal datacenters.

AQS purchased a **Precision PCB Services** SV500 BGA rework system.

Board Shark PCB named **MarTec** to provide sales and service in Alabama, Georgia, Mississippi, and Tennessee.

CalcuQuote and **Advanced Assembly** announced a new collaboration to expand software functionality and streamline processes through digital innovation.

Compaq and **Ossify Industries** have launched a range of QLED TVs in India.

Computrol purchased a **Viscom** X7056-II 3-D x-ray inspection system and an **Aqueous Technologies** Trident LDO-DUO cleaning system.

Dorigo Systems is showing off its new 105,000 sq. ft. EMS plant in Burnaby, BC.

Foxconn and **Pegatron** are reportedly eyeing new factories in Mexico as the US-China trade war and coronavirus pandemic take their toll on global supply chains.

Foxconn's chairman told investors China's "days as the world's factory are over."

An Indian panel has approved a plan by **Foxconn, Pegatron, Wistron** and others to export mobile phones worth around $100 billion, or Rs 7.3 lakh crore, from India.

Some 15 tonnes of copper scrap were reportedly stolen from **GPV's** facility in Tarm, Denmark, the second break-in since July.

Jabil has selected **Keysight's** 5G device test solutions to address the demand for 5G product validation in design and manufacturing. Jabil is also suing **Singer,** saying it was not reimbursed for more than $2.6 million in pre-production costs.

Nortech Systems has completed the sale and leaseback transactions for its manufacturing facilities in Bemidji and Mankato, MN, at a sale price of $6.3 million. It also will close a production plant in Merrifield, MN, affecting 60 to 70 jobs.

Outroar LLC has launched new EMS PCB assembly services under the name **Titan Circuits.**

Specialty Coating Systems moved its Parylene coating center to a new 6,000 sq. ft. multipurpose facility in Dublin.

TopLine announces the availability of comprehensive FPGA repair, rework, and column attachment services.

The **University of Wisconsin-Madison** has received less than 1% of the money **Foxconn** pledged to it two years ago. In August 2018, Foxconn committed $100 million to the university to help fund an engineering building and for company-related research.

The **US Defense Department** is proposing to amend the Defense Federal Acquisition Regulation Supplement (DFARS) to update the policy and procedures for use of the Supplier Performance Risk System.

The US Undersecretary of Defense for Acquisition and Sustainment says America can "no longer clearly identify the pedigree of our microelectronics. Therefore, we can no longer ensure that backdoors, malicious code or data exfiltration commands aren't embedded in our code."

Violet Defense has awarded **SMTC** a multimillion-dollar, multiyear contract to build Xenon UV disinfection devices.

Virtex announced the creation of 40 to 50 new manufacturing jobs at its EMS plant in Waynesboro, VA.

Viscom sold S3016 ultra 3-D AOI to **Bosch** and **E.D.&A.**

Weller Tools named **Cardinal Marketing** manufacturers' representative in Illinois and Wisconsin.

Creation Technologies Breaks Ground on EMS Plant in Hermosillo

HERMOSILLO, MEXICO – Creation Technologies has broken ground on a high-volume electronics manufacturing facility here that will nearly triple its Mexico footprint. The company is expanding its North American footprint to better serve aerospace and defense, medical, and tech industrial customers.

The new facility will provide more capacity, with a total of 205,000 sq. ft., bringing total capacity of Mexico operations to 330,000 sq. ft., including existing capabilities in Mexicali. It is scheduled to be operational in the third quarter of 2021.

"We are thrilled to announce our plans for a significant expansion of our manufacturing capacity in Mexico," said Stephen P. DeFalco, chairman and CEO, Creation Technologies. "This expansion builds on our current Mexico operations, where we have over 700 dedicated employees focused on providing outstanding service to our customers' high-reliability needs."

The site will have space for up to 12 automated SMT lines and will be a purpose-built greenfield facility designed for Lean factory flow.

The facility will provide dedicated areas for PCB assembly, system integration and test, as well as forward and reverse logistics. (MB)

Gowanda REM-tronics to Close EMS Plant in NY

DUNKIRK, NY – EMS firm Gowanda REM-tronics will shutter its plant here Nov. 15, eliminating 69 jobs, according to reports.

Staff received a letter stating Gowanda Components Group and its affiliates have been "adversely affected" by economic factors. The company said trouble in the avionics and fiberoptic sensor markets led to the "shutdown of entire industries," affecting orders.

The factory supplies to the aerospace, industrial, medical and military industries. (CD)

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>
> – *Rick Hartley*

written by

Charles Pfeil

Charles Pfeil has spent over 50 years in the PCB industry as a designer, owner of a service bureau, and in engineering management and product definition roles at Racal-Redac, ASI, Cadence, PADS, VeriBest, Mentor Graphics, and Altium. He was the original product architect of Expedition PCB.

TVS TURNED ON

Trends in the U.S. electronics equipment market (shipments only).	% CHANGE MAY	JUN.	JUL.	YTD%
Computers and electronics products	0.3	-0.3	4.0	1.5
Computers	2.1	0.2	-3.0	-11.3
Storage devices	-2.1	-4.9	1.6	46.6
Other peripheral equipment	9.5	-14.5	20.3	6.3
Nondefense communications equipment	0.2	-0.4	9.5	7.2
Defense communications equipment	7.2	1.1	-4.5	0.4
A/V equipment	4.0	13.9	11.0	-13.9
Components[1]	-0.3	0.0	5.5	9.1
Nondefense search and navigation equipment	-0.7	1.0	1.4	-6.4
Defense search and navigation equipment	-0.2	0.2	2.2	3.0
Medical, measurement and control	0.0	0.2	0.4	-3.5

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, Sept. 2, 2020

Hot Takes

- **Personal computing devices,** including traditional PCs, tablets, and workstations, will grow 3.3% year-over-year in 2020, with shipment volumes reaching 425.7 million units. (IDC)
- **By 2030, augmented, virtual and mixed reality optics and display markets** are expected to total more than $28 billion. (IDTechEx)
- **Total smartphone production** reached 286 million units in the second quarter, a sequential rebound of 2.2% but a 17% drop year-over-year. (TrendForce)
- **The worldwide smartphone market** is forecast to decline 9.5% year-over-year in 2020, with shipments totaling 1.2 billion units. (IDC)
- **The consumer electronics market** is expected to surpass $1.5 trillion by 2026, up from $1 trillion last year. (Global Market Insights)
- **The output of PCBs in Japan in June** was down 234% year-over-year to 803,000 sq. m. (JPCA)
- **Global home audio** posted second quarter shipment growth of 20% sequentially. (Futuresource Consulting)
- **The fan-out wafer level package (FO-WLP) market** is projected to grow 15.5% in units from 2020 to 2024. (TechSearch International)
- **The worldwide electronics assembly market** consisted of approximately $1.3 trillion in terms of cost of goods sold as of 2019. (New Venture Research)
- **M&A activity in the EMS sector** stalled in the second quarter, with just three deals closing in the period. The three deals included two consolidations and one vertical/horizontal convergence. (Lincoln International)
- **Taiwan automotive PCB shipments** declined 6.7% in the first half, the only segment with negative sales growth in the domestic industry. (TPCA)
- **The overall 5G enterprise market** will reach $2.3 billion in 2020 and is projected to reach $31.7 billion by 2026, at a CAGR of 54%. (MarketsandMarkets)
- **The printed electronics market** is forecast to grow 4% from 2020 to 2026. (ReportLinker)

METALS INDEX

US MANUFACTURING INDICES

	APR.	MAY	JUN.	JUL.	AUG.
PMI	41.5	43.1	52.6	54.2	56.0
New orders	27.1	31.8	56.4	61.5	67.6
Production	27.5	33.2	57.3	62.1	63.3
Inventories	49.7	50.4	50.5	47.0	44.4
Customer inventories	48.8	46.2	44.6	41.6	38.1
Backlogs	37.8	38.2	45.3	51.8	54.6

Source: Institute for Supply Management, Sept. 1, 2020

KEY COMPONENTS

	MAR.	APR.	MAY	JUN.	JUL.
Semiconductor equipment billings[1]	21.2%	18.7%	13.5%	14.4%[r]	27.6%[p]
Semiconductors[2]	6.85%	6.13%	4.82%	4.95%[r]	4.92%[p]
PCBs[3] (North America)	1.15	1.19	1.10	1.12	1.00
Computers/electronic products[4]	5.43	5.44	5.44	5.44[r]	5.28[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

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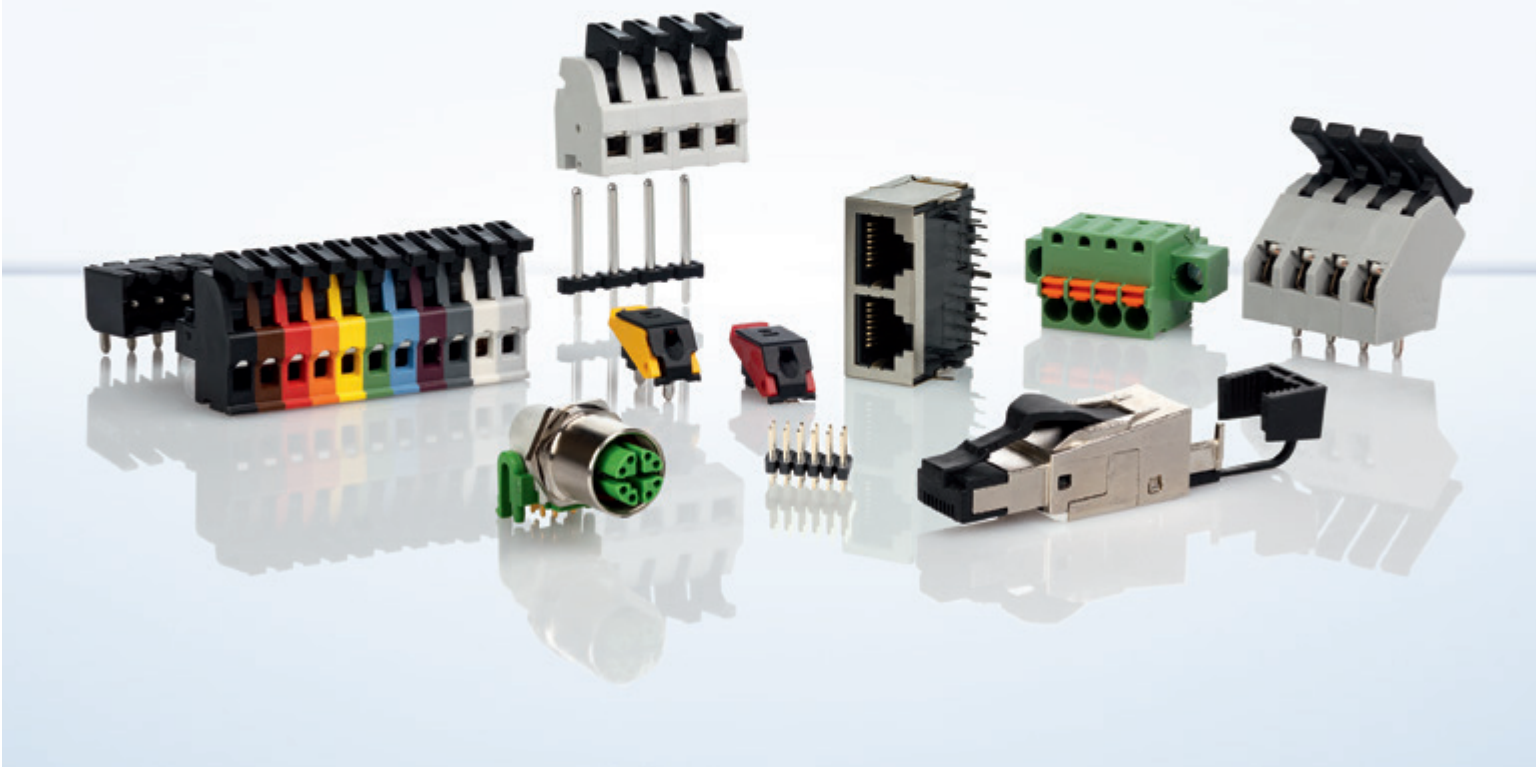

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Meeting of Minds: Are Company Events 'Virtually' Never-ending?

As communication shifts online, time management becomes a group effort.

TIME MANAGEMENT, THE operative word being *management,* is never easy to master. Scores of books and lectures elaborate on how to stop the interruptions, focus on the important, and liberate one's ability to get things done. Even so, the challenge has become even more elusive over the past year.

Until recently, time management focused on how to reduce interruptions from various activities and events, such as unwanted phone calls, perpetual cubicle chats, and the length and focus of conference room meetings. Historically, those were leading contributors to inefficiency and wasted time. That was then; this is now.

Communication has become email-centric. Phone tag is no longer the corporate sport. A typical workday commences by sorting the email inbox, vetting the important ones, and then doing the same in the spam folder filled with six zillion missives, many from finance ministers of countries no one has ever heard of. Face-to-face interaction, however, has remained tied to the corporate conference room, where at any time different combinations of coworkers, customers and suppliers meet to solve some problem or communicate about new or changing opportunities.

Over the past year a seismic shift has taken place. Social distancing, travel restrictions and work-from-home have altered the workplace and how we collaborate. Tools that were known but not generally deployed – like Zoom and WebEx – are now the preferred methods of group communication and collaboration. As convenient and spontaneous as these technologies are, they have wreaked havoc on time management as we know it.

Efficient use of time typically means arranging events, such as meetings and customer/supplier visits, into time blocks around which other activities can be scheduled. The sales staff visits several customers in a similar location on a single trip. Ditto the purchasing staff when visiting suppliers. Company meetings are set for a time and date when all participants are in the office. And most of all, because of logistics such as travel time, they spread out to keep those costs to a manageable minimum. Time was managed in advance based on schedules. Effective time management successfully eliminated the sporadic interruptions that torpedoed otherwise well-planned days.

The current work environment has changed dramatically. Employees rarely work in the office. Customer and supplier visits are increasingly virtual. Schedules are flexible. Spontaneous virtual meetings, gatherings and collaboration, often outside the traditional "9 to 5" business hours, have become the norm. And because technology permits it, "regular" meetings seem to be more frequent and include a far greater number of participants. All this tanks traditional time management strategies.

Successful time management is now as much a group effort as an individual initiative. Good time management still includes sharing a schedule with colleagues, communicating it through whatever method – usually electronic – your organization utilizes. It still requires focus on what is important. However, it is more important than ever for the organizer of a virtual meeting, gathering or event to plan!

Think beyond just the purpose of the virtual gathering. Other planning is critical to manage time effectively. Ask: How long is reasonable for the meeting to last? Who must attend vs. who may want to be included? Most important, how frequently will the virtual event be held? This last point may be the single contributor to inefficient time management.

Do you find monthly meetings become weekly meetings, and one-off gatherings morph into ongoing scheduled events? Just because we *can* meet doesn't mean we *must* meet. Spontaneity can be great, and with coworkers and colleagues seemingly so flexible and available, virtual meetings are easy. But when they become too frequent or spontaneous, they tend to accomplish less, and the time consumed outweighs the benefits. The virtual event itself overshadows the reason the event was needed in the first place.

Right up there with meeting frequency is being clear as to who needs to vs. who could attend. Again, discerning *need* vs. *could* is critical to effective time management. The more people involved, the more time each virtual meeting inevitably takes. Compounding this basic time management inefficiency is the number of nonessential people who instead need the time to accomplish more important tasks. Most virtual meetings or events are arranged to accomplish a specific result, so it is critical to keep the attendee list to just those who are needed. Be proactive. The organizer should identify which participants are necessary and which participants are welcome only if more important activities aren't on their plate.

Finally, everyone needs to stick to the schedule. If the event is scheduled to take one hour, do everything possible to keep to that time. If it looks like the subject needs five more minutes to complete, offer that as an option before scheduling the next meeting. Regardless of technologies utilized, locations of employees and colleagues, or the purpose of the meeting, effective time management means a shared focus on getting things done. □

PETER BIGELOW
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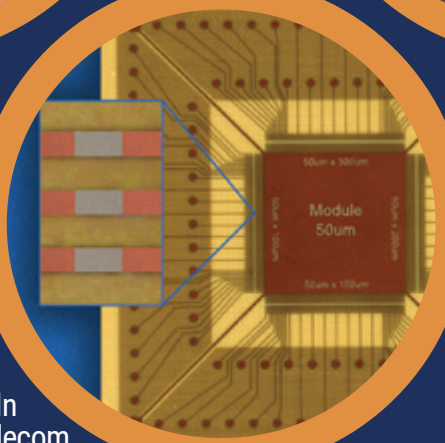

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Hindsight is '2020': The Organizational Stress Test

The big lesson from this unpredictable year is infrastructure planning pays.

"HINDSIGHT IS 20:20" refers to a vision measurement, not this crazy year. But from a planning standpoint, the year "2020" has rewarded electronics manufacturing services (EMS) companies that built resilience into their operational plans. As I write this, the Covid-19 pandemic continues to spur an era of new normal. The introduction of vaccines will hopefully drive a return to something close to the old normal. While this challenge is ongoing, however, it is important to look at some of the operational investments that have proved most beneficial.

Here are five areas that stand out to me:

IT. Companies that were already supporting employees working remotely as a result of business travel, remote home offices or a need to work in multiple time zones more comfortably had an edge in converting a larger portion of the workforce to work-at-home scenarios. VPNs, internal systems capable of supporting secure and fast access to remote users, videoconferencing tools, seamless transfer of work phones to mobile phones, and existing policies/training on maintaining security in home office environments are all key elements enabling employees to effectively work at home. Companies with these in place simply had to scale up to accommodate a larger user base. Systems strategy has also been integral in managing the supply chain and forecasting disruption driven by Covid-19. Companies with systems that can quickly assess inventory levels, material availability and production status globally were better off than those with facility-specific systems or systems that required much manual interpretation to gather that information.

Issues to consider in future investments include:

- What security vulnerabilities did work-at-home scenarios create, and how does the protection and training strategy need to change?
- Were connections fast enough for remote work and communication?
- Overall, are systems providing enough status visibility when forecasts, availability and production capacity/output are changing rapidly?

Design for procurement. Covid-19 hit just as industry was returning to normal from multiple years of supply-chain constraints. Companies with good discipline in terms of getting customers to specify or approve alternates on all component line items, internal stocking programs, and good relationships with a broad base of suppliers were better prepared for Covid-19 disruptions. Unlike the previous constraints, Covid-19 disruptions ran the gamut: closed factories, logistics surprises and prioritized demand under the Defense Production Act. Consequently, it wasn't a matter of getting in line for a later delivery on an allocated part. In some cases, it required a quick switch to alternate suppliers or broker authorizations because there was no clear timeline on when the original part would be available. There was also little predictability on which suppliers would be disrupted because factory closures and shipping disruptions were occurring all over the world. Internal stocking programs and finished goods kanbans helped buy time when alternate arrangements were needed, but they weren't a total solution.

Issues to evaluate include:

- Is the purchasing department too dependent on a limited supply chain?
- Do program managers help customers scrub BoMs and AMLs early to flag potential part problems and ensure options are identified and approved for most of the BoM?
- Are stocking programs and finished goods kanbans sized appropriately?
- Do any areas of the supply-chain disruption mitigation strategy need to be enhanced?

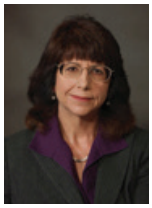
Rapid, repeatable NPI. New product introduction has a lot of definitions in the EMS industry. In some companies it is a unique process every time, predominantly driven by customer requirements. In other companies there is a formal base process with a defined timeline, support team and systems which support rapid transfer and verification of documentation, process validation and initial builds. Companies with well-defined processes were in a better position to add business from companies needing to reshore or expand their suppliers to deal with disruptions or excess demand in their existing supply chain.

Issues to evaluate include:

- Were any opportunities lost because of an inability to launch a new project quickly enough?
- Are the systems supporting the NPI process automated enough to support rapid response?
- Is the NPI process well defined and repeatable enough to launch projects rapidly without mistakes?

Lean manufacturing. Lean manufacturing philosophy offers a variety of benefits, including scheduling flexibility, optimized throughput and better organized factory floors. All these things have come into play during the pandemic. Some OEMs increased orders dramatically in medical or critical infrastructure sectors. Others cut forecasts or ceased production, then began increasing orders to address pent-up demand later in the

SUSAN MUCHA is president of Powell-Mucha Consulting Inc. (powell-muchaconsulting.com), a consulting firm providing strategic planning, training and market positioning support to EMS companies and author *of Find It. Book It. Grow It. A Robust Process for Account Acquisition in Electronics Manufacturing Services*; smucha@powell-muchaconsulting.com.



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(G)type NEW

Laminate **R-5785(GN), R-5785(GE)**
Prepreg **R-5680(GN), R-5680(GE)**

(GN):Low Dk Glass cloth type (GE):Normal Glass cloth type

Features

- Improved lamination processability compare to MEGTRON7 R-5785(N)
- Glass transition temperature (Tg): 200℃ (DSC)
- Multi-site production in Japan/China

	Dk	Df
R-5785(GN)	3.4	0.002 @ 12GHz
R-5785(GE)	3.6	0.003 @ 12GHz

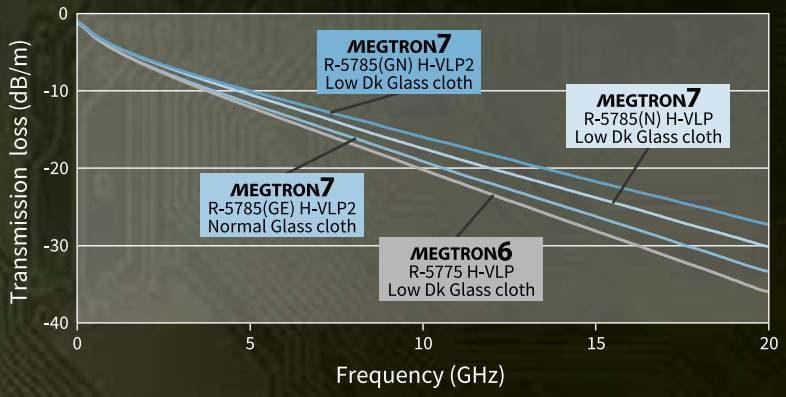
Applications

- High-end servers, High-end routers, Supercomputers, and other ICT infrastructure equipment, Antenna (Base station, Automotive millimeter-wave radar), etc.

Transmission Loss

- Construction

Trace thickness(t)	18μm
Dielectric thickness(h)	300μm
Copper thickness	18μm
Inner treatment	No-surface treatment
Core	0.15mm (#1078 x 2ply)
Prepreg	0.15mm (#1078 x 2ply)
Line length	1000mm
Impedance	50Ω



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year. Some EMS factories needed to shut down or had capacity constraints due to local mandates on employee headcount. Companies with production processes optimized for scheduling flexibility, combined with good visibility into inventory, material on order and production status, were in the best position to address this chaos. Additionally, the level of organization and lack of clutter or work-in-process (WIP) found in most facilities focused on Lean manufacturing principles made it easier to address mandated social distancing requirements.

Issues to evaluate include:

- Did equipment constraints create bottlenecks or otherwise limit flexibility in accommodating demand increases?
- Did factory clutter or WIP create issues in implementing recommended social distancing practices?
- Is the company too Lean in areas such as inventory to accommodate this level of disruption?
- Is there sufficient commonality in equipment and processes among facilities to accommodate rapid transfer of work in the event of facility shutdowns?

Cross training. Cross training makes it easier to shift employees around a factory as demand changes. It also makes it easier to accommodate vacations or absences. Companies that had invested in cross training were able to give production workers more flexibility in shift choices as schools closed and childcare became a problem. They also have been better situated to cope with attrition or headcount constraints driven by employee health concerns or local restrictions.

Issues to evaluate include:

- Were all employees who needed shift changes due to personal issues accommodated?
- Were there surprises in the employee competencies when workers changed shifts that should be better addressed in future training programs?
- Have enough employees been cross-trained in critical functions to accommodate absenteeism where sick employees are asked to stay home and employees with health issues may want to stay home?
- Does current shift structure fit the needs of the labor market, or would a different schedule better accommodate the workforce?

None of these five areas of investment is groundbreaking or new. Many companies are investing in these areas at some level. While 2020 is a year no one is likely to want to repeat, the organizational stress test is invaluable. In a year where all the original plans were wrong, investments made in these areas turned out to be of far greater value than anyone likely assumed. Companies that take the time to evaluate the gaps in infrastructure identified in this reactionary environment and the organizational investments that outperformed expectations, and incorporate that knowledge in their future planning, will likely leave 2020 in a better position than they entered it. ▫

Made in America is Great – *If* You Can Do It

American manufacturers are throwing away business opportunities. Are you?

GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying; greg@boardbuying.com.

ACCORDING TO A recent statement by US Undersecretary of Defense for Acquisition and Sustainment Ellen Lord, national electronics procurement is at a crossroads.

"[America] can no longer clearly identify the pedigree of its microelectronics," she said. "Therefore, we can no longer ensure that backdoors, malicious code, or data exfiltration commands aren't embedded in our code."

According to Lord, a variety of price pressures – ranging from government regulations to labor costs – have driven manufacturing of electronics offshore and created not only an economic imbalance but a security threat as well. "That's what we need to reverse," she said.

Like the Defense Department, American consumers also support bringing manufacturing back onshore. They believe the "Made in USA" slogan means saving American jobs and, often, superior quality of goods. They support "reshoring" – bringing the manufacturing and assembly of goods – back to the US.

But would that actually work? Would US PCB customers receive the same service from domestic sources they get from offshore assembly houses and manufacturers? Can domestic PCB suppliers keep up with demand and provide timely delivery?

The answer, unfortunately, is no, unless domestic firms make some critical changes.

Since the onslaught of tariffs and the Covid-19 pandemic, my firm has received many inquiries for new projects to be fabricated or assembled domestically, along with possibly reshoring ongoing work. It's a noble intention, and we've been trying to help. We've reached out to more than a dozen North American PCB assembly houses and manufacturers to get work placed.

The experience has been a mixed bag, to say the least. Here is what we have encountered in our search for domestic shops:

- Inflexible order sizes. Domestic companies with huge assembly operations seek large-volume orders and won't quote a job less than about $2 million annually in revenue. On the other hand, most domestic fabricators prefer small to midrange run orders. They won't take on customers with the mid-to-higher-volume business typically made offshore. Plenty of customers with orders in that range couldn't place their business domestically even if they wanted to. That's a shame. Offshore companies are aggressively quoting NPI programs. If China can compete on small lots, then the US should at least try to compete on big ones.

- Inefficient quoting. I can't tell you how many times after I have submitted an RFQ that I have to either follow up to confirm the RFQ receipt, or call weeks later looking for an update on the quote. And the US-based sales department frequently fails to communicate pertinent information to its quoting team, so the quote is inaccurate. Or a quote has been sitting overlooked on someone's desk or in their email. I get better communication from companies on the other side of the world.

  Every assembly quote is different, each with its challenges. But like most processes in our industry, quoting should follow established procedures. What is your company's policy for quote response time? (Do you have one?) How often do you hit your target? And when the promised response date has passed, do you always call the customer to notify them of the reason for the delay?

- Refusal to quote. One shop I tried to get quotes from – a new state-of-the-art facility that touts its production capability – flat-out refused because they "don't want to compete with China." I explained the end-customer understands the price would be higher and still wanted a quote. The answer remained "no." What's going on here?

- Poor customer service. Do you have problems with simple stuff, like getting people to respond to an email or return a call in a timely manner? Me too. There's also a lack of urgency with the basics, like notifying customers about schedule changes or ensuring paperwork is correct.

  These are companies I've done business with before. In many cases, I personally know the owner. They know I have many customer contacts. If they treat me this way, how do they treat an unknown prospect?

- Unwillingness to invest in technology. Because of customer requests, I've been trying to reshore existing volume orders, with some difficulty. One of my domestic board shop connections is an established facility known for large-volume orders.

Unfortunately, this company appears averse to change, especially when it comes to upgrading the equipment needed for today's technology that would permit it to compete globally.

Investing in capital equipment isn't cheap, but it is certainly more costly to our industry when domestic shops fail to meet the rising technology curve and cannot fulfill customer demands. Perhaps a collective could be formed to improve capital expenditure purchasing terms and, since hardly any PCB equipment is manufactured in the US, ensure a domestic ample inventory of spare parts. Investment in local personnel who could provide tech support for the equipment is also advisable.

When an OEM approaches me for help, I recommend a domestic source about 80% of the time. I've found that when a domestic supplier goes head-to-head with an overseas manufacturer – factoring in tariffs, minimum order values, overseas delivery, and time-zone delays – the total cost of ownership (TCO) for PCB assembly is comparable in the US to offshore.

(Many customers forget tariffs add to the bottom line. While 2- and 4-layer bare boards are exempt, 2- and 4-layer *assemblies* are subject to tariffs.)

Thus, it is even more frustrating when domestic assemblers refuse to accept quotes or fail to deliver decent service. The TCO often favors a domestic manufacturer – *if* an OEM can find one willing to build mid-to-higher volumes. American manufacturers are throwing away business opportunities.

Of course, many domestic PCB manufacturers and assemblers don't have these problems. But if we want the broader industry to return to the US – instead of getting piecemeal jobs – we need to be willing to provide a comparable level of service to that of the overseas competitors.

Undersecretary Lord properly defines the goal, but I believe her solution focuses too much on pricing and not enough on the customer experience. US assemblers need to open their arms to potential customers. It will help both them and the US manufacturing situation at the same time.

Otherwise, OEMs and other board buyers will stick with offshore sourcing because they need to get their products built at a good price *and* in a timely manner. And "Made in America" will remain only a slogan from a bygone era. □

Design for Rework: Extending the Usefulness of a PCB

Anticipate the assembler's needs in placement and routing.

WE ALREADY DESIGN for fabrication, assembly and test. DFx can be extended to thinking about future uses of an assembly. Sometimes a printed circuit board needs to be revised right away. There are things we can do to facilitate rework. Clearly marking all the components is a good start. A robust design will lend itself to touch-up and rework scenarios. Let's dive into some techniques.

Breadboarding for "science projects." Ever seen a breadboard? In PCB design terminology, a breadboard is a rectangle with a grid of plated through-holes set on the same pitch as a DIP package (**FIGURE 1**). The holes will accept axial-leaded components as well as the odd transistor package. Notice the rows of pins are tied together but can be cut as required by the mad scientist in the lab. Jumper wires on the leads create the rest of the circuit. Development boards can usually afford a slimmed down version of this.

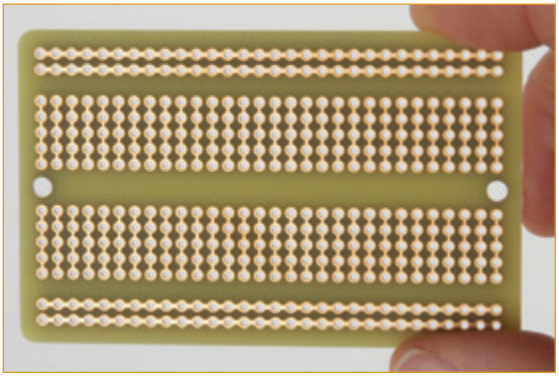

FIGURE 1. A corner of the board can have a similar function for added development potential. Credit: Adafruit

No space for a breadboard? A rectangular region of the board can be set aside for a "dead bug." A component of any type can be glued to the board with the leads facing up. Then wires can be attached to the leads and connected as necessary. Another option uses a common component footprint placed on the board without any actual routing. A cap footprint can be placed at either end.

Two rows of pins can be placed side by side without a specific footprint in mind. One or both rows can have extra wide pins to accommodate the usual width, along with a wider package. The extended pads provide a location to attach a jumper wire. A second pair of rows can have a finer pitch. The idea is the geometry lends itself to different potential footprints, SO-8, SO-16, etc. It all depends on the component mix as to how future-proofing is implemented.

More generically, the solder mask can be strategically opened to allow a shunt cap or resistor to be placed along a transmission line. Again, different size phantom components can be added as the possibilities allow.

Typically, closed circuits can be designed with the option of becoming series elements. It's all the same net until the technician cuts the strap across the pads. Then a resistor, capacitor or ferrite bead can be installed in the component location. This wouldn't be great for a controlled impedance situation. It is, however, a common option when a power domain must branch out.

Joining two small pieces of metal together in an oven is easy. All it takes is two pieces of metal and something that melts and then "wets" to both elements, which harden after coming out of the oven heating zone. Chocolate chip cookies come to mind (as they always do). Given a big enough chocolate chip, two cookies could be fused together, creating a crazy figure-8 cookie held together by chocolate. (Note to self: Expand on this two-for-one, high-chocolate ratio cookie idea next time we're going down the baked goods aisle.)

FIGURE 2. Series elements can be preplanned with common footprint geometry.

FIGURE 3. The additional border area enhances the jumper effect of this normally open circuit. Heating both sides permits a blob of solder to bridge the gap.

That is not a great metaphor for all the chemical transactions that occur on an SMT line but the effect is the same. Bring

continued on pg. 23

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

Human-Augmentation Technologies are Worth the Risks

Advanced prosthetics highlight the value of pure research, with or without a business case.

I HAVE SAID this before, but I am a huge fan of technology's potential to help humanity, and particularly the opportunities to improve quality of life and restore impaired physical capabilities.

In my last column, I enthused about using augmented and virtual reality to create experiences and environments that help people interact and enhance their well-being. Physical augmentation, with technologies such as powered exoskeletons, have industrial and therapeutic applications and could also be used to help people with mobility problems get outdoors to tackle activities such as hill walking. Lack of mobility can have negative effects on the state of mind, as well as physical condition, so an assistive technology that tackles both these challenges could help us establish healthy approaches to aging and help us all keep engaged with the world around us for longer.

"Engineering communities should take on projects for no better reason than because they can."

A prime application for exoskeletons is to help people suffering from disability or limb loss reacquire important capabilities such as walking. Remarkable as these technologies are, there is enormous scope for improvement to make them easier to use and more affordable and therefore accessible to more people worldwide.

A lot of exciting work is happening in this area, particularly at the interface between academia and the many young startups spinning out of medical research projects. One that came to my attention is Mitt, which is connected with the Imperial Enterprise Lab at Imperial College London. Inspired by finding that some 50% of medical patients who receive a prosthetic give up after about one year because the limb is uncomfortable, difficult to use, and complicated to acquire and maintain, Mitt's team is developing high-tech solutions to improve wearers' experiences. It's not only the user interface – which, perhaps surprisingly, often comprises hooks and cables similar to the mechanisms used in prosthetics dating back as far as World War II – that is calling out for improvement. Affordability is a problem in the Western world, and even more so in the developing world, where limb loss is a greater problem. By leveraging technologies such as 3-D printing and smartphone-scale AI, we can hope these powerful restorative therapies become accessible to more than just a relatively privileged few.

Ideally, it would be best to control the prosthetic as easily and as naturally as a biological limb. Researchers have been developing brain-machine interfaces (BMIs) to achieve this, with limited success so far. Elon Musk's Neuralink initiative has sought to address some scalability issues that have restricted earlier BMIs to a relatively small number of channels and hence placed limitations on their speed and capabilities.

By developing robot-assisted processes to insert fine, flexible electrodes into the brain, without causing damage or being constrained by the presence of blood vessels, Neuralink aims to permit BMIs to have any number of channels for the electrode transmission from just a few to hundreds or thousands. It has also worked out a way of inserting these quickly, using robotic tools, that could reduce the time for the process to just a few minutes. The electrodes are brought out to a device worn discretely behind the ear, which handles the processing and wireless connectivity that allows the wearer to control a device such as a computer or machine with their mind.

Neuralink is still in its early stages and may ultimately fall short of Musk's hype. However, this work could at least help standardize aspects of the BMI and thus contribute toward reducing the cost of advanced prosthetic controls.

The issue here is not the accuracy of Musk's claims but the value of the insights acquired. While Neuralink may or may not succeed, the body of knowledge within the scientific community continues to grow. This is the reason research must be allowed to continue without necessarily having a business plan behind it. Sometimes you have to start the journey before the destination becomes clear.

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ALUN MORGAN
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How Big is Your Moat?

If the clearance is not at least 10 mils, yields may drop.

ONE OF THE often-overlooked aspects of a board design is the moat. Perhaps this conjures up images of Monty Python's *Holy Grail*, but moat does not refer to the ring around a castle. Instead, this is the clearance between pads and a surrounding copper plane, sometimes also referred to as embedded clearance.

These clearances often are 0.004" to 0.005" wide. This may seem like plenty of room, but Pareto analysis tells us this can lower overall manufacturing yield. These clearances often lead to unexpected yield loss, depending on certain design and processing factors. Believe it or not, etching these moats or clearances is difficult, due to the closed-ended, circular nature of the clearances. They do not image or etch well and are prone to shorting.

One reason is that driving the energy into the resist can result in bleeding and create an imaging short. But etching is also more difficult, as the etchant flow is trapped in a dead-end donut. These can conspire to create unintended image/etch shorts.

Mechanically there is potential for misregistration shorts, depending on the drill size, annular ring design and layer count. In such cases, the drilled and plated hole may short to the neighboring plane.

A good rule of thumb for mechanically drilled holes is to maintain at least 0.010" clearance from a drilled hole edge to any adjacent copper. This helps ensure adequate mechanical clearance to account for layer misregistration, drill inaccuracies, as well as any internal etch-back or wicking in the hole. Note that this measurement is from drilled hole edge, not finished hole edge. Drilling is often 0.003" to 0.006" larger than the finished hole requirement to account for plating thicknesses and tolerances. This is where things end up tighter than expected if the designer does not account for drilled size compared to finished size.

Keep in mind there may be literally thousands of these embedded pad clearances on plane layers, especially as we see more HDI features. With multiple ground, power and voltage planes, this adds up. The term DPMO (defects per million opportunities) comes to mind. If we reduce the number of these potential tight spots, yield improves.

Our first advice is to grow the clearances, if possible. Clearances of 0.006" or 0.007" are a substantial improvement for 1-oz. and thinner copper. If the layer is 2-oz. copper or thicker, we suggest another 0.0015" to 0.002" per ounce.

Sometimes this may present a challenge or two. If the moats get bigger, there may not be room for material between pads. That is fine, provided we don't leave isolated pieces of copper. Those can lead to slivers of copper that may come loose, or electrically floating planes. Completely remove any slivers. Review any isolated floating planes for opportunities to make at least one web connection to the larger plane.

In other cases, there may be signals between pads, and the plane is supposed to cover them. Here, do your best to thread the needle with signal trace and minimize the web between pads (**FIGURE 2**).

Beware the autorouter! It will not always center traces between pads (**FIGURE 3**). The autorouter will route signals to meet the minimum requirement, not the optimal solution. Often it will pack two traces between pads when it should or could have routed one to each side of a pad. This may not be perfect when it comes to impedance signals but in practice is likely to be overlooked in the system.

This is where a designer can maximize their impact by taking the time to center traces, as well as revisit how traces are routed between pads. Is there an alternate path that opens space to reduce the plane? Are traces moving efficiently between the pads? Many times, the angle the trace cuts between pads causes smaller spacing than necessary. Design diligence can result in a much higher yield and lower overall unit costs. The investment in design time will pay off in production.

Another option: Consider

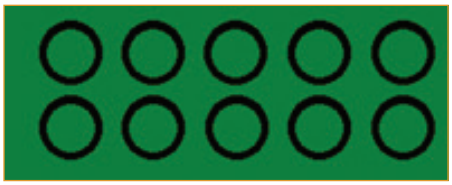


FIGURE 1. The clearance between pads and a surrounding copper plane is called a moat.

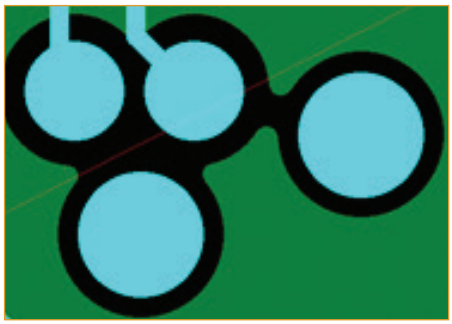


FIGURE 2. A larger moat could eliminate room for material between pads.

NICK KOOP is director of flex technology at TTM Technologies (ttm.com), vice chairman of the IPC Flexible Circuits Committee and co-chair of the IPC-6013 Qualification and Performance Specification for Flexible Printed Boards Subcommittee; nick.koop@ttmtech.com. He and co-"Flexpert" **MARK FINSTAD** (mark.finstad@flexiblecircuit.com) welcome your suggestions.

the size of the nonfunctional pads. After completing routing, if there is no room to reduce the webbing of the plane, an acceptable option is to reduce or eliminate nonfunctional pads. On plane layers, a vast majority of pads are nonfunctional, since only the ground or power connections are made. Conversely, on the signal layers the ground layer pads are similarly isolated. There are many opportunities to increase spacing without impacting the available plane area.

As you polish up the design of your castle, er, circuit, pay attention to the moats. An extra mil of clearance will make a big difference. The extra time spent will be worthwhile and improve your curb appeal. ▫

FIGURE 3. The autorouter might not center traces between pads or take an inefficient angle.

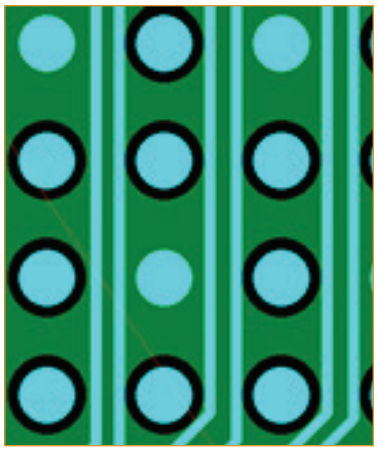


FIGURE 4. Smaller nonfunctional pads can increase embedded clearance.

Designer's Notebook, continued from pg. 20

your cookies together with a gob of chocolate or use solder paste to create electrical and mechanical bonds between your components and boards.

Placement strategies for rework. Keep-out regions around a BGA permit a rework nozzle to seat around the perimeter, so hot air can reflow the component without removing other parts. Leaving the area around the BGA clear permits ground pour to surround the device. That isolation helps with the thermal challenges by providing a heat spreader on the board. It may also be useful to contain electromagnetic interference with other devices. Most discrete components will be fine at a short distance or placed on the bottom of the board.

Speaking of small components, assemblers often have a spacing guide that considers the orientation of passive devices. Side-to-side spacing will have a smaller gap than side-to-end or end-to-end spacing. Reason: to provide access to the toe fillet for the soldering iron. Building those rules into the footprint is good.

Better still if the layout software controls the spacing numerically. The design-for-assembly feature allows the same footprint to be used with different placement density levels. This is more flexible than a one-size-fits-all courtyard. Taller components require more space. Some connectors need extra area for actuating the retainment hooks. SMA connectors should have room to get a little wrench around the coax connector. Consider assembly and disassembly for troubleshooting.

Routing guidance for reworkability. Fanning out a through-hole connector or similar component using the bottom layer provides access to the traces, so they can be cut more easily. Avoid the situation where a component must be removed to do the rework. It is possible to cut an inner trace with a controlled depth slot, but it might be difficult to find a place to make the incision without harming other traces.

Test points can be used to solder down a jumper wire. Even if the majority of the nets lack room or cannot afford the test point for impedance reasons, adding test points on the external power and ground plane areas will make it easier to change the voltage of a device should the need arise. Even when a PCB is designed as a low-volume test fixture, there is a chance it will become a product or a ship-along item for a customer. Design everything as if it could be a mass production run.

Designing for rework, repair and troubleshooting goes hand in hand with other DFx practices. Board designers who also work on the bench will be familiar with the common problems. Removing an RF shield wall in order to replace a filter is a pain. Thinking ahead and providing a little breathing room reduces that pain. We could all use a little pain-relief now and then. ▫

Education Unlocks the Golden Door to Freedom

"Education is the key to unlock the golden door to freedom."
– George Washington Carver

THIS MONTH I speak with the PCEA Educational Committee regarding the team's take on the PCEA's role in education. What do they have in store? Next, PCEA Chairman Steph Chavez weighs in on the strength of the Education Committee and why it is crucial to the PCEA's mission. Finally, with our normally provided list of professional development opportunities and events, I give a preview of next month's column.

PCEA updates. The PCEA Educational Committee discusses the importance of well-rounded technical curricula, as well as how they started in the industry. It covers PCEA educational resources, including technical books, papers, and lunch-and-learn webinars, as well as chapter presentations and field trips. Upcoming presentation topics include materials, high speed, advanced placement and routing, power distribution, and flexible circuits. You will also learn more about the PCEA's mentor pairing program.

Kelly Dack: Today, I am speaking with Rick Hartley, Mike Creeden, Tara Dunn, Gary Ferrari, and Susy Webb. Thank you for coming together as members of the PCEA Educational Committee. One of the main goals of the PCEA, along with collaborating and inspiring the electronics community, is to find ways to engage our membership in the realm of education and seek out ways to fulfill their needs. How is that going?

Rick Hartley: Over the past few months, as we were generating content for our website, we brainstormed ideas about what to offer our audience and how best to reach them. What you are going to hear from us are efforts to share knowledge with our industry peers.

Susy Webb: Our website is chock-full of technical information. We provide informational links to guide industry professionals through links to technical papers. The topics range from general electronics theory to high-speed SI, EMI, power, flex design, HDI and DFM. It is a very comprehensive list.

Mike Creeden: Not only do we provide a full page of content links under our technical info section, we also have another full page of references in our books section. We list works from authors including Bruce Archambeault, Eric Bogatin, Clyde Coombs, Clive Maxfield, Christopher Robinson, Lee Ritchey, Howard Johnson, and many more.

Dack: Let's talk more about what value-added content the PCEA Educational Committee is bringing to the electronics PCB engineering community. Do you have any plans for programs offering financial assistance or scholarships for young engineers?

Creeden: We have a spot explaining our mentor pairing program on our website. Our website is becoming quite automated, and we now have a way of taking feedback request data entered on the site and matching it with other solution data on the site.

Readers can find that on the education page of our website under the topic "mentor pairing." It is a very simple process to sign up for this service. We have a section to fill out if you would like to be a mentor or be mentored. Then, we have a place to fill in your areas of expertise and the software you use or are proficient in. This keeps users of the same category of software tools in the same family. We make the introduction to facilitate the mentoring relationship but then allow the mentor and mentee to take it from there. We feel this is a very good solution to fulfill the collaborative commission we speak about.

Dack: Gary, you've served quite a lot in the PCB fabrication industry. How did you get your start? Were you mentored?

Gary Ferrari: I did not have any mentors on the electronics side. On the mechanical side, I was mentored in castings and other machine gears and metals technology through meeting contacts and by job shopping in the early years. Even as I moved around the country, I always had friends. Wherever you work, you should make connections and find somebody to share knowledge with. It's about planting seeds for lasting relationships.

Dack: You learned on the job from coworkers and peers, which transformed into a network of friends and colleagues you could tap into for advice wherever you found yourself.

Susy, you teach so many PCB design classes. Where did you fill your head full of knowledge early on?

Webb: Back then, PCB layout was an art. Now, it is definitely an electrical engineering trade, which is dramatically different. I gained a lot of knowledge by attending the many electronics trade shows and conferences that began to spring up, especially in the '90s. I learned so much from the speakers at these

KELLY DACK, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). Read past columns or contact Dack; kelly.dack.pcea@gmail.com.

shows that I felt a compelling need to share the knowledge I'd gained with others, so I started teaching my own subjects at these conferences.

Dack: Tara, I know from firsthand experience you are well-versed in teaching and mentoring folks in the electronics industries about flex circuit manufacturing and flex design and DfM. Did you start with a mentor?

Tara Dunn: I got my start in the electronics industry just out of college, working for a small flexible circuit manufacturer. Working with a small company provided the opportunity to wear many hats and learn the PCB fabrication process and industry quickly. I was fortunate to work with several mentors helping me understand both flex technology and the PCB industry in general. Because of the foundation that effort provided me, I feel strongly about mentoring and helping others new to the industry, or new to flexible circuits.

Hartley: In addition to what we mentioned earlier, there will be a great emphasis on local presentations to our local chapters whose members have incredible backgrounds and much to share.

Dack: Susy, you emphasize the importance of going to these shows to connect and learn. Do you feel a need to facilitate education by getting your students out of the classroom and into a PCB fab shop or EMA site for a more tactile learning experience?

FIGURE 1. The PCEA Education Committee.

Webb: Getting our membership out to see the equipment that makes design so important is not to be underestimated. This practice has been implemented in many of our local chapters over the years. We have discussed ways of doing this in a virtual fashion recently with Covid-19. But there is nothing like showing up at a PCB shop with boots on the ground. It makes it easy to ask spontaneous questions and get feedback. Without feedback, it's hard to become a good designer.

Creeden: Rather than tell stories of mentoring, which people don't fully get, I explain it like serving as an apprentice under the guidance of a tradesman. We all grew up in the companies that hired us, and they modeled the designer hierarchy similarly by calling us junior designers. As we gained knowledge, we became designers and then senior designers. The electronics industry has bypassed that system of gradual learning. Without understanding the complexities of the trade, management now just hires a new engineer and says, "Here is a 32-layer board design that will require HDI. Get 'er done."

Our industry has lost the apprenticeship. New EEs today may have taken a couple of day courses in PCB layout or can find a 40-hour class offered by an organization, but there is nothing that will systematically build our profession like the unions of the trades.

Dack: In a sense, all company structures can facilitate an apprentice program in some way if they have the experience within their staff. But if their staff is inexperienced, they may suffer from intellectual inbreeding. Is this where the PCEA comes in? Does meeting within a local chapter fill this gap of outside knowledge by bringing it into the chapter via presentations?

Hartley: Not only that, but it couples with the mentoring we discussed earlier. Combatting intellectual inbreeding requires getting out of the office and being subject to new ideas and methodologies. Our presentations and mentoring are not only about learning a software tool; it can also be about a method or a process. A junior designer could mentor with any of us in the PCEA. Besides some colorful language, who knows what they could learn! (laughs)

Webb: It is important to continue this type of education throughout your career because if you have designed only one board – and you think that if it was somehow built successfully, you are a board designer who can design anything – you might be surprised. The importance of continued learning is critical because the next board design could have an entirely different scheme of technology that could cause you to fail miserably.

Ferrari: I've mentored several people over the years about how to grow their long-term career paths. I've guided them to look to the future and where they want to go. Mentoring is all around, and we want to be a part of it because we feel we have the right experience in the PCEA to help. Our local chapters are dialed in to help, too. There is a lot of opportunity in our local chapters to ask questions and get help through presentations and peer review.

Dack: It's good to hear about your progress and plans for the upcoming months. Thank you deeply for your service to the industry.

Message from the Chairman

by Stephen Chavez, MIT, CID+

Another month has gone by, and I am still amazed at how the PCEA continues to expand globally, as each day, week, and month comes and goes. So much positive activity is taking

place regarding the PCEA, as our membership continues to grow along with our sponsorships. As I collect my thoughts on all the activities taking place, I feel a sense of euphoria still in the air from our grand opening in early July.

When I think about the powerhouse of industry professionals on the PCEA Education Committee, the first word that pops into my head is "wow!" The PCEA Education Committee is made up of five main individuals whose combined industry experience is easily over 200 years. The PCEA is blessed to have the following individuals that make up the Education Committee:

1. Mike Creeden, technical director of design education, Insulectro (vice chairman of the PCEA)
2. Tara Dunn, president and founder, Omni PCB
3. Gary Ferrari, executive consultant, Ferrari Technical Services Inc.
4. Rick Hartley, principal engineer, RHartley Enterprises
5. Susy Webb, senior PCB designer, Design Science PCB

At the core of the PCEA, our mission is to collaborate, inspire, and educate. These five people have been doing that daily for a very long time. They are more than industry professionals; they are close and dear friends whom I have had the pleasure to come to know for over 15 years.

At many industry conferences and workshops around the world, Mike, Tara, Gary, Rick, and Susy bring it. They pack the house every time they step up to the microphone, walk on stage, or set up to lecture as a featured speaker on many industry webinars. These five professionals are true industry icons. When I think about how blessed the PCEA is to have these five amazing professionals that make up our Education Committee, I strongly feel we could not be in better hands as we move forward.

Again, the most important thing that our PCEA Education Committee brings to the table is its combination of over 200 years of industry experience, along with endless wells of industry knowledge when it comes to printed circuit engineering.

If you have not yet joined the PCEA, I highly encourage you to do so by visiting our website (pce-a.org). I continue to wish everyone and their families health and safety.

Next Month: Chapter Reports

You can distance this body but not this mind. You can't keep good folks down. This virus has certainly tried, but our PCEA chapter leaders have been working in the background to plan events to bring the membership in local areas together. Next month, I am looking forward to pulling our local chapter leadership together for some behind the scenes reaction to the challenges of Covid-19 and what they are doing to overcome its attempts to shut down our collaboration engines: the local chapter meetings.

Our chapter activities are coming alive, and our membership is benefitting from the synergy of their collaboration. Please look forward to my Zoom meeting interview with this dynamic group of leaders in next month's column.

Professional Development and Events

- Sept. 8–Oct. 13, 2020: PCB West Virtual 2020
- Sept. 28–Oct. 23, 2020: SMTA International – Virtual
- Oct. 7–9, 2020: AltiumLive – Virtual
- Mar. 6–11, 2021: IPC Apex Expo (San Diego, California)
- Apr. 13–15, 2021: DesignCon (Santa Clara, California)
- May 5–6, 2021: Del Mar Electronics & Manufacturing Show (Del Mar, California)
- May 11–13, 2021: IPC High-Reliability Forum 2021 (Baltimore, Maryland)
- Nov. 10, 2021: PCB Carolina (Raleigh, North Carolina)

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

See you next month or sooner! ▫

The Case for a 1.1mm BGA/CGA PACKAGE

A marginally larger package would cut design times and improve PCB yields and performance. **by GERRY PARTIDA**

Most electronics engineers know there is no 1.1mm BGA or CGA package. Because we are forced to use a 1mm pitch package, we live with tradeoffs. A slight increase in the pitch size, however, could satisfy the needs for today's high I/O pin count designs.

This conclusion comes from my observations of building Class 3 and aerospace 1mm pitch products, and the challenges, setbacks, redesigns, returned product, and field failures we all endure.

Ideally, we would have the following allowances in a design for performance, layout, compliance and yield:

- The ability to double tract conductors between via lands.
- Conductors not less than 0.004".
- Spacing between conductors not less than 0.004".
- Drill-to-copper distance of 0.010".
- Drill diameters of 0.010" and aspect ratios less than 12:1.
- Annular ring that meets Class 3. (Design should have a land 0.014" over the drill size.)
- Meets copper plating in the hole 0.001" minimum (IPC-6012 Class 3).
- If via-in-pad, epoxy fill that meets IPC-6012.
- A design that passes OM reflow (IPC-TM-650, method 2.6.8) and thermal shock (IPC-TM-650, method 2.6.27B) testing approaching 100%.

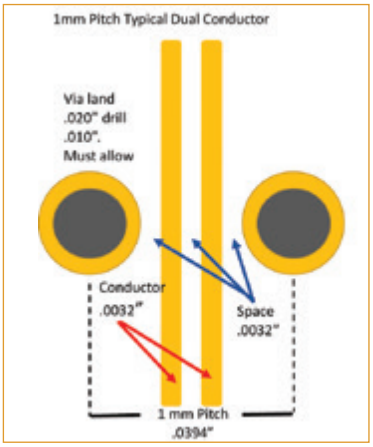


FIGURE 1. 1mm pitch typical dual conductor.

Currently the 1mm pitch does not permit this, and we enter a world of compromise and higher noncompliance results (**FIGURE 1**). Look at the tradeoffs in respect to IPC-6012 Class 3. Keep in mind for these complex builds with multiple lamination cycles, the loss of one panel can be $1,000 to $10,000 or more.

The issues for 1mm BGA pitch with dual traces include:

- Class 3 annular ring requirement is relaxed to tangency or Class 2. This gains only 0.001" additional space. Moreover, there is higher risk of breakout, nonconformance and rejection on an entire production panel.
- Drill sizes are typically reduced to 0.0079", gaining another 0.001" of space. Aspect ratio can be 12:1 or higher for the same thickness. The customer may need to relax copper thickness requirements and change from long-established minimum copper requirements. A failed cross-section results in rejection of the entire production panel.
- Dual conductors between via lands will have conductors that are 0.003"-0.0034" in the BGA package. Conductor resistance becomes a concern. Fabricator yields for innerlayer processing drop.
- Space for dual conductors limits differential pair and dielectric options. There is little room to change values or dielectric thickness. This reduces space, and also reduces innerlayer fabrication yields.
- Drill to copper internal signal layers. The best scenario is drill to copper distance of 0.009". I highly recommend 0.010" or greater for reliability and field life. Here is the reason for a distance of 0.009". Layer and drill registration will take up to 0.005" of

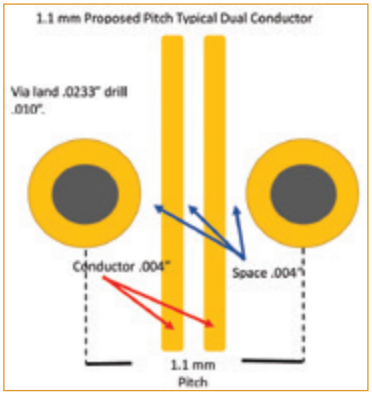
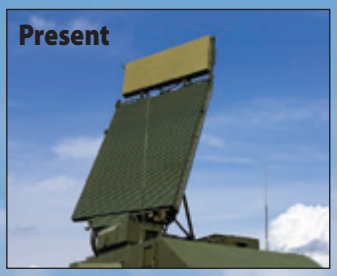


FIGURE 2. Proposed 1.1mm pitch typical dual conductor.

For military and aerospace circuits, **Rogers' circuit laminates** have been there from the start.



Material	Features
RT/duroid 5000 CuClad	Low Dk • Low Loss
RT/duroid 6002 CLTE Series	High Reliability MLB Materials
RT/duroid 6000	High Dk Materials
TMM®	Rigid Materials with Broad Range of Dk Values
TC350 TC350 Plus TC600 RT/duroid 6035HTC	Low Loss High Thermal Conductivity materials
SpeedWave 300P Prepreg RO4000 RO3000	Commercial-off-the-Shelf High Frequency Options
MAGTREX 555	Magnetically Permeable Dielectric Material

Much has changed in 60 years. Some things haven't had to: **Rogers' High Frequency Laminates**

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distance in a typical build. Dielectric removal (etchback, wicking, drill quality) typically will take 0.002". IPC-6012 permits 0.00315 for Class 3, so with normal conditions we have used up 0.007" of the 0.009" spacing budget. Finally, IPC-2221 guidelines require 0.002" minimum (worst-case condition) distance between 0V to 50V. We have now arrived at the value of 0.009".

- Drill-to-copper plane layer has the same distance rule, except the designer would like additional copper on the plane return for impedance. The impedance conductor edge is typically exactly over the plane clearance edge because they have the same exact design distance to the drill.
- Via pad and epoxy filling a 0.0079" drill bit might not meet the IPC-6012 60% fill requirement. The entire production panel could be rejected for a nonconformance condition.
- OM testing failures can increase with the smaller diameter vias.

Here is conceptually how a 1.1mm pitch device provides a win-win for everyone in the supply chain:

- The pitch is now 0.0433".
- The via land size is 0.0233" with a 0.010" drill.
  - The design annular ring is 0.0067". Assured meeting tangency, best-in-class fabricators will meet Class 3.
  - Assuming PCB thickness is 0.100", the aspect ratio is 10:1, which means no plating issues.
  - Can be epoxy-filled in compliance with the IPC-6012 60% fill requirement.
- Dual conductors with 0.004" lines and spaces.
  - Higher manufacturing yields.
  - Permits impedance line, space and dielectric flexibility.
- Drill-to-copper for signal layers 0.0107", assuming 0.0067" annular ring and 0.004" land-to-conductor space.
- Drill-to-copper can be set to 0.010" and permit "wider" copper return for impedance line. This adds 0.0007", which is better than the current zero oversize for dual conductors on a 1mm pitch.

I can imagine the impact this size package could have on our industry. Many programs suffer and respin the design just to get to the point that fabricators reach yields in the 70% range. I have seen entire programs canceled. It seems we have been forced to use package sizes dictated by semiconductor providers that have never designed or fabricated a PCB. In researching this article, I read several semiconductor design guidelines for 1mm grid pitches. I thought I was reading fiction. One even recommended a drill-to-conductor space of 0.007" for designers. Naturally, I hit the comment button and used words like "egregious."

Let's consider a different package size other than a whole number (1). We did it for 0.8mm, 0.65mm and other pitch sizes. I understand the package is bigger; for instance, a 40 x 40 1,600 I/O 1mm package grows from 1.575" to 1.732". But I have also seen there is generally enough room around these large packages and in almost all cases could accommodate the larger package.

The benefits of a 1.1mm grid package are many: faster design time, reduced cycle time, better signal performance, more current carrying capacity with a larger drill, compliant to IPC-6012 Class 3, higher PCB yields, and staying on schedule. If you believe this has merit and would like to enjoy the benefits, present this concept to your semiconductor suppliers. □

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Material Gains, continued from pg. 21

It's important for scientific and engineering communities to take on projects for no better reason than because they can. Some may have scoffed at Honda's Asimo, for example, as a hugely expensive project with little practical value. After all, the leading markets for robotics, such as automotive, are not looking for humanoid robots. So why build one? Arguably, however, lessons learned about the way humans balance and move on two legs has contributed to where we are now with the powered exoskeletons I mentioned earlier. The increased strength and endurance these can provide for industrial workers could help to defend certain jobs against the relentless advance of full automation for a while longer. At the very least, they could help protect workers against the risk of injury due to physical overstress and allow those who may be less physically strong due to factors such as gender or limb difference, for example, to compete more equally for employment opportunities.

As we continue to pursue scientific discovery and technological advancement, whether for its own sake or for more immediate objectives, blurring the distinction between humans and intelligent machines raises ethical questions that challenge us to understand what it is that makes us human. Despite these uncertainties, I'm convinced future generations will accept many human-augmentation technologies as part of everyday life and will take full advantage of these to overcome the challenges of the time. □

5 Things for Better PROGRAM TRANSFER from Prototype to Volume

Is manufacturing at scale a building block of your development plan? **by PAUL ROBERTSON, IAN HARDY and MATHIEU KURY**

Beyond conception, bringing a new product to life is a challenge. From the saying that "hardware is hard" to the number of failed product launches and missed deadlines (behind the scenes of all major consumer products we use today), we've compiled a few important lessons learned to help founders and engineers on their product development and manufacturing adventures. Too many design projects go to waste or must restart from scratch because manufacturing at scale wasn't a building block of the development plan. Here are five things OEMs and EMS companies should do to better ensure a seamless transfer of programs from proto to volume:

1. Ensure the build priorities are thought-out and communicated to the team. Don't assume the team should know your project's priorities. We like to start development builds by explaining we are not building things: PCBA, subassemblies, or finished units. Rather, we are building information, developing the process, and solving problems. The units being built will never be sold and are not useful on their own; they are a means to an end, not an end unto themselves. Do we want to solve problems 10 at a time or 10,000 at a time? When the team asks if they can move forward, even though the MES system is not set up to collect data, or asks why Lean matters in a build of 40, we ask if their solution meets the stated goals or is just a shortcut to get the units out.

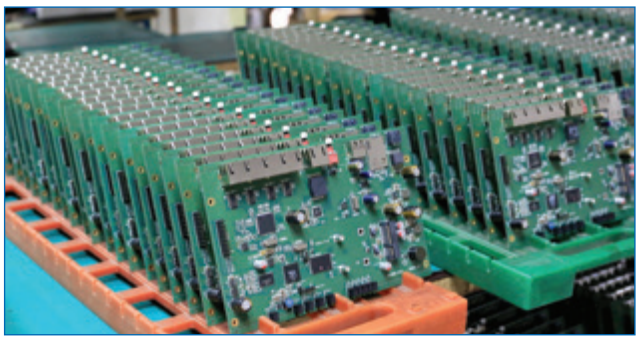

FIGURE 1. Do you scrap designs because manufacturing at scale wasn't planned?

2. Look at designs and determine what is easy and what is hard. What hasn't been done before, either at your facility or at all? What parts of the design have been done before? If the solution is known and just takes work to complete, then move on and focus on areas for which the solution is unknown. We call these areas knowledge gaps. Focus on closing these knowledge gaps early. If the team guesses at the solution to a knowledge gap, it will likely be wrong and can have big impacts on quality, schedule and cost. Use designed experiments to methodically fill in the unknowns until the process is stable.

3. Seamless transfer to manufacturing doesn't happen without a lot of planning and effort. Telling clients and project teams it can happen without this work sets a project up for failure. We tell clients and project teams we are confident we can transfer on the quality, time and cost planned, but we never use the term seamless transfer. We like to compare it to a magic trick; when done well it looks effortless and easy. The reality is there is a lot of practice, preparing the props, planning and learning. The magic can't happen without the planning and prep.

4. Think about the strategic relationship, not the revenue forecast over the next six to 12 months. Being a partner that is integral to a client's success story generates future business and spurs organic growth. The best way to not be a commodity is to treat each client as a strategic partner. If you treat a client as a commodity, expect the client to do the same.

5. Execute. Nothing shakes client confidence faster than repeatedly slipping dates on a ramp-up action plan your team has created. It communicates that either you don't know what

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FIGURE 2. Hardware development is about designing the process.

it takes to ramp to volume, or they just aren't your most important client. If an action is important enough to commit to schedule, it's important enough to complete on time. That's not to say that everything will go smoothly and as planned, but committing to the plan and the client means being flexible and finding a way to recover and hold schedule at all costs. Eventually, be it in-house or through outside engineering resources (product development firms, independent contractors, or joint-design manufacturers (JDM/ODM)), engaging with partners early is instrumental to the overall success of your project. Tackling design challenges upfront is overall a much cheaper approach than dealing with them on a production line or when all your products are returned, causing immeasurable damages to your bottom line and, more important, your brand. □

PAUL ROBERTSON is global head of new product introduction and manufacturing, IAN HARDY is senior NPI Engineer, and MATHIEU KURY is director of business development at Synapse (synapse.com), a product development and consultancy firm; mathieu.kury@synapse.com.

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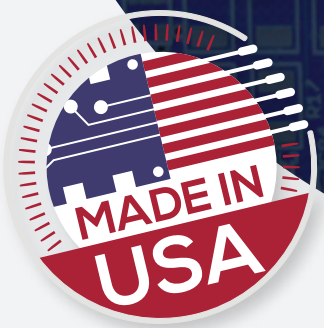

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Test Methods to Identify COUNTERFEIT MLCCS

Electrical and physical characteristics play a role in high-accuracy detection.

by YUNG-HSIAO CHUNG,[1] CHENG-HSUN LEE,[1] LIWEI XU,[1] YUQIAN HU,[1] ZONGXUAN WANG[1] and STEPHEN E. SADDOW[2]

Most multilayer ceramic capacitors (MLCC) have no marking and cannot easily be distinguished from their package, which gives unscrupulous vendors opportunities for fraud. Here, the authors introduce several test methods for MLCC compliance verification, namely 1) the effect of DC bias on capacitance, 2) capacitance temperature characteristics, 3) high-voltage testing of DCW (dielectric withstand voltage) and IR (insulation resistance), 4) cross-section (dielectric layer and terminal comparison for flex types), and 5) electron microscopy (EDS) material analysis to match with known good device chemical composition.

One important step must be performed before testing Class II capacitors. This is referred to as the "capacitor precondition test." The standard way to do this, according to Murata, is to perform a heat treatment at 150+0/-10°C for 1 hr., then let the part sit for 24±2 hr. at room temperature, then measure its electrical characteristics.

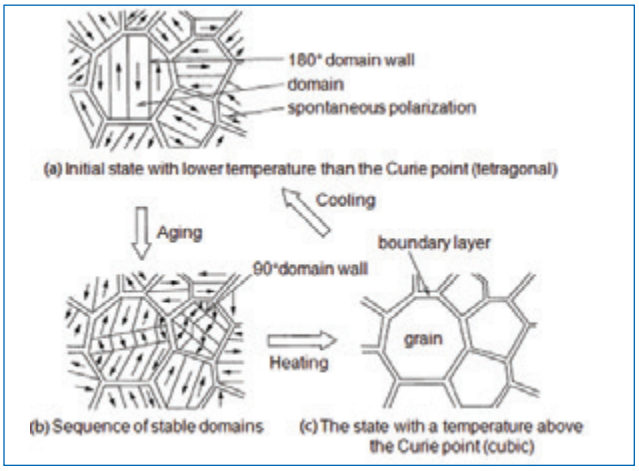

FIGURE 1. Material characteristics inside MLCC devices. The initial electric dipole orientation (a) explains how capacitors store charge, with galvanic molecular structure, while (b) shows the chaotic couple structure. The rotation of the dipoles is how capacitors lose charge storage over time. (c) Structure when temperature is above the Curie point. (Source: Murata)

TABLE 1. Industry Standard Tests for Class I/II Capacitors[1]

Class	Rated C [µF]	Frequency [kHz]	Voltage (Vrms)
I	C ≤ 0.001	1000 ± 10%	0.5 to 5.0
	C > 0.001	1 ± 10%	1.0 ± 0.2
II	C ≤ 10	1 ± 10%	1.0 ± 0.2
	C >10	0.12 ± 10%	0.5 ± 0.2

The reason to perform this precondition test is due to the characteristics of $BaTiO_3$, a typical metal-oxide dielectric used in MLCCs and the base material of Class II MLCCs (**FIGURE 1**). A decay in dielectric permittivity has been observed with these formulations, whereby the molecular structure of $BaTiO_3$ changed over time. The initial galvanic molecular structure displayed gradually transitions to a chaotic couple structure. The chaotic couple structure of the dielectric molecules has a lower ability to store charge than the galvanic molecular structure, thus causing the capacitance value to decrease. In general, this phenomenon is referred to as the aging process.

This process can be reversed via de-aging using a heat treatment. Provided the temperature of the material is above its Curie point (for $BaTiO_3$ ~125°C), and since most de-aging procedures are 150°C for 1 hr. with a 24-hr. pause, the material can recover. Once the $BaTiO_3$ reaches its Curie point, the molecular structure converts back to the chaotic molecular state, and the device is "reset."

Capacitance Measurement

Several factors may affect capacitance measurements: test signal level, frequency, and device impedance. **TABLE 1** is the industry standard for measuring Class I/ II capacitors.

4-Terminal-pair (4TP) measurement method (impedance). When using an auto-balanced bridge capacitance meter, the most common measurement technique is the 4-terminal-pair (4TP) measurement method.[2] In these measurements the

Hc and Hp terminals are shorted together, while the Lc and Lp terminals are also shorted (FIGURE 3).

The Hp and Hc terminals are often referred to as the CMH (capacitance meter high) terminal, and the Lp and Lc terminals are commonly referred to as the CML (capacitance meter low) terminals. Some residual inductance and resistance are in the cables, along with parasitic capacitance between the cables, or between the device-under-test (DUT) and ground. When the measurement is performed, parasitic compensation and calibration must be performed to eliminate these parasitic elements. Otherwise the accuracy of the measurement will be greatly reduced.

Compensation and calibration. Four types of compensation and calibration steps are usually performed: open correction, short correction, cable length calibration, and load correction. The open/short correction (FIGURE 4) is used to compensate for stray admittance and residual impedance due to the test fixture.

With these two corrections, then we can extract Z of the text fixture.

$$Z = \frac{Z_m - Z_s}{1-(Z_m - Z_s)Y_o}$$

Cable length calibration improves bridge balance stability at high frequencies, and it compensates for any phase drift induced from cable length and high frequency. Perform phase compensation before open/short cable compensation to achieve the best calibration condition for the test.

Load correction is usually performed if the testing frequency is greater than 5MHz. Since the MLCC test frequencies are all below 1MHz, we do not need to discuss this further here.

Test frequency. Test frequency can be a useful means to detect counterfeit MLCCs, especially in the common case where type Class II capacitors are substituted for Class I capacitors. The frequency test characteristics of Class I capacitors are very stable since the capacitance does not change with frequency. On the other hand, Class II capacitors display a well-known drop in capacitance at high frequencies. Thus, it is easy to determine if the MLCC is Class I or Class II by simply doing a frequency sweep. FIGURES 5 and 6 compare Class I and II capacitance during a frequency sweep from 20Hz to 10MHz:

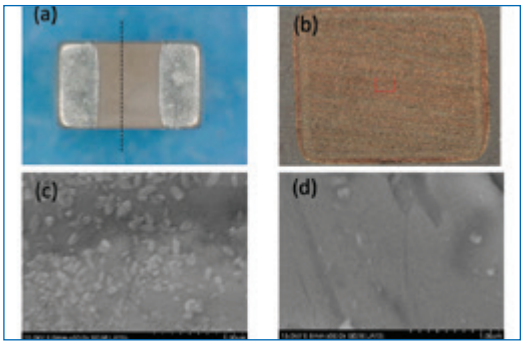

FIGURE 2. MLCC physical characterization. (a) Device cross-section location. (b) Photograph of device examined under SEM. (c) Cross-section SEM micrograph (50000X) of capacitor dielectric ($BaTiO_3$) before preconditioning. (d) Cross section SEM micrograph (50000X) of capacitor dielectric ($BaTiO_3$) after preconditioning.

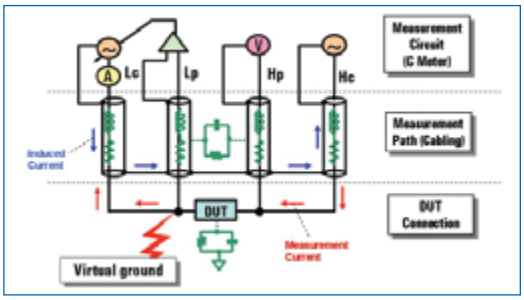

FIGURE 3. Measurement of MLCC capacitance using the 4TP measurement method. (Source: Agilent/Keysight)

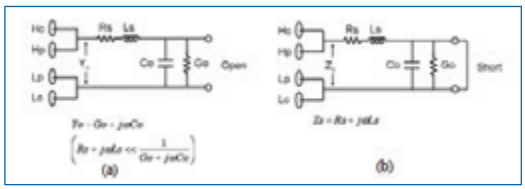

FIGURE 4. Open (a) / short (b) correction is used to calculate residual impedance and stray admittance of the test fixture. (Source: Agilent/Keysight)

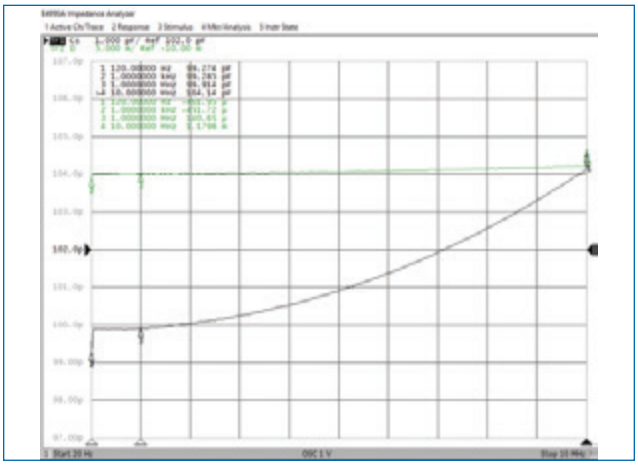

FIGURE 5. Class-I MLCC capacitance measurement. C0805C101F-1GACTU capacitance change vs. frequency (20Hz to 10MHz).

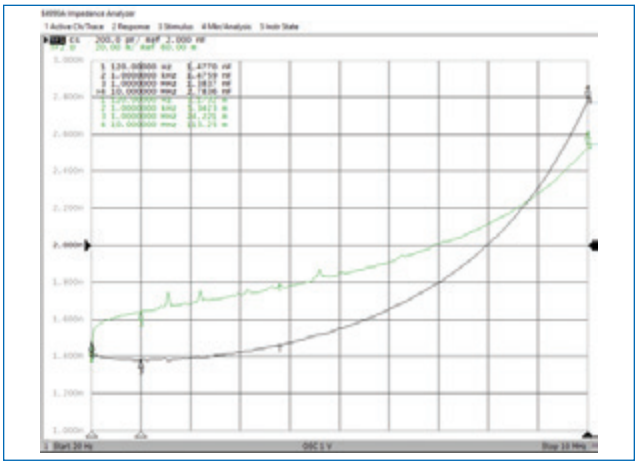

FIGURE 6. Class-II MLCC capacitance measurement. C0805C152K-DRACAUTO capacitance change vs. frequency (20Hz to 10MHz).

Frequency sweep in these two samples:

Sample 1: C0805C101F1GACTU
Rated: 100pF, 100V, C0G (class I) 1% tolerance
Sample 2: C0805C152KDRACAUTO
Rated: 1500pF,1000V, X7R (class II) 10% tolerance.

Frequency sweep 20Hz to 10MHz, E4990A Keysight Impedance Analyzer; test fixture: Keysight 16034G.

Test level. The test level will change the measured capacitance, especially for general Class II capacitors. FIGURE 7 shows data for a general Class II capacitor from Murata.

However, when the capacitance is greater than 10µF, the impedance is too low to keep the voltage at the right voltage level. In this case,

$$Z(\Omega)=R+j(-1/\omega C)$$

where

$$\omega=2\pi f$$

In this case 10uF, R is so small

$$Z(\Omega)\cong 1/\omega C=1/(2\pi x1000x10x10^{-6})16\Omega$$

To keep the AC signal in the 1Vrms level, the meter must have the ability to source the current to:

$$I(rms) = \frac{V(rms)}{Z} = 1/16 = 62.5mA$$

Also, the meter needs to function in auto-level control (ALC) mode, which will increase the output voltage on the test meter to adjust for the voltage divider. FIGURE 8 shows the measurement result without the ALC function: Voltage across the DUT was 181mV with a set voltage of 1.0Vrms. If the ALC function is enabled, the instrument will automatically raise the source voltage to achieve the desired 1.0Vrms across the DUT. FIGURE 9 shows a measurement of the same 10µF capacitor using the Keysight E4980 LCR meter with the ALC feature set to ON.

In some cases, we noticed general Class II capacitors were used to replace automotive MLCCs. Both are Class II. Therefore, the frequency method or temperature method is not able to detect the counterfeit part. However, the AC characteristic can be used in this case.

The automotive-grade MLCC capacitance is more stable vs. AC voltage variation. FIGURE 10 shows the AC voltage characteristics of the GCM32EL8EH106KA07 Class II capacitor. Compared with the general MLCC, GRM188D70J106MA73 capacitance change (loss) vs. AC voltage was 27.9% at 0.01Vrms (Figure 10), while the GCM32EL8EH106KA07 and GCM32EC71H106KA03 experienced only a 4.2% loss (FIGURES 11 and 12).

Insulation Resistance and Leakage Current

Insulation resistance is one of the important parameters used to identify counterfeit MLCCs. The different MLCCs have different insulation resistance, which depends on the application. From experience, a common method to counterfeit MLCCs is to place low specification chips into high specification packages, and then claim it as a high specification part. For some applications, the MLCC must have a higher insulation resistance. If the user chooses the counterfeit MLCC, the device/circuit performance may initially seem fine, but over time leakage current and breakdown voltage will degrade, adversely affecting circuit performance and possibly leading to device/circuit failure. This is particularly the case where low insulation resistance affects the operation of circuits intended to be isolated. Unexpected high leakage currents can eventual-

TABLE 2. Class I and II Capacitor Capacitance Change vs. Frequency

Sample	Frequency				Unit
	120Hz	1KHz	1MHz	10MHz	
C0805C101F1GACTU	99.274	99.285	99.914	104.14	pf
% diff to rating	-0.64%	-0.0063	0%	4.23%	
C0805C152KDRACAUTO	1.477	1.4759	1.3837	2.7836	nf
% diff to rating	0.07%	0.00%	-6.66%	88.60%	

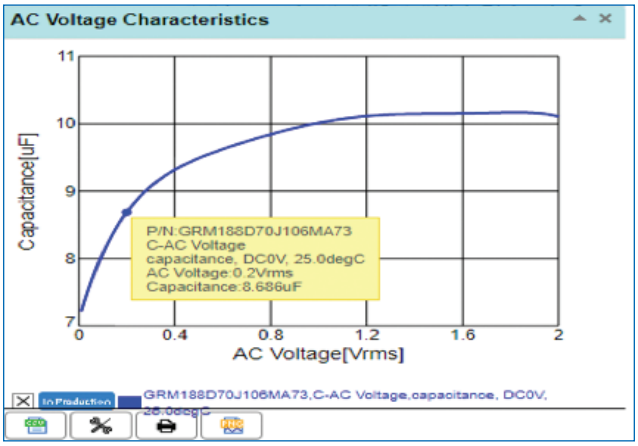

FIGURE 7. AC voltage characteristics from Murata Class II (GRM-188D70J106MA73).

FIGURE 8. Capacitance measured *without* ALC. The testing level set to 1.0V; however, the voltage monitor shows only using 181.864mV.

FIGURE 9. Capacitance measured *with* ALC on. The testing level set to 1.0V, and the voltage monitor also showing using 999.787mV.

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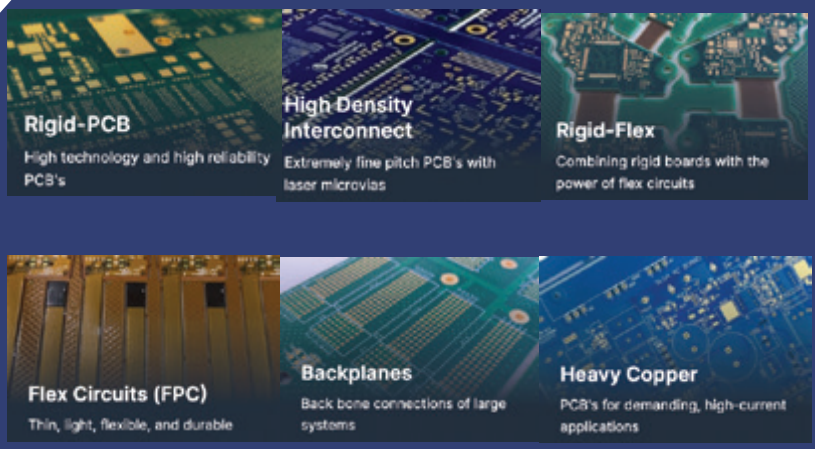

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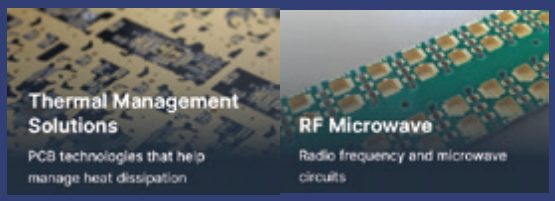

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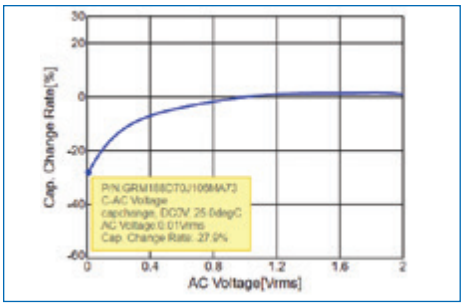

FIGURE 10. General rating class II capacitor (GRM188D70J106MA73), capacitance loss (-27.9%) at 0.01Vrms. Data from manufacturer.

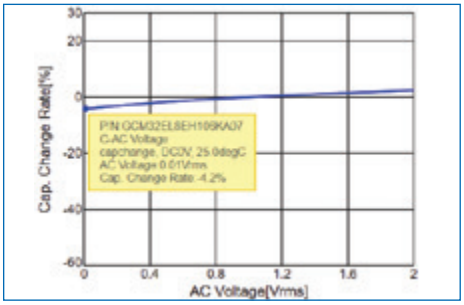

FIGURE 11. Automotive rating class II capacitor (GCM32EL8EH106KA07), capacitance loss (-4.2%) at 0.01Vrms. Data from manufacturer.

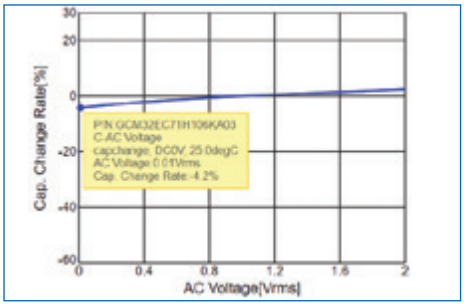

FIGURE 12. Automotive rating class II capacitor (GCM32EC71H106KA03), capacitance loss (-4.2%) at 0.01Vrms. Data from manufacturer.

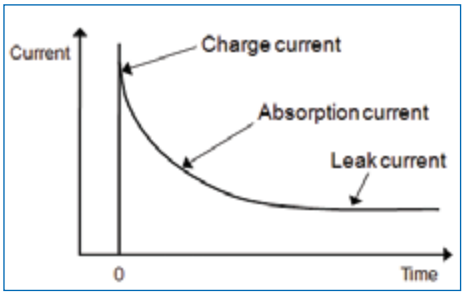

FIGURE 13. Behavior of MLCC current vs. charging time. Note three distinct current levels: charge current (peak MLCC current), absorption current (exponential decay due to device RC time constant) and steady-state leakage current.

ly lead to deterioration of the insulation by heating or direct current electrolysis. Consequently, knowing how to measure MLCC insulation resistance is one of the important methods to identify counterfeit MLCCs (**FIGURE 13**).

The insulation resistance values for MLCCs are usually very large, generally in the mega-ohms (MΩ) range. In terms of the RC time constant, the product is typically in the ohms-farads (ΩF) range or larger. For example, if the MLCC capacitance is 10μF and the minimal insulation resistance is 500ΩF, the insulation resistance equals 500ΩF/10μF or 50GΩ. This value cannot be measured by a conventional ohmmeter, as those instruments are only accurate up to ~1GΩ. We thus need to measure the insulation resistance using the electrometer/high-resistance meter and follow the procedure outlined in MIL-STD-202-302.[3]

For instance, for the Keysight B2987A electrometer/high-resistance meter, the capacitance resolution is 0.01fA, with a maximum resistance measurement of 10PΩ. On the other hand, there are two basic ways to measure leakage current: the series method and the parallel method. In the series method an electrometer is placed in series with the capacitor and voltage source (**FIGURE 14**). For the parallel method, a voltmeter is in parallel with a resistor, and then connected in the series to the capacitor and voltage source (**FIGURE 15**). The series method measures leakage current for the MLCC. From the MLCC datasheet, we apply the rated voltage to the capacitor for 60 to 120 sec., depending on the capacitance because, while we apply a DC voltage to the capacitor terminals, current will start to charge the capacitor, and, after charging is complete, the current will decrease and then level off (Figure 15). From this steady-state current we can identify it as the leakage current. In this measurement, we determine the voltage applied to the capacitor and leakage current passing the capacitor after it is fully charged. Then we can calculate the insulation resistance of MLCC by Ohm's law, R = V/I.

Since the MLCC is made using a real dielectric material with a non-zero loss tangent, which is not a perfect insulator, there will always be leakage current present. Additionally, MLCCs have a different value of insulation resistance because they are composed of different materials or combinations of materials. Therefore, low MLCC insulation resistance or high leakage current has many causes, such as device temperature and moisture, dielectric contamination, oxidation, loss of volatile materials, and material cracking. Insulation resistance measurement is especially helpful to determine the extent to which the insulating properties are affected by deteriorative influences and whether the MLCC is counterfeit or of low quality.

For example, the MLCC part no. C2012JB1A476M125AC, manufactured by TDK, has a nominal capacitance of 47μF. We used the B2987A electrometer/high-resistance meter to measure its insulation resistance by the series method (**FIGURE 16**). We set the voltage source of the meter to 10V, which is its rated voltage. From the datasheet, we found the voltage application time for the insulation resistance measurement is 60 sec., and the minimum insulation resistance is 2MΩ. Figure 16 shows a stable measurement of 59.8444 MΩ, which is higher than the datasheet spec. Therefore, we can identify the device under test as matching the manufacturer's

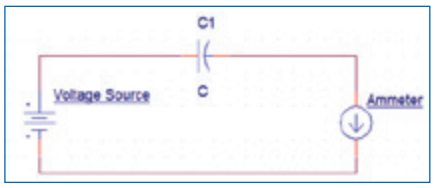

FIGURE 14. Series method for insulation resistance measurement.

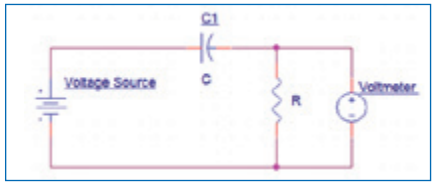

FIGURE 15. Parallel method for insulation resistance measurement.

specification. On the other hand, in FIGURE 17, we observed the insulation resistance was lower than the specification and kept decreasing as we charged the MLCC for 60 sec. Therefore, we can identify this DUT as failing the insulation resistance measurement and designate it a counterfeit MLCC.

FIGURE 16. Insulation resistance measurement of a qualified MLCC using the B2987A electrometer/high resistance meter.

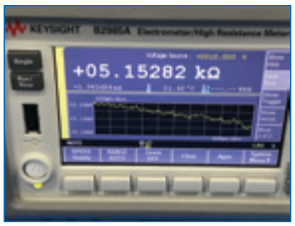

FIGURE 17. Insulation resistance MLCC failure using the B2987A electrometer/high resistance meter. Note the decay in resistance vs. time.

Dielectric Withstanding Voltage

The dielectric withstanding voltage test assesses the reliability and expected lifetime of an MLCC. Failure during a dielectric withstanding voltage test results in short circuits caused by decreasing insulation resistance and increased current, which will damage other chips on the board. The typical breakdown voltage for an MLCC is much greater than the rated voltage. But a voltage less than the breakdown voltage may permanently damage the insulation and thereby reduces its safety factor. For an MLCC, dielectric withstanding voltage failures lead to internal damage by electrical overstress cracking (FIGURE 18).

The manufacturer uses the dielectric withstanding voltage test to determine the voltage rating and verify the MLCC can operate at its rated voltage without material degradation. It is also used to assess whether the device can withstand a momentary overvoltage event due to switching spikes or surges. In other words, the dielectric withstanding voltage represents the maximum level of continuous voltage that can be applied across an MLCC. Dielectric withstanding voltage tests vary on the voltage applied or stress condition. According to military[5] and manufacturer specifications, the dielectric withstanding voltage for Class I MLCCs is usually three times the rated voltage. For Class II MLCCs, the dielectric withstanding voltage is 2.5 times the rated voltage.

For the dielectric withstanding voltage test we used a Vitrek V73, which is an AC/DC/IR hipot tester. It can provide 5kVAC/DC with a 20mA source current. As mentioned, the dielectric withstanding voltage test measures the MLCC breakdown voltage and confirms the MLCC can safely operate at the manufacturer's rated voltage. When an MLCC fails the dielectric withstanding voltage test, application of the test voltage will result in a disruptive discharge, such as a flashover, sparkover or breakdown. Additionally, MLCC deterioration due to excessive leakage current may change the device's electrical parameters or physical characteristics.

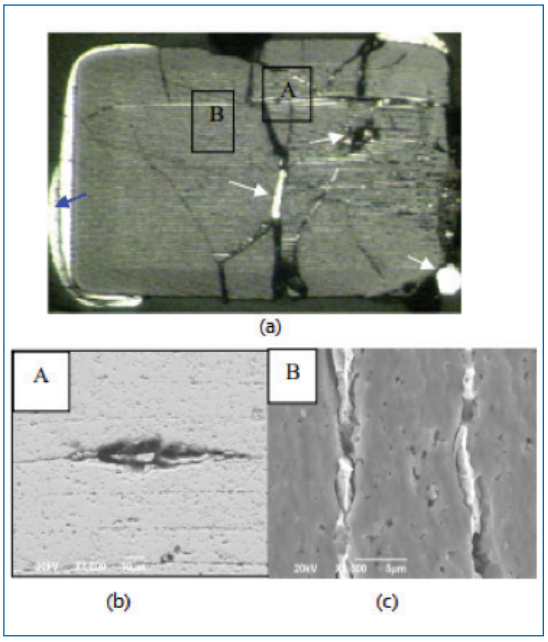

FIGURE 18. MLCC dielectric withstanding voltage test. (a) Dielectric breakdown by EOS (electrical overstress). (b, c) SEM morphology of dielectric showing a local stratification phenomenon.[4]

For example, from the datasheet for the C2012JB1A476M125AC MLCC tested in the last section, the rated voltage is 10V, has a JB temperature characteristic and is Class II. That means the dielectric withstanding voltage of the device under test is 2.5 x 10V = 25V, and the voltage application time is 1 sec. We observed no breakdown when 25V was applied to the device. The rated voltage of the device under test matches the manufacturer's specification and passes this test (FIGURE 19).

FIGURE 19. Dielectric withstanding voltage testing using the Vitrek V73 AC/DC/IR hipot tester showing the device passed the 2*voltage rating for the Class II MLCC part no. C2012JB1A476M125AC. which is expected for this class of MLCC.

MLCC DC Bias Effect

MLCCs use dielectric materials, which makes them different from other capacitors, such as electrolytic. Their materials provide a high dielectric constant (Dk) that changes according to environmental factors.

MLCCs are divided into classes based on the dielectric materials used. Two of the most common types of MLCCs used in the industry are Class I, which is temperature compensating, and Class II, which has a high Dk. Class I capacitors tend to have lower capacitance values and are more stable than Class II capacitors.

Class I MLCCs contain a low-loss dielectric and are very stable, as shown in the measured data of FIGURE 20. These measurements were taken at room temperature at a frequency of 1MHz under various DC bias applied voltage ranging from 0V to 40V.

Class II MLCC permittivity depends on the applied electric field. Therefore, with different applied voltage, the MLCC capacitance varies accordingly. The measured data in **FIGURE 21** show that the capacitance changed after performing the DC bias sweep. These measurements were taken at room temperature at 1kHz and under various DC bias applied voltage ranging from 0V to 10V.

As shown above for a Class 2 MLCC, as the applied voltage increases, the change of capacitance becomes more significant. For Class I MLCCs, however, different voltage ratings hardly affect how they perform. With this knowledge, we can tell if a part is a legitimate Class I MLCC or not based on its DC bias capacitance profile.

MLCC Temperature Characteristics Testing

As mentioned, Class II MLCCs tend to have a larger capacitance compared to Class I MLCCs. The capacitance value of Class II MLCCs changes greatly with temperature, yet for Class I MLCCs this is not the case. The following research results show how to measure the difference between these two kinds of capacitors based on temperature cycling.

The test shown in **TABLE 3** on Class I capacitors was performed at 25°C, -55°C and 125°C at a frequency of 1KHz. **TABLE 4** helps understand temperature coefficients for Class II MLCCs. The capacitance change rates (around 10% under -55°C) of Class II MLCCs are more obvious than Class I MLCCs. Thus, by looking at the capacitance change rate versus temperature, we can tell if a part belongs to Class I or Class II.

Energy dispersive spectroscopy (EDS) is a chemical microanalysis technique used with scanning electron microscopy (SEM) and widely applied to research of elemental analysis and material characterization. The fundamental principle is based on the interaction between an excitation source and the specimen. Different elements have their own unique structure, and x-rays are emitted with unique peak energy forming an energy spectrum for each sample. It is a similar, but opposite, principle behind element identification using x-ray fluorescence (XRF). In both cases photon energy is emitted; with EDS they are stimulated using electrons, while in XRF x-rays do the job.

In EDS, the specimen is illuminated with an electron beam and transfers its energy to the atom, which changes the electron state in the atom. When the electron relaxes back to its original state, energy is released in the form of an x-ray photon. EDS can measure the energy and the number of x-ray photons, called counts (cnts.). Thus, we can identify the elemental composition of the specimen, but the sensitivity of the analysis depends on the atomic number of the element and the matrix it resides in.

Cross-section and Metallography

The physical cross-sectioning of an MLCC always provides essential information to aid in understanding electrical testing of the device. It physically shows the device structure and allows easy material characterization of the metal and dielectric components. Cross-sectioning is not a means but a goal. It is a destructive metallographic technique to show the internal structure for material analysis, whereas x-ray inspection only provides information on device geometry.

Metallography was originally used on metal alloys but has since been applied to a variety of materials such as plastics and ceramics. In the IC industry, metallographic techniques are often applied during failure analysis because they can reveal the internal structure of the PCB, joint terminals and electronics inside the component package. In failure testing of MLCCs when cross-sectioning is used, check if the capacitor is soldered properly to the PCB. For example, open cracks may be found in the solder joint(s) but appear during electrical testing as a device failure, resulting in a false positive.

Besides electrical functionality tests, the other testing method to identify counterfeit MLCCs can be binned into two types: structural component and material composition characterization. These methods are more likely to allow observation of the entire capacitor from its external to its internal structure. The choice of tools and equipment is vital when performing material structure analysis. X-ray, x-ray fluorescence spectroscopy (XRF), optical microscopy or SEM are the most common tools used to perform material analysis. However, each has its limitations and, often, complementary methods are used to evaluate an MLCC structure and material composition.

X-ray and visual inspection by optical microscopy are typically nondestructive methods used to observe the sample; however, they are limited in the details they reveal. X-ray analysis can only show the rough structure, and visual inspection is limited to exterior information, such as the package and leads. In both cases they cannot reveal more about the materials used in the construction of the device. Therefore, cross-sectioning provides another tool to explore details of the device more completely and allows access to the internal material composition, such as the dielectric compounds used, which is critical to ascertain if an MLCC is legitimate. Cross-sectioning reveals the material grain structure and internal boundary conditions between the metal layers and the gap spacing. It is therefore an important technique to analyze the structure of MLCCs, with the proviso that it is a destructive test.

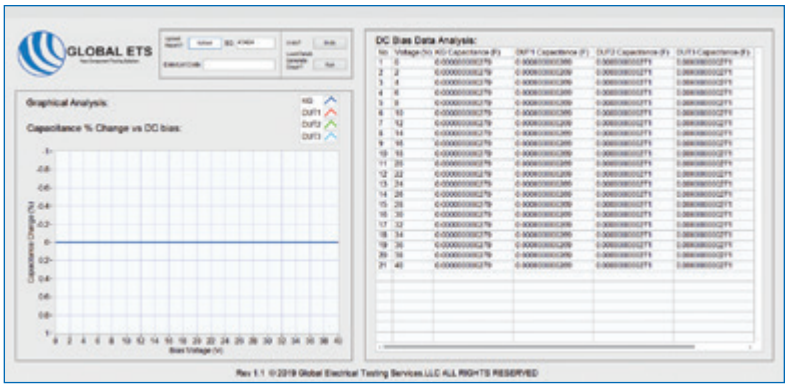

FIGURE 20. Effect of DC bias on Class I MLCC capacitance for a 270pF, C0G. Note that the capacitance did not change as the DC bias was swept from 0 to 40V, which is expected for this class of MLCC.

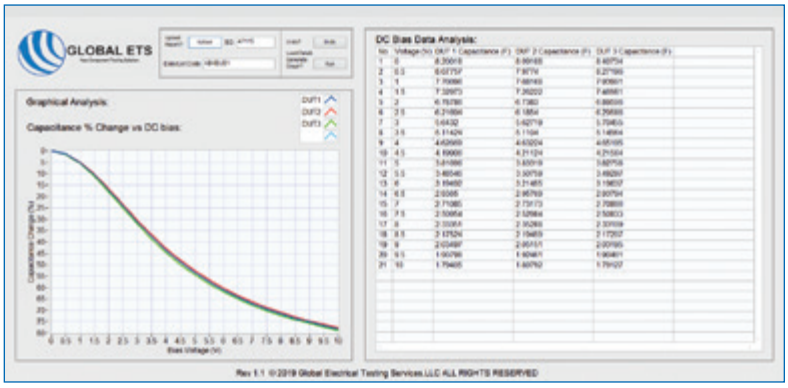

FIGURE 21. Class II MLCC capacitance for a 10µF, X5R. Note that the capacitance changed value as the DC bias was swept from 0 to 10V, which is expected for this class of MLCC.

TABLE 3. Class I MLCC Temperature Test for CL21C682JBFNNNE

From Datasheet					
Items	**Test Conditions**	**Min.**	**Type**	**Max.**	**Unit**
Temperature coefficient	-55°C - 125°C. C0G 0+/-30ppm/°C	-0.3	-	0.3	%

TABLE 4. Class II MLCC Temperature Characteristics Codes[6]

Letter Code Low Temperature	Number Code Upper Temperature	Letter Code Change of Temperature Over Temperature Range
X = -55°C(-67°F)	4 = +65°C(+149°F)	P = +/-10%
Y = -30°C(-22°F)	5 = +85°C(+185°F)	R = +/-15%
Z = +10°C(+50°F)	6 = +105°C(+221°F)	S = +/-22%
	7 = +125°C(+257°F)	T = +22/-33%
	8 = +150°C(+302°F)	U = +22/-56%
	9 = +200°C(+392°F)	V = +22/-82%

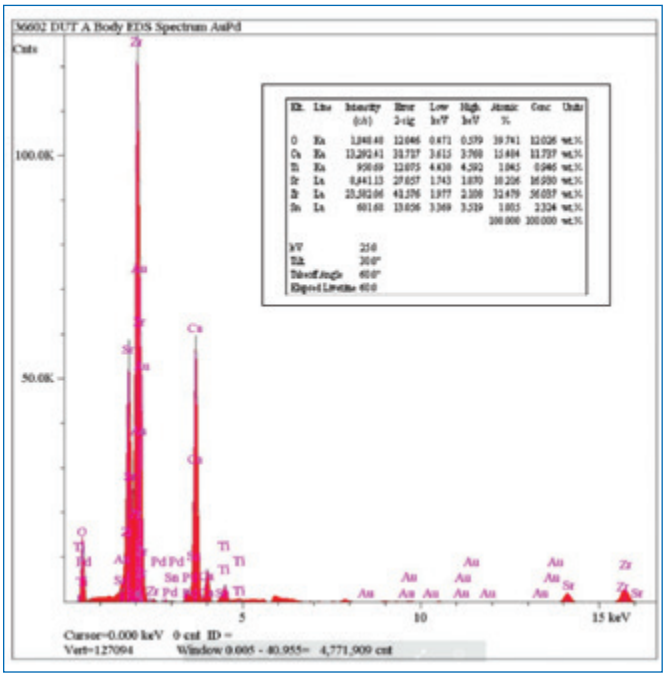

FIGURE 22. Material analysis of class I capacitor - C0402C0G500-470JNP. Note the dominant peaks are for Au, Ca, Ti, Pd, Sn, etc. Inset: relative count percentage for each element.

Metallography method. Metallographic specimen preparation can be broken down into a few steps: device mounting, sectioning, grinding, polishing, and then etching. Preparation of the sample is vital to preparing a suitable cross-sectioned device. Improper specimen preparation can contaminate the various device components, making elemental chemical analysis impossible.

Mounting the specimen encapsulates the sample in an epoxy, acrylic or polymer compound (**FIGURE 23**). This mechanically fixes the specimen within the compound to be held easily during the grinding and polishing processes and reduces contamination caused by debris migration across the sample. Additionally, the orientation should be considered when mounting the specimen. **FIGURE 24** shows the cross-section of an MLCC we want to study and the mounting orientation.

A variety of methods are used to section the specimen, such as hacksawing, diamond blade cutting or a hot flame blade for larger specimens. In the metallography for small specimens, an abrasive or precision cutter is often used. As a result, mechanical and thermal damage cannot be avoided during this type of process, but if done properly it is possible to minimize damage. This allows more precise steps that follow to accurately reveal device material with minimal contamination.

During the grinding process, silicon carbide or alumina

grit sandpaper is widely used. Grinding is always performed using water since it helps reduce heat damage and removes impurities during the process. The main purpose during grinding is to remove damage caused from sectioning.

Polishing is the final step needed to finish preparing the specimen for material analysis. With proper polishing, a fine, flat surface without scratches and deformation results. The choices of polishing abrasives are usually diamond, aluminum oxide and silicon dioxide. Polishing cloth is also used when performing gel polishing. Generally, low nap cloth is used for coarse polishing, and medium or higher nap cloth is used for final polishing.

After polishing, a chemical etching step is used to complete specimen preparation. The different metal elements in the part have different resistance levels to chemical solvents. After the etching process, the microstructure of the metals (and ceramic) parts are more obvious. Proper etching during metallography can be used on IC terminals, which are made of alloys. In the MLCC case, we care about the chemical composition of the materials that can only be obtained from part cross-sectioning. Therefore, we don't need to perform etching in this case.

Case study. **FIGURE 25** is an as-received original part before cross-sectioning and after cross-sectioning (**FIGURE 26**). Figure 26 also shows the proper orientation of the MLCC during cross-sectioning.

We use one known good device and one unknown sample device to do the comparison. **FIGURES 27** and **28** show the terminal on the left side, ceramic body and the intermetallic boundary. **FIGURES 29** and **30** show the dimensions of the MLCC and intermetallic boundary. We can see the composition and structure are the same for the known good device and test device, which indicates the unknown device is an authentic, i.e., non-counterfeit, part.

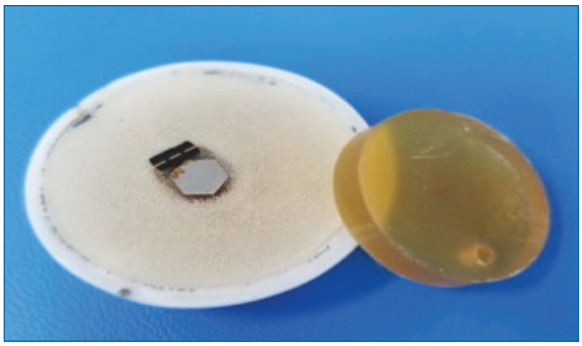

FIGURE 23. Specimens mounted in both epoxy and acrylic for cross-section processing.

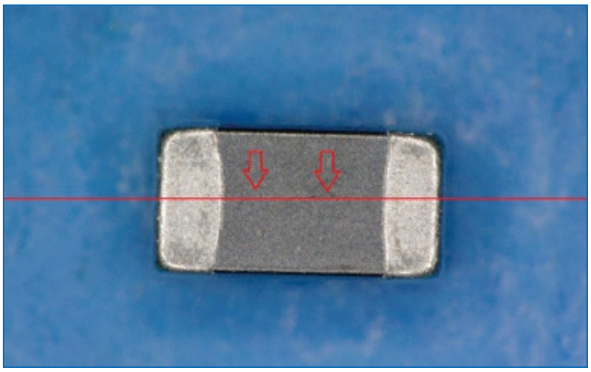

FIGURE 24. MLCC before mounting in epoxy or acrylic compound. Red line and arrows show where device is to be sectioned. (Sample dimensions: length = 1.75mm, w = 0.98mm, thickness = 0.95mm).

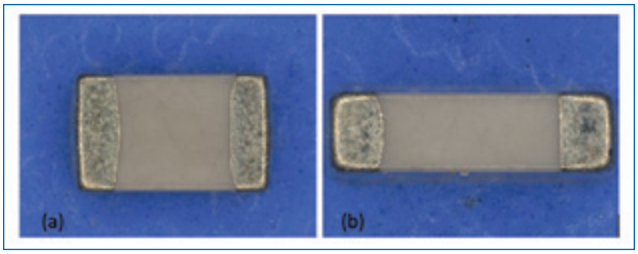

FIGURE 25. MLCC prior to sectioning. (a) Front view of capacitor under test, (b) top view of capacitor under test. (Sample dimensions: length = 2.04mm, width = 1.21mm, thickness = 0.59mm).

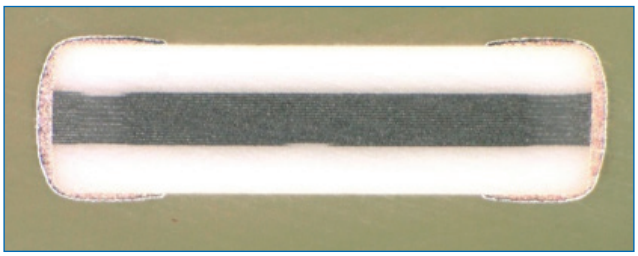

FIGURE 26. Cross-section view showing proper orientation of sample after cross-sectioning. Note metal alloy package leads (left and right) and capacitor plate layers imbedded in dielectric (white material). (Magnification: 100x).

Conclusions

Counterfeit MLCC identification is challenging. Only a few papers or articles focus on this issue. Even manufacturers are unable to provide an effective way to identify counterfeit parts. We contacted many major manufacturers, and they only provide the service to verify part authenticity via the label on the parts reel, which clearly does not solve the counterfeit MLCC issue.

Our work introduces some counterfeit MLCC case studies and several methods to help identify counterfeit MLCCs. These methods are based on their electrical and physical characteristics. Based on the electrical characteristics of the target device such as high-frequency RF capacitance, we can use a test frequency sweep. Using the MLCC high-voltage rating, we can use the dielectric withstand voltage test and insulation resistance test; for soft terminal MLCCs (vibration-proof) we can use cross-section testing based on metallography methods.

MLCC physical characteristics provide a golden sample that helps identify counterfeit capacitors, especially during physical comparison (EDS and cross-section).

A combination of these test methods successfully identifies 80% to 90% of counterfeit MLCCs. Future research will focus on the capacitor mechanical characteristics, such as bent testing, vibration and mechanical shock, etc., and lifetime testing such as moisture resistance, operational life (at high temp.),

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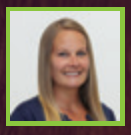

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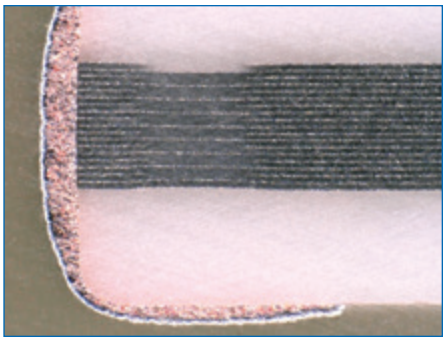

FIGURE 27. Optical micrograph of a known good device – intermetallic boundary. (Magnification: 400x).

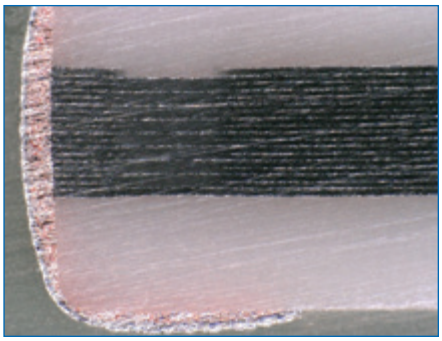

FIGURE 28. Higher magnification optical micrograph of the unknown sample device – intermetallic boundary. (Magnification: 400x).

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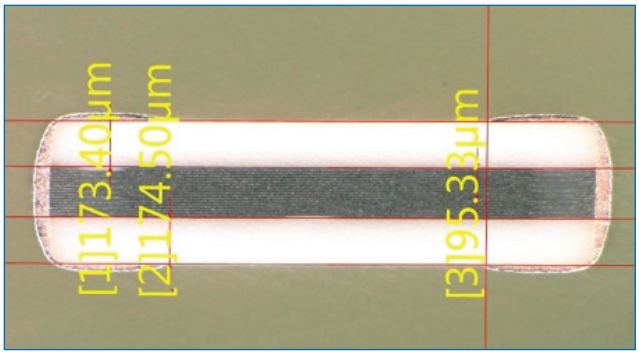

FIGURE 29. Optical micrograph of the known good device - dimensions of structure. (Magnification: 100x).

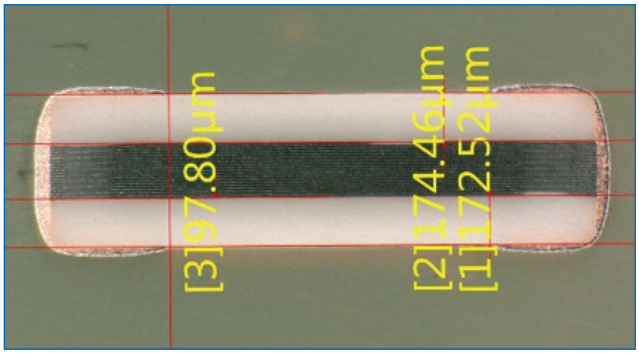

FIGURE 30. Optical micrograph of the unknown sample device - dimensions of structure. (Magnification: 100x).

SMTAI Women's LEADERSHIP PROGRAM Shows 'Drive'

Annual career development program features talks on automotive safety systems and quality. **by PRIYANKA DOBRIYAL, PH.D.**

In the wake of Covid-19, SMTA International is virtual this year, and so is the Women's Leadership Program! It is a challenging time for everyone, but we can concentrate on developing our careers by charting a positive course now. Join the "Road Trip" for a program of technical presentations, speed networking and a connection reception. Although some aspects of the WLP will be different – such as two speakers instead of three, and a completely virtual event – we believe it will still be one of the best platforms to connect with colleagues within our industry.

Virtual networking can be an effective way to build professional relationships. The virtual program this year can be especially beneficial for parents who may have to limit their travel due to family commitments at home and helpful to everyone in overcoming the challenge of obtaining travel funding. (No travel cost is associated with the virtual program this year!)

We have two speakers and three speed networking topics in this year's WLP. This year's speakers include Lenora Clark, director – Autonomous Driving and Safety Technology, MacDermid Alpha Electronics Solutions and Nancy Lange, director of Quality-Regional, Plexus.

We extend an invitation to everyone to join the Women's Leadership Program "Road Trip" to promote women in engineering fields. Support diversity in engineering fields by attending this session, which is free for everyone and all are welcome.

The event takes place Sept. 30 from 3 to 6pm Central time and is chaired by Priyanka Dobriyal, Ph.D., Intel, and Marie Cole, IBM.

Presentation Schedule

3pm: Lenora Clark
3:30pm: Nancy Lange
4pm: "Fuel Stop" speed chats with topics:

- Unconscious Bias: Real Actions to Overcome
- Keeping Your Balance While Working Effectively from Home
- Relentlessly Reinvent Yourself

5pm: The Women's Leadership Program continues its annual gathering, hosting the Connection Reception on the evening of Sept. 30.

Featured Speakers

Lenora Clark: A Cruise Through Automotive Safety Systems

Lenora Clark

Lenora Clark is director of Autonomous Driving and Safety Technology for the MacDermid Alpha Automotive Team. She leads the team in understanding all systems involved in advanced safety on the path to full autonomy. She seeks to understand industry challenges associated with this endeavor. Clark works closely with fabricators, tier ones and car makers to understand the needs of the entire supply chain to achieve faster, more reliable solutions. She works in all aspects of electronics, uniting circuitry, semiconductor and assembly solutions for a holistic approach to automotive market needs, especially for advanced driving assistance. Clark has worked for MacDermid for over 20 years and has been published in numerous industry technical conferences. She holds four patents. She graduated from the University of Connecticut with a bachelor's in chemistry and has a master's in chemistry.

Nancy Lange: Quality Requirements Across Industries – More the Same than Different

Nancy Lange

Nancy Lange has worked in the consumer product, cosmetic, pesticide, food, drug, medical device, and aerospace industries and in multiple points in the supply chain, including specification owner, contractor manufacturer, and material supplier. This presentation will take a view across those industries and share the common themes. Lange is director of quality for the Americas Manufacturing Solutions

business unit of Plexus. In this role, she provides quality leadership for the contract manufacturing services of electronics assemblies for healthcare/life sciences, aerospace/defense, communications and industrial markets across seven facilities in the US and Mexico. Key accountabilities of the role are quality strategy deployment, customer satisfaction, employee satisfaction, and quality execution.

She has worked for Plexus for two years and has prior experience with Bemis (now Amcor), Tufco Technologies, and Kimberly-Clark. She holds three patents. She graduated from Purdue University with a bachelor's in chemical engineering.

"Fuel Stop" speed chat hosts

- Martin Anselm, Ph.D., associate professor, Rochester Institute of Technology (RIT)
- Elizabeth Benedetto, distinguished technologist, HP Inc.
- Srinivas Chada, Ph.D., senior principal engineer, Stryker
- Debbie Carboni, global product manager, Kyzen
- Chrys Shea, president, Shea Engineering Services
- Brian Toleno, advanced materials team leader, Facebook □

PRIYANKA DOBRIYAL, PH.D., is technical program manager, Datacenter at Intel (intel.com) and co-chair of the SMTAI Women's Leadership Program; priyanka.dobriyal@intel.com.


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CIRCUITS ASSEMBLY

Keeping Count: Accurately Tracking Stencil Life

An RFID tag can log everything from storage location to print strokes.

OUTSIDE OF SHEER printing machine capability, the stencil is arguably the next most important element of the printing process. Stencil material, thickness, aperture integrity, sidewall smoothness (or lack thereof), and tension all play a role in the quality of the solder paste deposit. And, like all consumables, metal stencils have a lifetime: They do not last forever. Unless a stencil is damaged, tension loss is the factor that most often determines when a stencil has run its course. A properly tensioned stencil enables a good, solid release of the paste deposits onto the board. Alternatively, a stencil that has lost tension and has begun to "sag" may result in defects such as "dog ears"[1], bridges, or insufficient paste on pad, to name a few.

Today, stencil tension is more important than ever. Historically, when stencil thicknesses averaged 200µm, one was far more likely to retire a stencil from damage than from wear. Now, however, with the exceptionally thin 60µm foils required for miniaturized designs, tension loss can occur sooner, as repeated stencil pressure during the print stroke eventually reduces stencil elasticity. As has been addressed in this column, there is a proven correlation to changing tension and the output of the printing process.[2]

To ensure that stencil tension remains robust and does not become a defect factor, most manufacturers set a limit on the number of print strokes a particular stencil should see in its useful life, depending on elements such as aperture design, area ratios and application. The printer can certainly track the number of strokes for a particular job, but what if there are several stencils for that one product? Perhaps there's a spare and another for inspection? How do you know the stroke quantity of each? Manual logs are often kept to manage this, but they, too, are problematic for obvious reasons. Electronically tracking the print stroke quantity per stencil is the ideal solution to ensure that preset print cycle thresholds are not exceeded and quality protocols are reliably maintained.

Aligning with Industry 4.0 procedures, RFID tag technology now offers manufacturers a robust alternative to manual record-keeping to track stencil stroke exposure. It works like this: An RFID tag is bonded to the stencil at the beginning of its life. The printer software then monitors usage and tracks print cycle quantity for each specific stencil. Even if stencils are used on different lines or printers, the RFID technology maintains a precise record of print strokes unique to that stencil foil. The RFID can also integrate other useful information about the stencil, such as manufacturer origin or storage location for quick retrieval. All stencil data on the tag are read via RFID readers installed on factory printers or by a portable handheld scanner. Manufacturers set specific warning and machine stop thresholds to trigger new stencil ordering or halts to production. Authorization to bypass a machine stop can be assigned to specific employees to maintain quality procedures and process stability. Naturally, each stencil will have different thresholds, depending on the stencil design, the end application for the board being built and other quality criteria.

While attempts at implementing such systems have been made in the past, a lack of robustness limited their use. The stencil is moved frequently, put in and removed from storage, and must endure cleaning systems with harsh chemicals. So, the durability of the RFID tag itself and the bonding strength are critical to its effectiveness and longevity. The new technology addresses these necessary requirements, so assemblers can confidently process stencils as normal without concern for malfunction due to any chemical interaction, and while continuously writing important use data to the RFID tag. In today's dynamic manufacturing environments, where product quality is king and time is money, managing stencil use to ensure robust tension in an automated way is a welcome advance. Now manufacturers have a truly repeatable, Industry 4.0-capable method to track stencil life, provide critical traceability records, verify adherence to production protocols and ensure higher quality outcomes. ▫

REFERENCES

1. Clive Ashmore, "Dog Ears and Witch Hats," CIRCUITS ASSEMBLY, December 2019.
2. Clive Ashmore, "Stencil Tension: The Proof's in the Printing," CIRCUITS ASSEMBLY, August 2019.

CLIVE ASHMORE
is global applied process engineering manager at ASM Assembly Systems, Printing Solutions Division (asmpt.com); clive.ashmore@asmpt.com. His column appears bimonthly.

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Dendrites on PCB Assemblies

Solder joint corrosion causes.

BOB WILLIS
is a process engineering consultant; bob@bobwillis.co.uk. His column appears monthly.

THIS MONTH WE illustrate dendrites and corrosion on board assemblies. The example in **FIGURE 1** is straightforward. Saltwater was found on the surface of the metal board. It caused intermittent operation of the LED before failure at 25 meters. Yes, you guessed it: My underwater light leaked due to a rubber gasket failure. The rubber had been out in the sun too long and hardened, then cracked. The image shows chemical reaction with dendrite formation on the surface of the joints and some green verdigris.

FIGURE 2 is a dendrite under a component that caused intermittent failure. This was the result of not evaluating a new solder paste correctly after a change in solder paste supplier, plus a failure to change the reflow profile.

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at youtube.com/user/mrbobwillis. □

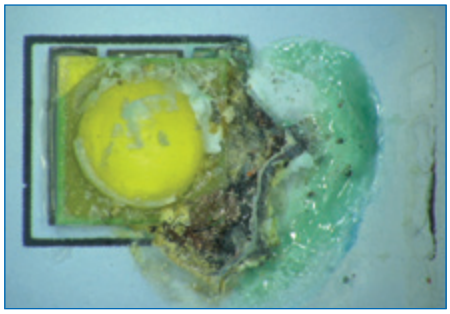


FIGURE 1. LED corrosion.

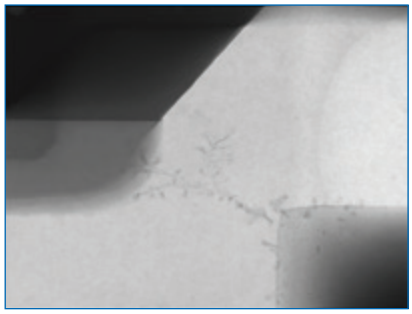
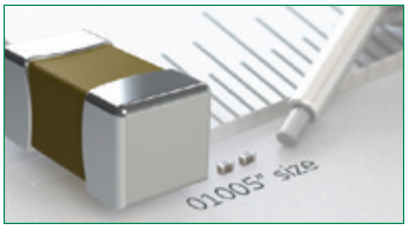


FIGURE 2. X-ray of dendrite.

DIGITAL STORAGE OSCILLOSCOPE

TBS1000C has 7" WVGA color display with up to 1GS/s sample rate and bandwidths from 50MHz to 200MHz. Software provides tips and hints throughout UI. Designed for quick hands-on learning and easy operation. Dedicated front panel controls.

Tektronix
tek.com



HIGH CAPACITANCE MLCC

GRM022R60G105M has a capacitance value of 1.0µF in 01005" size. Measures 0.4 x 0.2mm; has rated voltage of 4Vdc. Reportedly has 35% footprint reduction and 50% decrease in volume ratio compared to previous products with same capacitance value; delivers capacity more than twice that of similarly sized products.

Murata
murata.com

TEST DEVELOPMENT TOOL

ProVision 2020 simplifies testing processes through reliable and repeatable tests with high fault coverage. Includes DfT tools for initial design assessment and auto test generators. Structural and functional testing can be combined with high-speed device ISP. Test and programming applications can be reused.

JTAG Technologies
jtag.com

OTHERS OF NOTE

HIGH CAPACITANCE TANTALUM CAPS

F98-AJ6 series have max. heights of 1mm and 0.8±0.1mm and feature face-down under-tab terminations for high volumetric efficiency and high assembly densities. 0603 size is rated for 4.7µF/10V, 4.7µF/16V, and 10µF/10V and 0805 rated for 10µF/16V at 85°C with a ±20% capacitance tolerance at 120Hz. Rated for operating temp. from -55° to +125°C.

AVX
avx.com

SMT CONNECTORS

SFP-DD I/O interconnects are new double-density cages and surface mount connectors. Offer two-channel data transmission, helping data center systems enable doubled port density with faster data transfer rates. Provide data rates up to 28G NRZ and 56G PAM-4 protocols.

TE Connectivity
te.com

3-D EM SIMULATION SOFTWARE

XFdtd now addresses 5G millimeter wave antenna designs, including support for high-performance tuners and singularity correction. Includes enhancements to PCB import, allowing documentation layers of a PCB to be imported alongside geometry. Lumped circuit components specified in ODB++ and BRD files are also imported.

Remcom
remcom.com

HIGH-VOLTAGE CAPS

Tantalum Stack Polymer O 7360-43 surface mount capacitor is for high-voltage power management and high ripple current applications that require a small form factor, stable performance, and long operational lifespan. Also comes in 82µF/75V-rated voltage extension in polymer hermetically sealed.

Kemet
kemet.com

HIGH-SPEED CABLE ASSEMBLY

NearStack 100 Ohm and NearStack 85 Ohm reduce insertion loss and improve signal integrity. Optimize SI channel performance with direct linkage, bypassing board traces and use of lower loss materials. Remove re-timers and other active components from high-speed channels and reduce numbers of high-speed layers.

Molex
molex.com

SHOP FLOOR DATA ANALYSIS

InShop Industry 4.0 software provides analysis of data from across production floor to monitor operations and detect anomalies in near real-time. Improves manufacturing operational KPIs. By leveraging data collected from various machines on shop floor, including process parameters, machine utilization, and scrap data, software identifies anomalies and trends.

Frontline PCB Solutions
frontline-pcb.com

1µM FUME EXTRACTION

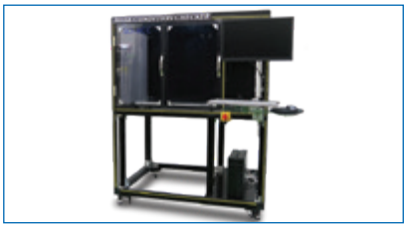
Easy Arm 1 and 2 supply a three-stage filter system to clean process air. Pre-filter (class F7) captures particles larger than 1µm size. In combined filter (class H13), micro-particles smaller than 1µm are bound, and activated carbon neutralizes harmful gases. Connect to Ersa soldering stations and rework systems.

Kurtz Ersa
ersa.com

SMT REEL BARCODE DECODER

AccuID produces a unique reel ID barcode label for each SMT component reel. Benchtop system has simple UI; operator places reel in system and scan begins automatically. Camera decodes all barcodes on reel in about 2 sec.; sends required data to database based on prefix on each label. Omni-directional decoding.

Accu-Assembly
accuassembly.com



METAL STENCIL OPENING INSPECTION

SCI-MCC (mask condition checker) checks stencil cleanliness and inspects solder residue and particle deposits after cleaning. Inspects all openings in a specified area. Each mask can be traced by registered control number. Preregistration of Gerber data not required.

Sawa
sawa-corp.co.jp

Seika Machinery
seikausa.com

OTHERS OF NOTE

DIE ATTACH ADHESIVE

Monopox EG2596 die attach adhesive offers high strength after aging. For use on PCBs to fix components and as electrical insulation. Temperature-resistant and dispensable by jet valves and needles. Drop sizes to below 250µm.

Delo
delo-adhesives.com

PH NEUTRAL DEFLUXING

Vigon NX 700 can be used in inline and batch cleaning systems. Is said to offer superior defluxing performance on PCB assemblies, especially under low-profile components. Removes a range of flux residues and is compatible with a variety of sensitive materials. Qualifies as a low-VOC product with applied VOC concentrations below 25g/L.

Zestron
zestron.com

8-ZONE CONVECTION REFLOW

GoReflow-plus has eight heating zones and active heated area of 2,980mm. Solders in ambient atmospheres and with local nitrogen inertion in peak area. High volume of circulated process gas, generated with axial fans and slot nozzles, ensures homogeneous heat distribution over transport width at simultaneously moderate gas velocities; good heat transfer rate is realized, allowing set temperatures of oven at low level. Three-stage cooling area.

Seho
seho.de

PB-FREE HYBRID FLUX

EO-Y-014 for wave and selective soldering contains organic, halogen-free activating additives and a small amount of synthetic resin. Meets temp. requirements of lead and Pb-free soldering. Alcoholic additives stabilize and improve drying times compared to conventional water or partial water fluxes.

Emil Otto
emilotto.de

HALIDE-FREE AG-FREE SOLDER PASTE

Jean-151 SN100CV ROL0 paste is silver-free and maintains fatigue strength of solder joint during aging processes at higher temp. loads. Bismuth (1.5%) aids long-term reliability. Highly printable.

Balver Zinn
balverzinn.com

FEEDER SOFTWARE PLUGIN

RCX320/340 software plugin eases integration of Asyril Asycube intelligent parts feeder and lets feeder take advantage of RCXiVY2+ high-speed, high-res vision system. Scara or cartesian robots compatible with RCX320 or RCX340 controller can rely on Asycube to sort and orient bulk components.

Yamaha Motor Europe FA
fa.yamaha-motor-im.de

In Case You Missed It

Component Assurance

"Assurance: A Data Driven Approach"

Authors: Richard Ott, Ph.D.

Abstract: The push toward globalization, combined with the proliferation of commercial and consumer products containing ICs, has led to rapid semiconductor business growth in Asia. ICs specifically produced for military applications make up a small percent of the total market, ranging from 0.1 to 1%. Due to low-volume requirements, the military is not capable of meaningful influence, resulting in a larger disparity between commercial and military requirements. Most IC fabrication and considerable intellectual property design is performed overseas, while domestic, trusted foundry options are often two to three process nodes (three to eight years) behind state-of-the-art (SOTA), with 50% higher cost. To take advantage of SOTA technologies, US military systems are forced to utilize commercially available supply chains. Offshore design, production, and independent distribution of ICs provide adversarial opportunity for malicious insertion and component counterfeiting, motivated by strategic objectives or economic gain. To combat this, while maintaining access to SOTA technologies, the US military must develop an approach to minimize platform and infrastructure risk, enabling cutting-edge capability to be delivered to the war fighter. Data-driven assurance methods provide an opportunity to deliver such capability, along with an understanding of associated risk. (SMTA Symposium on Counterfeit Parts and Materials, August 2020)

Electronic Materials

"Moisture-Insensitive, Self-Powered Paper-Based Flexible Electronics"

Author: Marina Sala de Medeiros, Daniela Chanci and Ramses V. Martinez, Ph.D.

Abstract: The fabrication of multifunctional electronic devices on ubiquitous paper substrates is gaining considerable attention due to their low cost, environmental friendliness, light weight, and flexibility. Development of paper-based electronics is subject to significant challenges, such as rapid degradation with moisture, battery dependence, and limited compatibility with existing mass-production technologies. This work describes omniphobic, self-powered paper-based electronics (R^F-SPEs), completely wireless paper-based electronic devices insensitive to moisture, liquid stains, and dust. R^F-SPEs can be rapidly fabricated through the sequential spray-deposition of alkylated organosilanes, conductive nanoparticles, polytetrafluoroethylene (strong electron affinity), and ethyl cellulose (weak electron affinity) over the surface of cellulose paper. R^F-SPEs are lightweight, inexpensive to print (<$0.25 per device), and capable of generating power densities up to 300μW/cm^2. Additionally, R^F-SPEs are flexible and exhibit excellent stability upon folding (0.3mm radius of curvature). The simple printing process and relative low cost of R^F-SPEs enable the large-scale production of self-powered, paper-based electronics toward the ubiquitous integration of human-machine interfaces. (*Nano Energy,* August 2020, https://doi.org/10.1016/j.nanoen.2020.105301)

Thermal Management

"Co-Designing Electronics with Microfluidics for More Sustainable Cooling"

Authors: R. van Erp, R. Soleimanzadeh and L. Nela, *et al.*

Abstract: Embedding liquid cooling directly inside the chip is a promising approach for more efficient thermal management. However, even in state-of-the-art approaches, the electronics and cooling are treated separately, leaving the full energy-saving potential of embedded cooling untapped. Here, the authors show that codesigning microfluidics and electronics within the same semiconductor substrate can produce a monolithically integrated manifold microchannel cooling structure with efficiency beyond what is currently available. The results show heat fluxes exceeding 1.7kW/sq. cm. can be extracted using only 0.57W/sq. cm. of pumping power. They observed an unprecedented coefficient of performance (exceeding 10,000) for single-phase water-cooling of heat fluxes exceeding 1kW/sq. cm., corresponding to a 50-fold increase compared to straight microchannels, as well as a high average Nusselt number of 16. The proposed cooling technology should enable further miniaturization of electronics, potentially extending Moore's law and greatly reducing the energy consumption in cooling of electronics. Furthermore, by removing the need for large external heat sinks, this approach should enable the realization of very compact power converters integrated on a single chip. (*Nature,* September 2020, https://doi.org/10.1038/s41586-020-2666-1)

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

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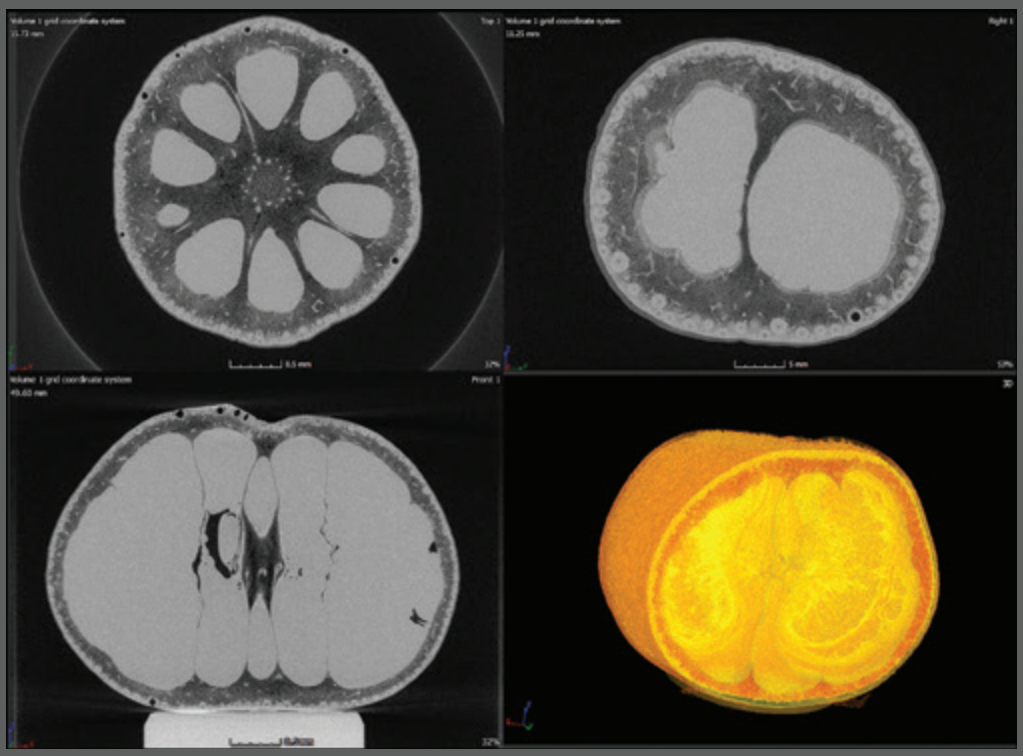

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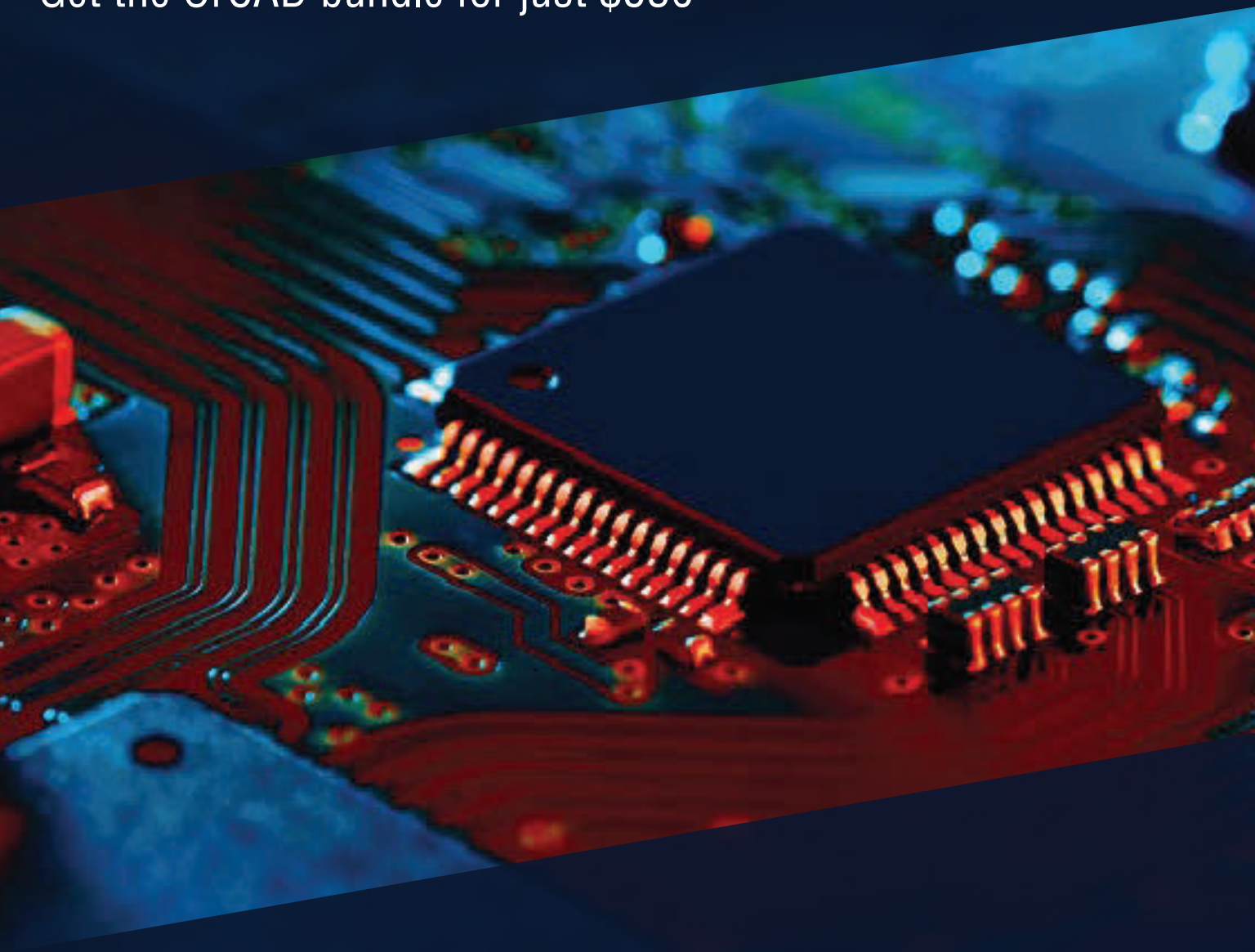

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