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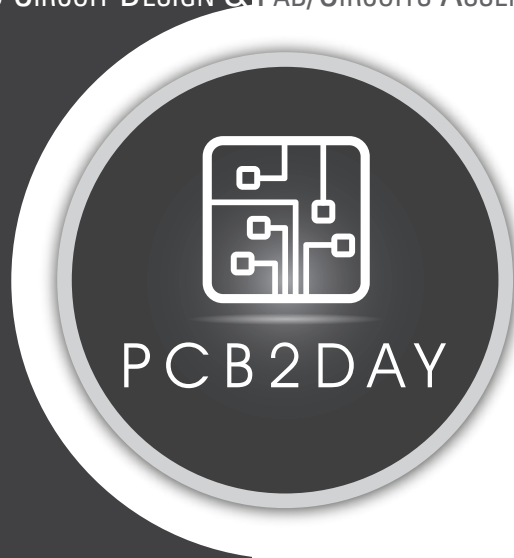
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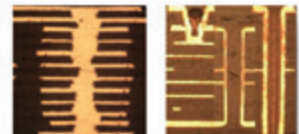


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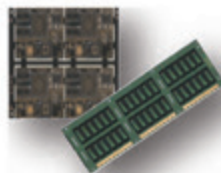
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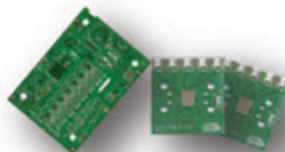
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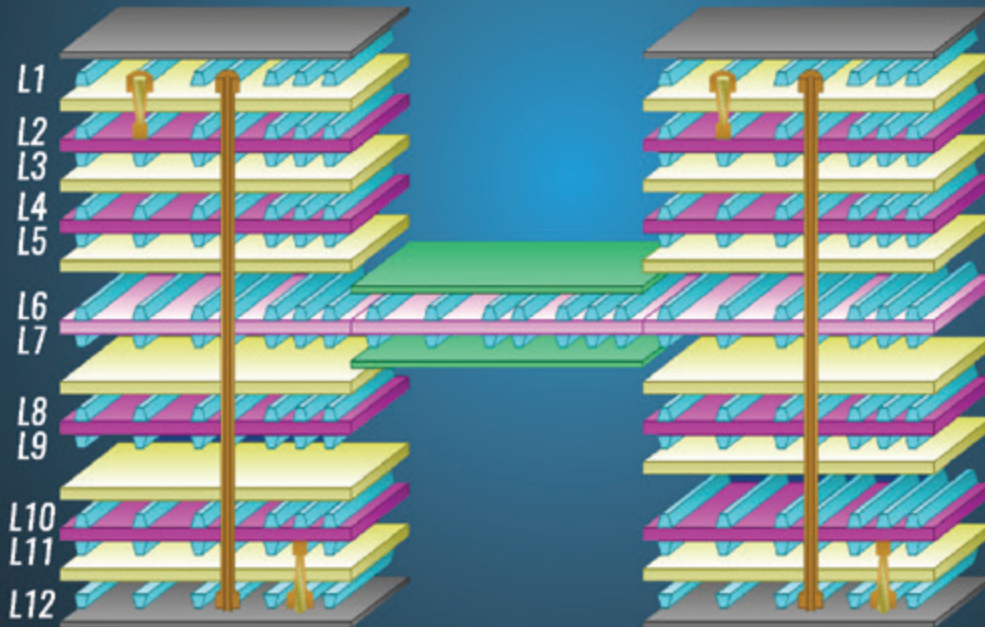


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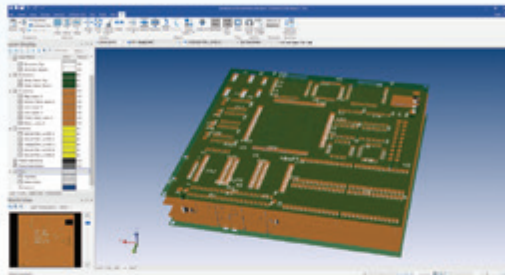
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MIKE  
BUETOW  
EDITOR-  
IN-CHIEF

# 'Future Factories' Require Thinking 'Smart' Today

**T**WENTY YEARS HAS passed since the US was a world leader in printed circuit board fabrication production. And not just in revenues, which tended to run neck-and-neck with Japan. The US also had the capability and capacity to build the largest-format boards in volume.

That was 2000.

I remember talking with Jack Fisher, then the technical director of the tech consortium ITRI, about the coming year. We were reviewing the latest bullish industry forecasts, in which some of the major fabricators were quoting lead-times of six to 12 months(!).

That unbridled optimism prompted Jack to observe that any hope of the US investing in HDI technology would be pushed out at least another year. Since order books were full for large boards, fabs saw no need to invest in next-generation technology.

Or so they thought. Because, as we all know, then the dot-com crash occurred.

It's hard to believe that was 20 years ago. But we might be edging toward history repeating.

Smart manufacturing, which is generally defined as the use of fully integrated, collaborative manufacturing systems that respond in real time to meet changing demands and conditions in the smart factory, in the supply network, and in customer needs, is quickly becoming reality.

It's been a long time coming. OEMs of assembly process equipment have long had the capability to see inside a customer's factory to perform software upgrades, view maintenance reports, and verify their machines were performing to spec. Manufacturer IT personnel, on the other hand, have historically resisted such intrusions to their networks. With IT and IP security recognized as intrinsic to operational success, most manufacturers have checked suppliers at the proverbial door.

In some of the largest EMS companies, that's changed, and it's working its way down to mid-tier companies as well. As we report in our cover story this month, Universal Scientific Industrial, which ranks 12th in the **CIRCUITS ASSEMBLY** Top 50, is all-in on an all-digital platform. Its Worldwide 5 Star Management System is bringing Industry 4.0 principles to every layer of the company. USI uses a common platform strategy to standardize the data automation protocols and equipment, and develop lead times and costs. They are making tremendous progress toward a true lights-out operation, having already reduced headcount in certain operations from the hundreds to single digits. AGVs move product from component stores to SMT lines several floors away, and inventory replenishment and vendor orders are triggered by software, not humans.

With its acquisition of AsteelFlash complete, USI can now roll out 5 Star to more than 25 manufacturing facilities worldwide.

As we reported in November, Lacroix Electronics is undertaking a similar transformation.

It has started work on the Symbiose smart factory in France, a greenfield project predicted to have 60% more output than similar-sized plants yet with the same number (450) of staff when it opens this year. The company is committing \$30 million toward a 205,000 sq. ft. (19,000 sq. m.) facility that it expects to generate annual revenues of more than \$120 million. Lacroix will use industry-developed open source IoT communications standards for its digital factory.

At its Shanghai smart factory, USI builds SIPs for smartwatches. Lacroix is heavily vested in automotive. Both are lower-mix, high-volume segments. It is predictable, then, that domestic North American assemblers will say, "Good for them, but it doesn't apply to me."

That's what we heard from fabricators two decades ago.

One person who has studied the implementation of the smart factory matter deeply over the past year believes the US is five to seven years behind Europe and as much as 10 years behind the leaders in Asia.

How many fabricators wish they could go back in time and invest in a laser drill or five? The US misplayed the technology game at immense cost to the region. The idea that assembly is somehow insulated from a similar outcome is wholly misguided.

The US shouldn't cede entire markets, as it currently does with consumer and mobile, thinking that aerospace, defense and medical are permanently sustainable and impervious to foreign competition. Fabricators learned the hard way that you can't always depend on what you have now.

Instead of saying, "Convince me," it would behoove North American shops to say, "Catch me up." And then act accordingly.

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P.S. We are pleased to bring back the PCB East conference and exhibition to the Boston area in May. Check out the details at [pcbeast.com](http://pcbeast.com).

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### WHO'S ON BOARD?

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## PCDF People



Altair appointed **Matthew Brown** senior vice president and chief financial officer. Brown previously served in finance leadership roles at NortonLifeLock, including as interim CFO from November 2019 to July 2020.



Altium promoted **Christopher Donato** to head of digital channel. He's been with the company in account management and sales positions since 2004.

CMR Surgical named **Jesus Castane** senior PCB engineer.

**Kent Balius** and **Ken Smythe** have launched EPIC Front-End Engineering.

## PCDF Briefs

**Amazon** has shifted part of the computing for its Alexa voice assistant to custom-designed chips, aiming to make the work faster and cheaper, while moving it away from chips supplied by **Nvidia**.

**Apple** has selected WLCSF/fan-in for its latest iPhones. Apple is expected to ramp up flexible circuit demand for its 2021 devices, and is looking to work more closely with **ZDT, Compeq, Unimicron** and **Career Technology**, according to reports.

**Amphenol** will acquire **MTS Systems** for approximately \$1.7 billion, including assumption of outstanding debt and liabilities, net of cash.

**Calumet Electronics** is expanding its PCB manufacturing operations in Michigan to meet market demand.

**China** is stepping up the development of homegrown EDA software and systems as part of its efforts to boost self-sufficiency in semiconductor, and many EDA startups have become operational with government subsidies, according to reports.

**Delta Sigma** will use **Zuken's** Harness Builder for E3.series for its electrical harness design.

**Firan Technology Group** achieved Nadcap accreditation and certification at its PCB manufacturing facility in Fredericksburg, VA.

**IMI Inc.** successfully completed an intensive audit to IPC-1791, *Trusted Electronic Designer, Fabricator and Assembler Requirements* and has earned a Qualified Manufacturer's Listing under IPC's Validation Services program.

**Jingwang Electronic Technology's** new 157,000 sq. m., \$175 million PCB fabrication campus is expected to open this year.

## 3D Glass Solutions, Nokia Collaborate on D-Band Signal Transport

**ALBUQUERQUE, NEW MEXICO** – 3D Glass Solutions collaborated with Nokia to deliver D-band signal transport. D-band signal transport requires integrated mm-wave modules with high spectral-efficiency. 3DGS worked with Nokia to develop a demonstrator for ultra >30Gbps speed wireless backhaul systems.

"This solution allows designers in D Band TX/RX modules the lowest loss and lowest cost point for TX/RX modules, as demonstrated by this radio-on-glass architecture for Nokia, operating up to 160GHz with less than 1dB of loss from the chip to the antenna output/input ports," said Jeb Flemming, CTO, 3DGS.

"One of the reasons we've been able to achieve such extraordinary performance numbers using our RFIC on glass is because we've been working closely with the engineers at 3DGS," said Shahriar Shahramian, director of sensing and communication ASICs research, Nokia Bell Labs. "Its unique etching process allows us to build things on glass that simply aren't possible using any other process. At the same time, 3DGS' willingness to collaborate and explore unexplored areas and applications has allowed us to build something incredible."

"This is the next generation of ultra-high-performance radio-on-glass modules operating at these frequencies," said Flemming. "Our demand for data continues to grow, and we are pleased to work with Nokia to deliver record-breaking solutions that can keep up with that demand." (CD)

## Altium to Sell Tasking Business to PE Firm

**SAN DIEGO** – Altium will sell its Tasking business unit to a private equity group for more than \$100 million in what the ECAD company is calling a "strategic divestment." FSN Capital, a European private equity firm, will pay up to \$110 million for Tasking, \$10 million of it conditional on the company hitting certain revenue targets in the 2021 financial year.

The deal will close in the second half of Altium's current fiscal year, which ends in June. Altium will instead focus on its PCB design software.

Tasking produces embedded systems development software. The unit recorded flat sales of \$20 million in Altium's fiscal 2020 due to Covid-related market issues.

"While Tasking is a great business, it does not play a central role in our design to realization strategy for the electronics industry, which is being delivered through our new cloud platform, Altium 365," Altium said in announcing the deal.

"The strategic divestment of Tasking, combined with our recent organizational changes and hard pivot to the cloud, marks an inflection point for Altium in its pursuit of industry transformation," said Aram Mirkazemi, chief executive, Altium. "The divestment of Tasking will free up organizational capacity and allow Altium leadership to focus on our main game, which is to expand Altium 365 and accelerate its adoption."

Altium acquired Tasking in 2001.

On Nov. 19, Altium guided for fiscal 2021 full-year revenue of \$200 million to \$212 million. Announcing the Tasking deal, it reiterated that guidance, less Tasking, implies a lower forecast for its PCB tools going forward in calendar 2021. (MB)

## Infinera Wins Best Overall Design in Mentor's PCB Design Awards

**WILSONVILLE, OR** – A team from Infinera and Jabil has been selected as designers of the best overall circuit board by a group of industry experts under the auspices of Mentor. (Mentor is now officially Siemens EDA.)

Now in its 28th incarnation, the PCB Technology Leadership Awards recognize engineers and designers who use innovative methods and design tools to address

complex PCB system design challenges and produce industry-leading products.

The contest is open to any designs created with Mentor PCB solutions. Judging is based on design complexity and overcoming associated challenges, such as small form factors, high-speed protocols, multi-discipline team collaboration, advanced PCB fabrication technologies, and design-cycle time reduction.

Experts in the PCB industry judged entries from around the world in categories representing computers, blades and servers, memory systems; consumer electronics and handheld designs; industrial control, instrumentation, security and medical applications; military and aerospace solutions; telecom, network controllers, line cards; transportation and automotive designs.

The panel of judges this year included Dr. Rajan Bedi, Stephen Chavez, Mike Creedon, Gary Ferrari, Rick Hartley, Steve Herbstman, Happy Holden, Pete Waddell and Susy Webb. (CD)

## Emerald EMS Acquires Saline Lectronic, Veris Manufacturing

**SALEM, NH** – Emerald Electronics Manufacturing Services has acquired a pair of electronics manufacturing service providers, extending its range to the Midwest US and adding capacity in Southern California. The deals also expand the EMS company's reach into the defense and medical end-markets.

Both Saline, MI-based Saline Lectronics and Brea, CA-based Veris Manufacturing are manufacturers of high-mix, low- to medium-volume printed circuit board assemblies and box-builds for high-reliability end markets, including industrial controls, aerospace and defense, and medical.

"All of us at Emerald are excited about the expanded geographic reach and manufacturing capabilities that Saline Lectronics and Veris Manufacturing bring to the mix," said Vic Giglio, chief executive, Emerald EMS. "Their addition expands the Emerald EMS footprint into Southern California and the Midwest domestically, bringing increased geographic flexibility and expanded capacity to all of our customers."

Founded in 2002, Saline is a full-service electronics solutions company with a 110,000-sq. ft. manufacturing facility providing engineering, PCB assembly, testing, electromechanical box build, and direct fulfillment for the industrial controls, aerospace and defense, medical and oil industry end-markets.

Originally known as Quality Control Manufacturing, Veris was founded in 1987. The company's 40,000-sq. ft. facility provides manufacturing and engineering services focused on the aerospace and medical end-markets.

"Our partnership with Emerald EMS will allow us to offer our customers expanded capacity, as well as access to lower-cost options through Emerald's Shenzhen, China, manufacturing facilities, while Emerald gains a strong Midwest presence," said Mario Sciberra, president and CEO, SLI.

"Joining Emerald expands our access to new markets and provides investment opportunities for us to build on our capabilities in order to stay ahead of the demands of our growing customer base," said Jay Cadler, president, Veris.

Day-to-day operations are expected to remain unchanged at both SLI and Veris, which will continue to operate under their existing brand names under the Emerald umbrella, Giglio said.

Emerald EMS was formed in July 2020 through the acquisitions of Data Ed and Bestronics by New Water Capital, a Chicago-based private equity firm. (MB)

## Syrma Technology, SGS Teknics Merge

**SAN JOSE** – Syrma Technology in November merged with SGS Teknics in a cash and stock deal of Indian EMS companies.

Syrma SGS Technologies will have a combined revenue of more than Rs 10 billion (\$134 million). Some 55% of revenues are from exports to the US and Europe.

**MKS Instruments** has received an order for multiple ESI Geode HDI laser drills in Taiwan.

**Nano Dimension** announced an additional 10 customers owning one or more older DragonFly Pro machines have upgraded to the next-generation DragonFly LDM machines.

SiC technologies are gaining the confidence of many customers and are penetrating various applications, especially electric vehicles, a new report claims.

**University of Southampton's Optoelectronics Research Centre** demonstrated an all-silicon optical modulator at 100Gb/s and beyond, without the use of digital signal processing.

**Ventec** has passed the ISO 9001:2015 audit for its Quality Management System at its facility in Fullerton, CA.

**Zuken** and **Electro Magnetic Applications** have entered a partnership to improve the accuracy of cable harness simulation models for complex electrical subsystems in aircraft and vehicles.

### CA People

Benetel named **Alan Hynes** director of engineering.

Creative Electron named **Jeff Darby** vice president of business development.



Enics appointed **Kristiina Leppänen** chief financial officer. Prior to joining Enics, Leppänen was CFO for Cavotec, among other executive positions.



Nordson Test & Inspection named **Dennis Rutherford** general manager, rest of Asia. He joined Nordson in 2016 after 15 years in high level sales positions with electronics inspection OEMs.



**Fred Dimock** recently started Fred C Dimock Global Services, focusing on thermal processes and profiling. He spent the previous 20 years as manager, process technology at BTU.



Yamaha appointed **Nick Iso-mura** division manager of the Intelligent Machinery (SMT Equipment and Robotics) Division. He has more than 20 years' experience in SMT equipment sales, and previously was group manager of Europe, Southeast Asia and Americas SMT sales for Yamaha in Japan.



Zestron named **James Mueller** Western regional sales manager. He has over two decades of professional sales management success, 12 years of which has been centered on achieving sales growth within the precision and critical cleaning marketplaces.

## CA Briefs

**Absolute EMS** installed a **Hanwha** HM520 SMT line.

**AIM Solder** opened a 12,000 sq. ft. ISO 9001-certified solder manufacturing facility in Malaysia.

**Amazon** has laid off dozens of R&D and manufacturing staff from its delivery drone project, Amazon Prime Air, and will outsource production.

**Apple** has reportedly started sending foldable iPhones to **Foxconn** for testing, with a possible release in September 2022.

**Apple's** plans to move the production of devices away from China received a major upswing, with several partners entering India through the government's Production-Linked Scheme (PLI).

**SMIC** and **China Electronics Technology Group** are among more than 30 companies blacklisted by the Trump administration for their suspected ties to the Chinese military. CETG is the parent of **TPV Technology** and **Shenzhen Kaifa**, two of the largest ODM/EMS companies in the world.

**Chase Corp.** finalized the acquisition of **ABchimie**, a developer of coatings for electronics, in an all-cash deal.

**Cogiscan** announced a strategic partnership with **Mycronic** to provide machine connectivity for Industry 4.0 applications.

**Creative Electron** has been awarded a patent for AI-powered programming of x-ray inspection systems.

**Datest** announced a new technical partnership with **Aster Technologies**.

**Ease** announced the availability of a complimentary new ebook, *The Ultimate Guide to Layered Process Audits*, which details layered process audits and offers advice, checklists and tips and tricks. ([https://go.ease.io/Ultimate-Guide-to-LPAs\\_LP.html](https://go.ease.io/Ultimate-Guide-to-LPAs_LP.html))

**Eolane** acquired a **Kurtz Ers** Versaflo 4/55 selective soldering oven for its Valence Romans Agglo site.

**Foxconn** is not expected to receive tax credits from Wisconsin in the next three years, according to the state Department

The combined company aims for 20% year-over-year growth.

The companies did not disclose any financial terms of the deal.

Syrma SGS Technologies will have eight manufacturing facilities in India and three design centers, including in Chennai and Gurgaon, India, and Stuttgart, Germany. Currently, Syrma and SGS each have four factories in India.

Syrma designs and manufactures RFID technology, power electronics, and turn-key manufacturing services and custom magnetics, and delivers IoT products for the automotive, computing, industrial, medical, power, and telecom companies. Medical and defense electronics are surging, the firm says. (CD)

of Administration.

**Foxconn** said a facility in Mexico has returned to normal following a ransomware attack in December. It also confirmed it has placed a bid to take over a stake in foundry **Silterra**.

**Indium** and **Valuetronics** have formed a strategic partnership to serve customers in the Americas with their cored wire, rework fluxes, and bar solder products.

**Intellitronix** acquired a **SpeedPrint** 700 series screen printer and **Europlacer** iineo+ pick-and-place system, and **Universal Instrument** model 5362i conveyors.

**Intervala** is reportedly considering a move in Pittsburgh that would increase its footprint from 136,500 sq. ft. to about 220,000 sq. ft.

**KIC** appointed **Rocka Specialty Solutions** manufacturers' representative throughout Mexico.

**Mentor** will now be known as **Siemens EDA**. The company will continue to operate as part of **Siemens Digital Industries Software**.

Fresh off its acquisition of **Tabtronics** in November, **Mirac** announced plans to will build an 11,800 sq. ft. EMS plant in Manchester, OH.

**Mountain Electronics** acquired **ALJ Electronics/ALJCO**.

**MRSI** and **Palomar Technologies** have reached an agreement that settles all litigation currently pending between the companies.

**NexLogic Technologies** added a 3,000 sq. ft. Class 10,000 clean room to its EMS operations in San Jose.

**Nordson Dage** named **Murray Percival** representative of its Assure series of x-ray component counters in the Midwest US.

**Northrop Grumman** awarded **Kitron** a three-year, NOK 20 million (\$2.2 million) contract to update a F-35 test program set and provide a repair capability.

**NovaCentrix** appointed **Torenko & Associates** rep in Texas, Oklahoma, Louisiana, Arkansas and the interior of Mexico.

**PDF Solutions** has entered into a definitive agreement to acquire **Cimetrix** for a \$35 million cash payment, net of cash, and subject to other closing adjustments.

**Pegatron's** board has approved an initial investment of \$150 million for building manufacturing facilities in India.

**Qualcomm** received a license from the US government to sell 4G mobile phone chips to **Huawei**, an exemption to US trade restrictions imposed amid rising tensions with China.

**Saki** opened the Saki Virtual Showroom, a digital reproduction of the Solution Center housed in its Tokyo headquarters.

**SEMI** submitted comments to the US Department of Commerce urging caution and the adoption of regulatory best practices and microelectronics industry recommendations to ensure its identification of foundational technologies does not restrain US innovation and exports without furthering essential US national security interests.

**South-Tek Systems** appointed Torenko & Associates manufacturers' rep in Mexico.

**TT Electronics** has completed the acquisition of **Torotel**, a manufacturer of power and electromagnetic assemblies and components for the aerospace and defense markets.

**TT Electronics** opened an electronics manufacturing facility in Kuantan, Malaysia.

**Universal Scientific Industrial** in December completed the acquisition of **Asteelflash** through the acquisition of its parent company, **Financière**. USI also broke ground on a 65,000 sq. m. facility in Haiphong City, Vietnam, with a planned investment of \$200 million for phase one.

**Vantage Specialty Chemicals** named **Creyr Innovation** manufacturers' representative for its surface treatment technologies.



**OUT OF STORAGE**

Trends in the US electronics equipment market (shipments only)	% CHANGE			
	AUG.	SEP.	OCT.	YTD%
Computers and electronics products	0.5	1.6	2.2	3.5
Computers	-0.7	4.3	1.7	-8.5
Storage devices	-1.3	-5.2	17.5	33.5
Other peripheral equipment	3.0	-7.9	2.1	9.5
Nondefense communications equipment	1.7	2.8	10.6	11.3
Defense communications equipment	6.2	-5.1	-0.4	5.9
A/V equipment	-3.0	4.0	1.6	-5.3
Components <sup>1</sup>	0.7	0.3	0.9	10.0
Nondefense search and navigation equipment	-0.8	0.0	2.6	-5.7
Defense search and navigation equipment	-3.2	2.9	0.8	2.5
Medical, measurement and control	2.8	1.1	1.7	-1.1

<sup>1</sup>Revised. <sup>2</sup>Preliminary. <sup>3</sup>Includes semiconductors. Seasonally adjusted. Source: U.S. Department of Commerce Census Bureau, Dec. 4, 2020

**US MANUFACTURING INDICES**

	JUL.	AUG.	SEP.	OCT.	NOV.
PMI	54.2	56.0	55.4	59.3	57.5
New orders	61.5	67.6	60.2	67.9	65.1
Production	62.1	63.3	61.0	63.0	60.8
Inventories	47.0	44.4	47.1	51.9	51.2
Customer inventories	41.6	38.1	37.9	36.7	36.3
Backlogs	51.8	54.6	55.2	55.7	56.9

Source: Institute for Supply Management, Dec. 1, 2020

**KEY COMPONENTS**

	JUN.	JUL.	AUG.	SEP.	OCT.
Semiconductor equipment billings <sup>1</sup>	14.4%	26.7%	32.5%	40% <sup>r</sup>	26.9% <sup>p</sup>
Semiconductors <sup>2</sup>	4.9%	4.23%	4.94%	5.79% <sup>r</sup>	5.95% <sup>p</sup>
PCBs <sup>3</sup> (North America)	1.12	1.00	0.94	0.93	0.97
Computers/electronic products <sup>4</sup>	5.44	5.28	5.22	5.15 <sup>r</sup>	5.00 <sup>p</sup>

Sources: <sup>1</sup>SEMI, <sup>2</sup>SIA (3-month moving average growth), <sup>3</sup>IPC, <sup>4</sup>Census Bureau, <sup>p</sup>preliminary, <sup>r</sup>revised

## Hot Takes

- The global wearables market grew 35.1% year-over-year during the third quarter, with total shipments reaching 125 million units. (IDC)
- Flexible hybrid electronics is expected to be an approximately \$3 billion market by 2030. (IDTechEx)
- Desktop and notebook PC shipments are expected to grow 18% year-over-year in the fourth quarter, followed by 1.4% growth in 2021. (IDC)
- Smartphone shipments are forecast to grow 2.4% year-over-year in the fourth quarter, followed by 4.4% year-over-year growth in 2021. (IDC)
- The market for high bandwidth memory is projected to grow 49% in wafers, including DRAM and logic layers, from 2020 to 2024. (TechSearch International)
- Third-quarter world electronic equipment shipment growth

was down an estimated 1.4% compared to the same quarter in 2019. (SEMI)

- India has 268 mobile and accessories factories, more than twice the number often quoted by many senior leaders in the government. (India Cellular & Electronics Association)
- Fiberglass yarn and fiberglass cloth materials for PCBs saw a 20% increase in quotes, reflecting strong demand for 4.5G and 5G applications. (TPCA)
- India has the potential to become a \$100-billion global manufacturing and export hub for printed circuit board assembly by 2025-26. (ICEA)
- The worldwide telecom EMS market was worth \$155.7 billion in 2019 and is projected to grow at a CAGR of 7% from 2020 through 2027. (Statista)
- Worldwide server shipments declined 0.2% year-over-year to nearly 3.1 million units during the third quarter. (IDC)

# Revealed: Technology Really Works!

Now, just how many people can we move off the floor?

**THIS PAST YEAR** was most unusual, distracting and challenging, and many of those distractions and challenges appear they will remain with us well into the first half of the year. As industry begins to focus on post-pandemic planning, however, much has been learned over the past year that can and is being applied to planning for the future.

Possibly the most significant thing learned is technology can – and does – work! A generation of manufacturing and technology leaders knew little of platforms such as Zoom, WebEx, etc. Through baptism by fire, we have become believers in virtual interaction, its effectiveness and value. Equally significant is the realization that for many business functions, including those in manufacturing, remote working – aka working from home – works and offers much more flexibility than the traditional structured workplace.

Manufacturers have by necessity reconfigured shop floors to accommodate social distancing, cleaning protocols, and all that has gone with the Covid pandemic. Adding space between production lines can accommodate social distancing. But while effective, it has proven costly. Splitting shifts is another tactic. Employees may be willing today to change schedules to keep a job; however, it is not ideal in the long term. Meanwhile, in the office environment social distancing is accomplished via interactive technology. Further, many claim the efficiency and flexibility from employees working remotely and communicating virtually has been significantly better than they imagined. The office environment success and flexibility from harnessing virtual communication technology has not gone unnoticed by the manufacturing manager.

Over the past couple months, I have had many conversations with colleagues in our industry and other manufacturing fields about how to apply the lessons learned as we attempt to return to “normal,” or as a “new normal” emerges. Much of the conversation has focused not on how to reduce headcount and therefore costs, but instead on how to reduce the “traffic” and “parking” on the shop floor via harnessing virtual interaction technology to increase efficiency and reduce process time. One of the observations I keep hearing is that with fewer people congregating on the shop floor at the same time, product seems to move faster through work cells and from process to process.

Further discussion has centered on rethinking manufacturing processes: separating the “hard” tasks of manufacturing, which require an onsite human operating a piece of equipment and touching product, from the “soft” tasks, which are often monitoring

processes, verifying and validating product, and generating documentation. On a traditional shop floor these tasks take place side-by-side by different employees with different skill sets.

The thought is if those responsible for the “soft” tasks do them remotely, it will reduce shop-floor traffic. Less traffic means fewer distractions and greater flexibility, and there is less opportunity a “parking lot” will develop as people chit-chat, reducing throughput and efficiency. Wherever traffic is, you frequently end up with an area filled with inert employees and products.

Performing those “soft” tasks virtually, however, requires more than just a Zoom account. And that’s where creative process engineers are working to harness sensors, test and measurement equipment and basic automation with the anticipation that a reasonable happy medium can be achieved.

For years it has been possible to monitor equipment such as drill machines remotely. Likewise, computer-driven CMM equipment can be operated offsite. Ditto for verification documentation, such as a FAI. Employees who handle these tasks from home or in a cubicle off the shop floor will continue to be the norm. But much of the other tasks in manufacturing are more challenging.

High-volume manufacturing offers some opportunity to lean out the shop-floor traffic as well. More than a few process engineers are looking at how to reduce the number of people in a work cell by locating one or a few off the shop floor, while they still monitor the process or line. Staggering work-cell schedules, not by multiples of shifts but by minutes, can also separate setup from operators from test and verification, collectively reducing shop-floor traffic.

High-mix, low-volume manufacturing environments have the greatest challenge to deploying virtual interactive technology to reduce shop-floor traffic. And more opportunities exist. Creating data and tooling packages can be done remotely, as can much of the end verification and validation data creation. Staging work through a network of onsite and offsite staff – implemented thoughtfully – can increase flexibility and throughput and reduce traffic.

Finally, for those who thought Industry 4.0 was interesting, much of the past year has provided validation that the technologies are in place and work well. Many colleagues are moving feverishly to take advantage of the available tools now that employees and managers – many who have never imagined utilizing such technology – are experiencing their power and convenience on a personal and professional level. □

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# PCB Costs Are Going Up. Here's What to Do

How to respond to supplier price increases.

**DEMAND FOR PRINTED** circuit boards is going up. But so are production costs.

Raw PCB material pricing has jumped about 40% since June, with the exact increase dependent on material type. This price increase was inevitable and is, in fact, overdue.

During the early months of the Covid crisis, most PCB suppliers were hesitant to pass on their already-increasing material costs. But as China has rebounded faster from the Covid slowdown than the US and Europe, demand for production has escalated. PCB vendors are now more willing to pass higher material costs onto their customers. And the price increases are by no means over.

The price of gold salt and the precious metals used for metallic finishes of the PCB are on the rise as well. While the cost for the application of ENIG finish is the same regardless of the layer count, the percentage of price increase is inversely proportional to the PCB layer count, meaning a double-sided board will see a higher percentage price increase than a 10-layer PCB.

To add insult to injury, American buying power has fallen almost 6% since January as the value of the US dollar has declined against the Chinese RMB.

When it comes to PCB costs, we are in a perfect storm. The price of raw materials, gold and precious metals is on the rise, along with production demand. At the same time, the dollar is weaker. That means higher prices for US PCB buyers.

Here's the bottom line: You can expect over the next few months to see an additional price increase of eight to 10% for doubled-sided boards, depending on technology and quantity requirements. Multilayer PCBs are expected to rise five to eight percent.

However, PCB buyers may be able to fend off some of those increases by buying smarter and more strategically.

Putting PCBs in an array for ease of assembly makes sense, but I can't tell you how many times I have seen wasted circuit board real estate when it comes to panelization design. More square inches mean a more expensive board. Buyers need to push back on their production and engineering departments by asking questions such as, "Does this array really need to have rails this wide?" or "Can we score instead of route?"

Does every board you buy require a gold finish? Yes, ENIG is lead-free; it has great coplanarity features and a long shelf life. But does every assembly on your production floor really need all those costly benefits?

Don't allow a boilerplate company standard to unnecessarily inflate costs. Be selective. Use a pre-

mium finish only when truly necessary. From a pricing standpoint, there is more than one "metallic" way to assemble a PCB.

Do you order the same part number and quantity monthly? If so, review those repetitive purchase orders and have a heart-to-heart talk with your customer. Your PCB vendor would prefer to run a larger quantity when and wherever possible. Ordering a larger quarterly quantity of PCBs and accepting them in monthly deliveries is a great way to get a discount.

Also, start leveraging your PCB spend with your vendors. Have them visit (for now, you may have to conduct a virtual meeting) and ask what else you can do to reduce costs. At the same time, remind them of your annual spend and length of business relationship. Have a serious discussion about performance issues. If your supplier intends to raise prices, demand those increased costs come with enhanced service.

Keep in mind, though, that the best way to keep pricing in check is to always pay your PCB vendors on time. Timely payment will dictate the strength of your relationships with suppliers. Habitually paying beyond the agreed-upon terms can harm your business relationship in a variety of ways, including lowering your level of customer service, giving you less favorable payment terms in the future, and increasing your pricing.

The more you string out payments to vendors, the less likely those vendors will be to jump through hoops – bending to price pressures, responding quickly when an expedite is needed, or acting to resolve a quality problem – when you need them to.

It always surprises me when a PCB buyer gets upset when I inquire about late payment. If one of *my* PCB shipments were late, that same customer would demand to know its whereabouts. Just as you as a buyer demand prompt delivery of product, you should also be a consistently prompt payer.

A customer who doesn't pay is not really a customer. That applies to your company as well. Paying your PCB vendors on time increases their confidence in you as a business partner, and you will reap the benefits of that confidence over and over again. It's a big part of fostering a good relationship with your vendors, and it makes it much easier to get price concessions, even during tough times. □

**GREG PAPANDREW** has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying ([boardbuying.com](http://boardbuying.com)); [greg@boardbuying.com](mailto:greg@boardbuying.com).





# Estimating the PCB Design Cycle with Limited Information (and Then Making It Happen)

What Charlie Brown can teach us about board design.

**NOT ALL BOARDS** are alike. In fact, no two are exactly the same. That's kind of the point. We always do something that hasn't been done before, or we wouldn't be doing it. The best we can say is many boards share similarities. Just the same, someone in every organization wants to know when the one-off job will be completed.

Often, there is a predetermined schedule in which someone who has never drawn a trace decides when the PCB layout needs to be finished. Such a schedule is usually the result of market forces. It could be back-to-school, CES, or even (especially) a rocket launch date that drives the deadline. Still, it's not unusual for stakeholders to ask your opinion about the estimated tape-out date.

**Life in a service bureau or as an outside contractor.** Service bureaus live or die by the accuracy of their bids. If their bid is too many hours, the customer will shop around. If the bid is too few, the designers end up eating that cost with overtime or, worse, missing the date and facing customer dissatisfaction. The one thing that saves them is that the service bureau is working from a baseline plan that does not usually include co-development.

A statement of work including a few milestones will put the customer in lockstep with the vendor. A definition of success that includes the delivery date will also have a few intermediate milestones, including schematic capture, mechanical lockdown, placement approval, and so on (**FIGURE 1**). The hourly amount the service bureau charges is more than it pays the designer. Even in a one-person shop, overhead comes first, and the owner-operator gets paid out of the

remaining funds.

I once owned one of those operations. The worst possible outcome was that I would have to subcontract work out. In that case, it was more like being a broker than a designer. If my plate was full, I would no-bid a proposal or quote a higher-than-normal rate. Getting a lot of business in a short amount of time is a mixed blessing.

The mid-design updates trigger an ECO charge that can be quite substantial. The incentive is to quote an aggressive but doable schedule. Once underway, the plan is to tack on fees if the design cycle is interrupted by improvements. Some customers appreciate they are spending money to pull in the launch date. You want repeat customers, so be careful not to overextend yourself.

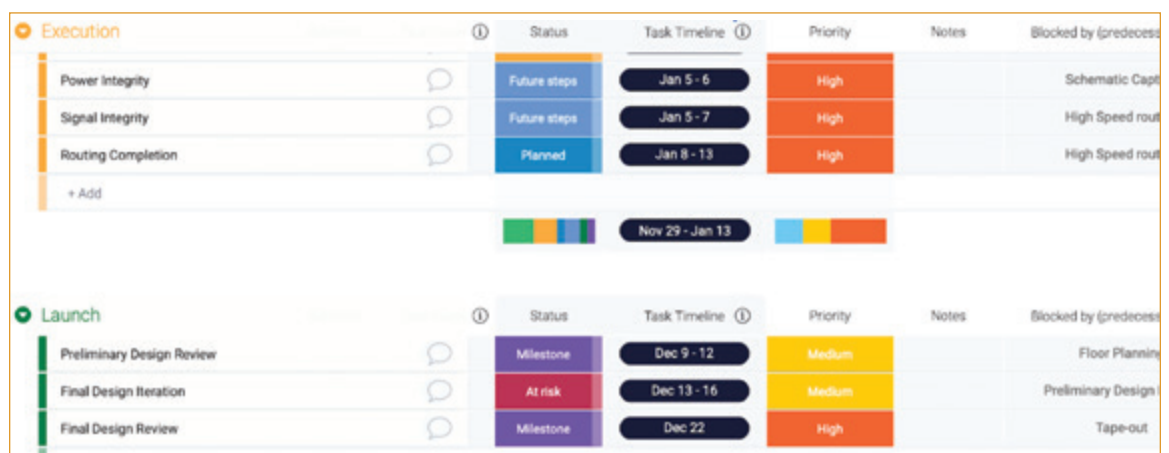
One of the main metrics in the design cycle is the number of pins. Back in the day, it was a dollar per pin. Some pins matter more than others. A length-matched pin counts as three pins because you take more time to dial it in with the rest of the bus. RF pins are two-for-one because of the expected back-and-forth with the analog engineer. As you build your portfolio, take note of the actual vs. estimated duration so you can fine-tune your scheduling quotes.

New component footprints, whether built in the CAD tool or imported from a vendor or library service, take time. You must take them into account for the estimate. Of course, not all components are created equal. Higher pin-count and fine-pitch devices are another weighting factor in the pin-count. Board density is in play, too. Test fixtures will usually go more quickly than production form-factors. The stack-up

## JOHN BURKHERT

JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design.

He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.



**FIGURE 1.** A scheduling tool helps keep the progress front and center.

technology will be a factor of all the above parameters.

It seems flippant in hindsight, but I used to ask how many engineers are on the project. The old saying goes, if you want three opinions, ask two engineers. The various subject matter experts believe their function to be the most important. Getting mixed messages based on different priorities puts us on the throne of King Solomon. There should always be a lead engineer who makes the final decisions. When conflicting instructions come to light, loop in that leader.

**Captive designers: No plan survives contact ...** Most of us are captive designers. The rule here is everything changes except the tape-out date. Some of you may remember the *Peanuts* cartoon strip in which Charlie Brown would attempt to kick the football. Inevitably, his foil Lucy would pull the ball away, leaving poor Charlie Brown on his back. It was a recurring theme: He never once got a foot on the ball.

That's a metaphor for board design if you're expecting to go from start to finish without a course-correction (**FIGURE 2**). After Google bought Nest, one of the Nest PCB designers wanted to join the Chrome team. I interviewed the guy and recommended approval of his transfer. For one thing, he knew how to code in Pearl and other tools for automating the drudgery.

The program manager asked him for a time estimate for a complex smartphone breakout board. He was savvy enough to quote three months based on the usual co-development with a large team. He was being too real, and the PM wasn't having it. Not knowing his projection when she asked for my opinion, I said two months, best case, but it would not surprise me if it went four.

That was also "too real," so it became one of those team efforts. Even with partitioning and sending the design out to

a service bureau every night, it took just under three months. That included Saturdays and short shifts on Sundays to keep the outside vendors on track. In the end, schematic and outline revisions were out of our control. It's difficult enough when you have not done something before. When a brand-new team does something for the first time, count on half-again more for expected churn.

The most optimistic people in the business seem to go into program management. They may put the PCB designer nominally in charge of driving the schedule, yet we have virtually no authority over the team that ultimately determines the outcome. It is easy to get ahead of yourself when working alone at your desk.

Adding to that uncertainty, some people are unconcerned with the schedule in the first place. Perfection, or simply better, is the enemy of good enough. Digital circuits either work or they don't. It's the analog engineers (I am one) who chase that last bit of performance. Prototypes will always require some improvements, and you won't know what those improvements are until you have that first round of hardware.

**When it comes to schedule progress, sharing is caring.** Simply sharing the data at the end of each day may not be enough. Asking one question related to the work may be sufficient to get the other people to look at the design. You're making design decisions all day long.

A real-life example goes like this: The vias under the SOC are too closely spaced to allow placement of the capacitors. We have to find one mil somewhere. Should we reduce the via size, the pad size or the allowable pad-to-via airgap?

If you make that decision yourself, then you own the problem should one arise. Let's say you take the third choice, reducing the airgap from four mils to three. Then, two days after tape-out, the vendor calls and says there is risk of exposed metal because of solder mask expansion. It's a little late to be thinking about the padstack options.

Getting to the end date with a viable board takes strong communication. The more urgent the schedule, the more you must be risk-averse. Respinning that critical-path layout is a much bigger schedule hit than taking the time to get buy-in on the deviation. No one likes surprises. Take a cue from Charlie Brown to avoid those traps. □



**FIGURE 2.** A Gantt chart helps visualize scheduling dependencies.

# Today's Best Technologies are the Roadmap to an Even Better Future

From autos to airplanes, change is in the air.

2020 HAS BEEN an unusual and challenging year, although many of us can be thankful for the resilience of high-tech industries. Indeed, activity has surged in some sectors, and generally the outlook is relatively buoyant.

In my other role as president of the EIPC (European Institute for the PCB Community), I moderated the Institute's Technical Snapshot webinar last November, at which Dr. Shih-Kao Chiang of Prismark described how various sectors have fared. While 5G infrastructure rollouts slowed and handset shipments fell about 10%, the PC market has been buoyed by the increase in work-from-home, and certain consumer markets such as wearables and smart appliances have also done well. Overall, he noted a surprising robustness across the electronics, semiconductor and substrate markets.

The automotive sector has been among the hardest hit, along with conventional commercial aerospace. Rebuilding after the damage to sales caused by the pandemic is just one of the challenges facing vehicle manufacturers right now. They are also contending with the push toward higher levels of driving automation, mandatory smart systems such as autonomous emergency braking, and real-time V2X capabilities, which are expensive to develop. At the same time, governments are signaling their intentions to accelerate electrification, which will require all manufacturers to move their entire product ranges to hybrid-electric or pure battery-EV platforms. The UK government has brought its intended start date forward to 2030. There is no doubt about the urgency, although I am sure at least hybrid-EVs will prove a steppingstone to the kinds of vehicles we use in the future.

Technical progress often happens this way. Consider where we are now with low-energy lighting, for example. Filament bulbs were the dominant technology lighting homes and had changed little in a hundred years. As we saw the imperative to reduce the energy consumed by lighting, we first adopted compact fluorescent lamps (CFLs). Disliked for many reasons, they could be slow to reach full brightness. The lumen output degraded badly over time, and they presented a hazardous waste problem at end of life. Clearly, the world needed to step beyond these and realize a better solution.

Today's solid-state domestic lighting is enabled by innovations in LED fabrication, of course, and by the enhanced thermal performance of insulated metal substrate (IMS) technology, developed within the PCB industry. We are now rewarded with even better lighting, not only more energy-efficient than those early CFLs but with improved reliability and more options than ever to create various lighting effects to suit our moods and activities.

Hybrid-EVs and battery-electric vehicles as we know them today have some notable drawbacks. Carrying both internal combustion and electric power systems makes today's hybrids heavier and more expensive than is ideal. Also, problems are associated with sourcing rare materials such as lithium, which is an issue because Li-ion is currently the most suitable battery technology. Natural lithium deposits are dwindling, although mining remains more cost-effective than reclaiming the material from scrap batteries. Nevertheless, automotive electrification has helped create a sizeable market for Li-ion battery recycling that should reach \$17 billion by 2027.

I'm optimistic the coming transition to hybrids and EVs will be just the beginning of our journey toward even better vehicles. They will be enabled by a variety of technologies, some of which are already known, while others remain undiscovered. Prospects are great for PCB stators, for example. These not only save the weight and losses of traditional laminated-iron cores but also allow direct integration of circuitry for important features such as sensing, condition monitoring, and IoT connectivity.

Insofar as energy for EVs is concerned, the hydrogen fuel cell could help relieve demand for lithium. Easy and fast to recharge, it could alleviate range anxiety, while at the same time permitting a significant reduction in battery size. On the other hand, this, too, could be a steppingstone toward another solution that will be more efficient and safer, easier to live with, and ready to offer more rewarding experiences than any we can imagine today.

In addition to road vehicles, shipping and aviation are elements of the transportation mix heavily dependent on combustion engines. The shipping industry is under pressure to move from traditional heavy fuel oil, with or without the use of exhaust scrubbing to remove sulfur-based compounds, in favor of cleaner fossil fuels or, ultimately, electrification. Leading logistics businesses and technology developers are teaming up to create solutions such as high-capacity marine batteries, high-power low-voltage diesel-electric hybrid drives, and hydrogen fuel-cell generators. Ferries, which cover short distances along fixed routes, could be the first step toward full electrification of long-distance shipping.

In the mission to decarbonize aviation, leading aircraft manufacturers are taking their first steps with

*continued on pg. 38*

## ALUN MORGAN

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# PCEA 2020: Small Rearview Mirror, Big Windshield

A successful first year promises even bigger things to come.

**IN THIS MONTH'S** forward-driving column, I glance back at PCEA's year in "rearview," which included an energetic jump-start, some challenging air filter retrofitting, some remote diagnostics, and a final refueling at a successful virtual chapter meeting. Next, I hit cruise control and rely on PCEA chairman Stephen Chavez, who focuses on what lies ahead between the vanishing points of highways 2020 and 2021. As always, I'll also point out some interesting events for you to consider attending.

## PCEA Updates

The past year can be viewed as one of the many good metaphors based on cars and driving, pointing out the differences in size between a rearview mirror and a windshield. You only need to glance in a rearview mirror when backing up or trying to see what may be overtaking you. But if you're driving forward, your main focus should be on the large, clear windshield to see what's coming.

2020 was a great year for the PCEA. It had to be because it's the only one we've had. A group of designers, engineers and PCB industry professionals found themselves looking for a new role after the dissolution of the IPC Designers Council in November 2019. The group was not ready to hang up their passion for highlighting and representing PCB designers. Additionally, they acknowledged a more intimate organizational structure was needed to better cultivate and grow relationships with all vital stakeholders to understand and communicate each other's requirements during the vital phases of design, manufacturing, procurement and test.

In January, meetings were called, and the group came together to prepare the vision and restart as a grassroots organization with a mission to collaborate, educate and inspire the electronics industry to create better printed circuits. However, the group soon found themselves masked and quarantined, as did virtually all the electronics industry. Meeting over the past months, the PCEA was forged and incorporated as a nonprofit. Stephen Chavez established this monthly column a few years ago, prior to the launch of the PCEA. He delegated it to me after he was named chairman of the PCEA.

In less than a year, the foundation of the PCEA has been laid. The organization held its grand opening event online and counts over 1,000 members among many local chapters itching to meet again. More recently, the San Diego and Phoenix chapters hosted a successful virtual chapter meeting attended by over 50

industry professionals from all over, including Canada.

## October PCEA Chapter Meeting

Local chapter presidents Luke Hausherr (San Diego chapter) and Randy Kumagai (Phoenix chapter) kicked off the meeting on Oct. 28 with greetings and an introduction to PCEA chairman Stephen Chavez. Steph gave an overview and called on people to spread the word that the PCEA was ready to fulfill its mission of leadership, membership and continually growing industry sponsorship. Recent sponsor Insulectro delivered a technical session on design innovation related to PCB materials, given by VP of technology Chris Hunrath and technical director of design education Mike Creeden, who is also PCEA vice chairman (**FIGURES 1 and 2**).

Topics covered included:

- Design innovation
- Hybrid stackup models
- Material properties and considerations
- Effects of loss tangent
- Mixing laminates
- Embedded capacitance
- Advanced HDI structures.

After the presentation, the chapters hosted a raffle with some outstanding prizes. Luke selected the winners (**FIGURE 3**). The grand prize was a seat of PCB Library Expert, thoughtfully provided by PCB Libraries.

## Message from the Chairman

*by Stephen Chavez, MIT, CID+*

What a year! We will never forget 2020. With everything happening in the world today, it amazes me how many have adapted to the virtual world, didn't break stride in meeting today's challenges, and continue to be successful. Our industry's evolution waits for no one, and many have stepped up to the challenge and conquered it. When I think about how 2020 unfolded for the PCEA, we have far exceeded our initial expectations and goals for the year.

From our grand opening on Jul. 14, our membership continues to see strong growth month after month. We are not only growing within the US, but we also have internal growth. Our local and regional PCEA chapters have seen momentum and success. We now have 10 active domestic and international chapters, with eight chapters in their infancy and many others coming soon.

What excites me most about the chapter activities is how each of the chapters is collaborating and

**KELLY DACK, CIT, CID+,** is the communication officer for the Printed Circuit Engineering Association (PCEA). Read past columns or contact Dack; kelly.dack.pcea@gmail.com.



functioning as one collective to better the industry. Even for those of us who have been around for many years and actively involved within the industry, this chapter-to-chapter communication and activity has not been seen before. We truly have collaboration, inspiration and education taking place, especially within our chapters, from one virtual event to another. There is an exciting buzz within the industry about the PCEA.

If these activities aren't enough to make you want to join the collective, then check out our industry affiliations and collaboration, both domestic and international, which is seeing the same type of growth. Our sponsorships also continue to make strides as we continue to get positive feedback and buy-in to what the PCEA is all about. And there are a lot of webinars offered for free, so take advantage of them when you can.

Our future looks extremely bright. For 2021, look for more activities, collaboration and synergy among all PCEA chapters. You'll also see growth with our industry affiliates and sponsors to solidify our mission to collaborate, inspire and educate. The year will be even better.

If you have not yet joined the collective, I highly encourage you to do so by visiting our website at [pce-a.org](http://pce-a.org) and becoming a member.

I continue to wish everyone and their families health and safety. I wish you all much success in 2021.

### Next Month

As our leader, Steph is doing his job to set the vision, and the PCEA executive staff will be meeting again soon. We will take feedback from the local chapters and work with our sponsors to make concrete plans for PCEA events to help the industry connect and become more educated. I will report on the materialization of these evolving plans in our first column of 2021, so stay tuned.

### Upcoming Events

- Mar. 8-12: IPC Apex Expo (Online)
- Apr. 13-15: DesignCon (San Jose, CA)
- May 10-12: PCB East (Marlborough, MA)
- May 11-13: IPC High-Reliability Forum 2021 (Baltimore, MD)
- Jun. 7-10: Zuken Innovation World (Scottsdale, AZ)
- Aug. 31-Sept. 3: PCB West (Santa Clara, CA)
- Nov. 10: PCB Carolina (Raleigh, NC)

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at [kelly.dack.pcea@gmail.com](mailto:kelly.dack.pcea@gmail.com), and we will consider adding it to the list.

### Conclusion

It's sometimes a relief to look in your rearview mirror and clearly see what you've left behind. But through a dirty windshield, covered with Covid-19 and other challenges, it can be daunting to drive forward without vision. At the PCEA, we want to be the windshield wipers or the sponge and squeegee to help you wipe away your printed circuit engineering apprehensions. Our collective will help you see where your industry is going, inspire you to take the wheel, hit the gas, and enjoy the ride. Now is a great time to check us out at [pcea-a.org](http://pcea-a.org) and make a New Year's resolution to rideshare with us. We're in it for the long haul and have many experienced designated drivers.

See you next month or sooner! □



**FIGURE 1.** Mike Creeden.



**FIGURE 2.** Chris Hunrath.



**FIGURE 3.** Luke Hausherr.

# Cutting Your Losses Upfront in PCB Design

A methodology for selecting the right material and the right price point.

**WHEN I STARTED** writing this column a couple years ago, I wondered how much I'd have to say. An experienced media guy told me to watch my inbox for topics and questions that may be of general interest. That turned out to be excellent advice. Here's one such example.

“What is the best laminate for a loss budget of  $x$  dB for  $y$  inches? I was thinking in terms of Panasonic Megtron 6 or something like it.”

Megtron 6 is an excellent material, but it's not cheap and it's not the only horse in the race. My response was to focus on a loss and material-planning methodology rather than making a firm material recommendation.

**Why we care.** Everything that improves material performance – in particular, reductions in loss – comes at a price. Loss versus cost is a classic optimization problem. Designers want to pay just enough to meet loss requirements, but not more than they need to.

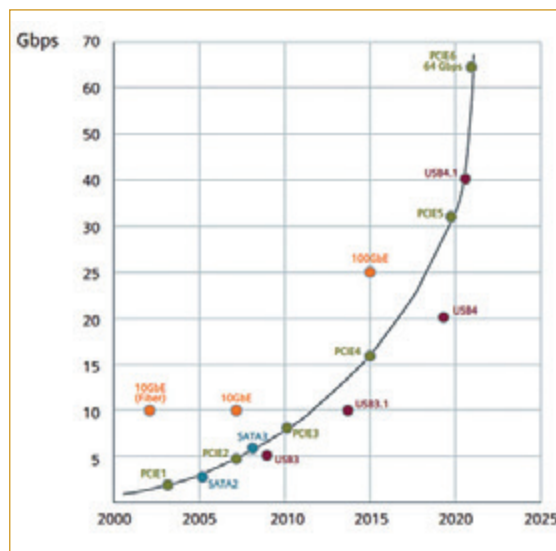
In the past, speeds were slow, layer counts were low, dielectric constants (aka Dk or Er) and loss tangents (aka dissipation factor, or Df) were high, design margins were wide, copper roughness didn't matter, and glass-weave styles didn't matter. We called dielectrics “FR-4,” and their properties didn't matter much.

As speeds increased in the 1990s and after, PCB fabricators acquired software tools for designing stackups and dialing-in target impedances. In the process, they acquired PCB laminate libraries, providing proposed stackups to their OEM customers, typically late in the design process, including material thicknesses, copper thickness, dielectric constant and trace widths often weeks or months after initial signal-integrity simulation and analysis should have taken place.

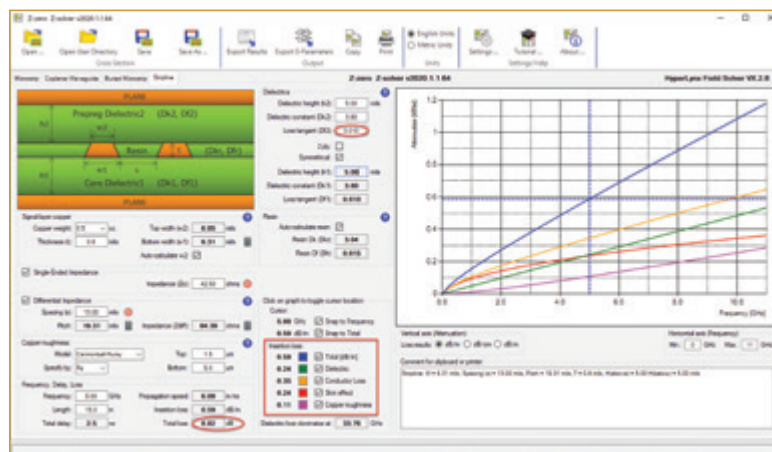
As speeds continued to increase, design margins continued to tighten and OEM engineers began tracking signals in millivolts (mV) and picoseconds (ps). **FIGURE 1** shows these trends starting in 2000. Note in particular the PCI Express trajectory. Critical factors for signal integrity now include not only impedance, but loss, copper roughness and glass-weave skew. Indeed, everything that happens in the process of physically building a PCB affects signal quality in a

negative way, and the details need to be accounted for across not just one PCB stackup, but across stackups from every PCB fabricator involved with a design.

**5dB interconnect loss at 5GHz.** Let's say we're targeting 5dB total interconnect loss at 5GHz for a 15" stripline run length using 0.5 oz. copper. We'll ignore vias for this example and just focus on the laminate. Experience says this may require a material that's indeed in the Meg6 range, but we don't want to spend more money than we have to, so we'll start with a loss



**FIGURE 1.** Interconnect speed increases in gigabits per second (Gbps) from 2000.



**FIGURE 2.** Our initial stripline configuration with  $Df=0.010$  and a total loss of 8.82dB. (Image from Z-zero's Z-solver software)

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tangent (dissipation factor, Df) of 0.010 and see where we're at for a starting point.

**FIGURE 2** shows the result, but some explanation is in order. The blue line represents total loss, which is the sum of all other sources of loss. The orange line is conductor (copper) loss, which is the sum of skin-effect loss (red) and copper roughness (magenta). The graph shows loss in dB per inch, resulting in a total interconnect loss of 8.82dB, a good bit above our target of 5.0dB.

The next place I look is the insertion loss box, which is expanded in **FIGURE 3**. The two biggest contributors to loss here are the skin effect loss and dielectric loss, both at 0.24dB/in. I know we can cut dielectric loss in half by cutting the Df value in half, so let's give that a try. Changing Df to 0.005 results in a dielectric loss of 0.12dB/in. and a total loss of just over 7.0dB – a significant improvement! Figure 3 also shows loss from copper roughness at 0.11dB/in. is very close to our new dielectric-loss contribution.

Figure 2 shows the core-side roughness for this hypothetical laminate has an Rz roughness of 5.0µm. This corresponds to what many call RTE, or reverse-treated foil. I happen to know that materials in the 0.005 Df range generally offer smoother copper either by default or as a loss-reduction option. Let's see what would happen with VLP2 or "very-low profile, 2µm" copper. **FIGURE 4** shows this change, along with the resulting total interconnect loss, which is now 5.92dB – much closer to our goal.

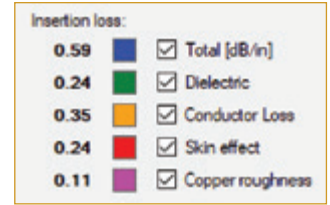
The total insertion loss is now 0.39dB/in. An easy next step toward achieving our 5dB goal is to create a routing rule that reduces the original 15" to 12". Let's make that change and see where we end up.

*Voila!* Total loss becomes 4.74dB. We now have a Df target for a laminate system, a copper-roughness selection, and a routing rule. That's a lot of progress early in the PCB design process. We can now begin looking for a material that aligns with these parameters.

Two good places to initiate that search are with your PCB fabricator(s) or from laminate-vendor data. Several materials that may be worth looking into are shown in **FIGURE 5**, based on their vendor-published Df numbers at 5GHz.

**Wrapping up.** If you can make material decisions like this early in the design process, you'll avoid prototype

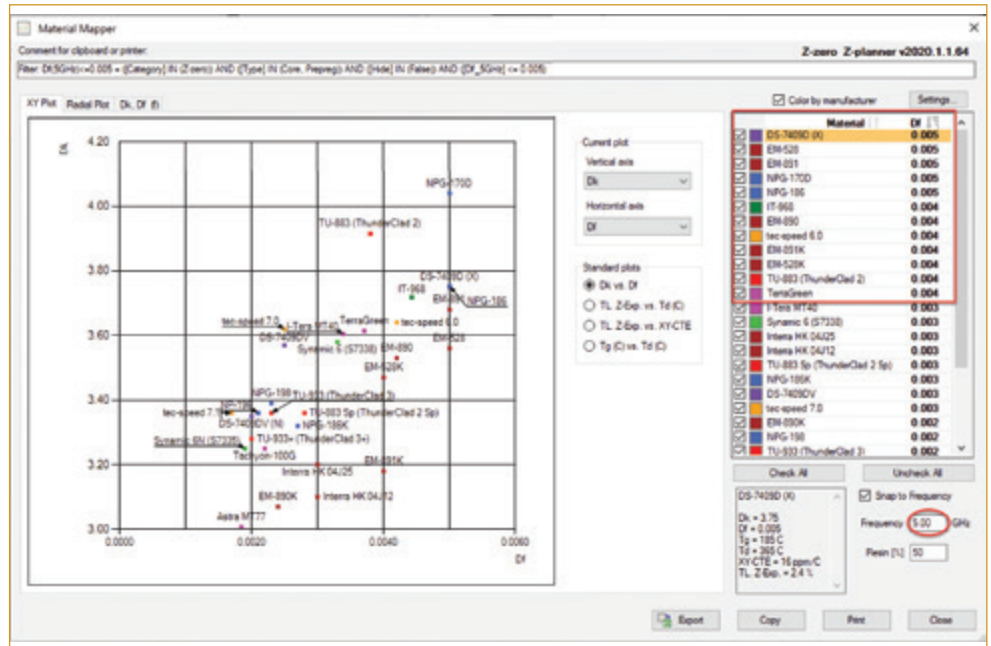
surprises down the road or paying more than you need to for laminate systems that are overkill for a design. Making these choices early also allows you to avoid initial laminate lead times that can delay prototypes or early production. Because of prepreg shelf-lives, fabricators carry only the laminates they know they can use within six months or less, following a just-in-time approach. As in many other aspects of life, planning means more options and fewer surprises. You can feed that expensive signal-integrity solution Dk and Df data from the actual laminate system you're planning to use. Moreover, it may allow you to hold to NPI (new product introduction) schedules more consistently, while at the same time relieving some of the pressure you put on PCB suppliers to make up for poor planning. Everyone wins! □



**FIGURE 3.** The insertion loss box, expanded from Figure 2. The two biggest contributors to loss here are the skin effect loss and dielectric loss, both at 0.24dB/in. (Image from Z-zero's Z-solver software)



**FIGURE 4.** The trapezoidal shape of innerlayer traces, shown in a strip-line cross-section, where w2 is narrower than w1. (Image from Z-zero's Z-solver software)



**FIGURE 5.** Materials to consider, based on their vendor-published Df numbers at 5GHz. (Image from Z-zero's Z-planner software)

# NEW DfX MODULE for IPC-2581 Slices Design-Manufacturing Time, Errors

The latest IPC-DPMX standard offers unique bidirectional data exchange between design houses and their manufacturing partners. **by HEMANT SHAH**

The authors of IPC-DPMX, previously known as IPC-2581, have come up with an innovative solution for addressing the needs of the industry for the latest version of the electronics data transfer standard. Developed by the industry, IPC-DPMX has many new enhancements. The just-released Revision C has been reviewed and unanimously approved by the PCB design, analysis and supply chain industry.

IPC-2581B introduced the concept of bidirectional data exchange between design houses and their manufacturing partners. It sought to eliminate the back-and-forth between partners at the very end of the design cycle for communicating and ensuring that critical net impedances were achievable. This communication was important earlier in the design cycle and impacted the layer stack-up, which is hard to change at the end, when design is complete and handed off. Although this innovation was unveiled almost seven years ago, it is still unmatched and unique within an open standard.

Fast forward to 2020. IPC-2581C brings yet another innovation driven by consortium members who saw one more thing that slows them down at the very end. When a design is handed off, the manufacturing partner often wants to check how efficiently the design can be built, including a look at the capability check, as well as any DfM errors within the design. Over 90% of finalized designs have DfM errors, some repeated in every design. There is then a back-and-forth between design and manufacturing to address the issues. Many times, manufacturers want something in writing in order to deviate from the very standard the designer wants the manufacturer to follow. This exchange and settlement can cost both companies time and effort. It's a lose-lose situation.

The result was that the consortium, with key contributions from Cisco, proposed a new function mode: a module for DfX sign-off between the designer and manufacturer that eliminates e-paper-based communications that are time-consuming and frustrating for both sides.

The DfX module within IPC-2581C enables OEMs and manufacturers to communicate in a bidirectional manner any DfX error and technical queries. The DfX module can be

the only functional module in an IPC-2581 file, or it can be included with the rest of the design data. Both fabricator and OEM can create databases of issues for root cause analysis and improvement. Over time, this enables designers and manufacturing partners to track responses to queries, collecting metrics over a period by class of design and by manufacturer/customer.

With IPC-2581C, the manufacturer (fabricator or assembler) and designer can use their specific viewing formats, while sending the information in a neutral format. This avoids the need for fabricators to use customer-specific TQ formats. Product engineers can use a single, standardized GUI.

The approved DfM files can be electronically stored within the IPC-2581 file instead of on an engineer's hard drive or another database.

Some of the changes in addition to DfX module in revision C include:

- Overhauled support for rigid-flex, with support for multiple stack-ups by rigid-flex zones, as well as complete bend information that includes bend line, bend area, bend order, bend type, direction, radius, and angle (**FIGURE 1**).
- Support for embedded components (face-up/down – mirrored/not, pins on top) (**FIGURE 2**).
- Impedance requirements can now be defined per logical net or physical net segment, in addition to the traditional per-layer or per-stack-up methods.
- Impedance or attenuation requirements can now be expressed in terms of loss (dB/inch or dB/mm). Also, power, signal or voltage loss can be defined for test or other purposes.
- Ability to specify net-shorts for RF circuits or other circuits that have been intentionally shorted.
- Pin polarity support enhanced – component pins can now be tagged with a property to specify polarity, for example plus and minus for a polarized capacitor, or anode and cathode for a diode.
- Ports definition for wire bonds to custom or off-the-shelf ICs, connectors to daughtercards, and pads to custom ICs. The custom ICs and daughtercards can be defined in a different step to the main board step, creating a hierarchical



board structure within the same IPC-2581 file (FIGURE 3).

- Component support enhancements, in addition to embedded components, include formed/printed components, negative body extension for package body below pins and silkscreen/outline/assembly on opposite side of board.
- Simple 3-D shapes to define coins or other objects (FIGURE 4).
- Edge plating.

IPC-DPMX (IPC-2581) revision C provides an innovative solution for addressing the needs of the industry.

Revision B saved design houses and manufacturing partners time that was otherwise wasted toward aligning both parties on the design expectations. With a unique and previously unmet need for intelligent, traceable bidirectional DfX exchange to complete support for rigid-flex PCBs to embedded component support, IPC-2581C streamlines design handoff and manufacturing intent communication, saving time. It remains the only open, neutral standard that can do this, and enables smart factory automation when used in conjunction with IPC-CFX. □

HEMANT SHAH is an EDA veteran and chair of the IPC-2581 Consortium (ipc2581.com).

Listen to the IPC-DPMX authors discuss the new standard on the PCB Chat podcast (<https://upmg.podbean.com/e/pcb-chat-episode-66-the-ipc-2581-consortium-on-electronics-data-transfer>).

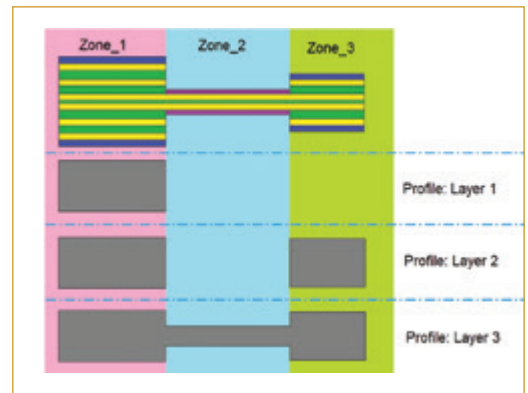


FIGURE 1. The new spec supports rigid-flex with multiple stack-ups (top) and all types of bends (bottom).

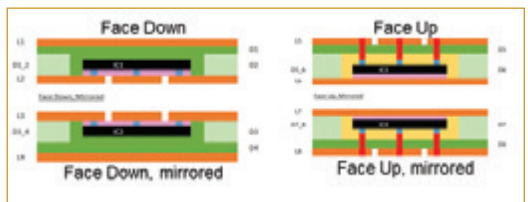


FIGURE 2. IPC-DPMX supports all types of embedded components.



FIGURE 3. Custom ICs like wirebonds can be defined separately from the main board.



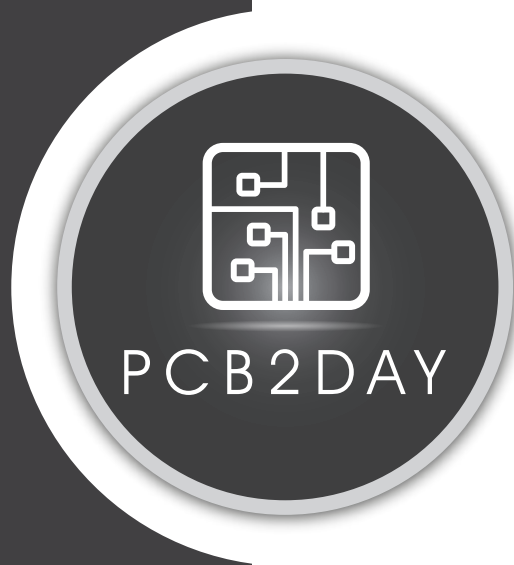
FIGURE 4. Thermal relief coin.

“Polar’s customers in the design and PCB fabrication community welcome a move to a consistent format for data transfer that permits efficient and open communication between the designer’s tools and the fabricators environment. Polar commits to support both export and import of IPC-2581 compliant stackup data from Speedstack PCB and Speedstack Si.”

— **Martyn Gaudion**  
Polar Instruments

ipc2581.com

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# Chiplet Implementation via VIRTUAL PROTOTYPING

Assessing the cost vs. performance tradeoff. by STEVE WATT

In the evolution of silicon implementation, creative solutions to costly problems have become standard practice. One of these solutions is the use of a “chiplet.” A chiplet is precisely what it sounds like: a smaller version of a chip. This doesn’t mean it’s a miniature version. It means that only critical functions that derive significant benefits from a 5 or 7nm fabrication process are included on the chip. Other functions that will work well with 10nm or greater can then be fabricated with appropriate cost savings.

Chiplet technology creates a challenge, however. If all functions were included in the chip, the interfaces could more easily be measured and evaluated. These items now must be accounted for on a package or, more accurately, a system-in-package (SiP) (FIGURE 1). This places greater importance on the electrical characteristics of those interfaces and how that SiP implementation affects that behavior. Thus, there is a need to rapidly assess these issues with minimal effort for

maximum results via virtual prototyping.

Virtual prototyping is inherent in all types of designs, be they mechanical, electrical, structural, or electronic. Using software that allows entered data to create various permutations of complex integrated circuits in a 3-D view with many underlying performance characteristics and configurations is a boon to today’s electronic designers challenged with meeting cost and specific performance measures.

Using an integrated design environment for single and multi-die, or chiplet packages for wire-bond, flip-chip, and high-density advanced packaging, electronic designers may harness the capability of early prototyping using different chips and package data. This enables designers to quickly evaluate design iterations while leveraging various wizards built into the packaging prototype software. These iterations can be evaluated against performance goals and cost estimates to arrive at the best solution. If needed, updated assignment information can be passed back to the chiplet design and into the PCB domain.

## Cost Savings

As mentioned, a significant advantage of chiplet implementation is cost savings.

Physical design and prototype costs are rising rapidly. They are becoming cost-prohibitive in a technical universe that continually demands new and unique functionality.

To develop a 5nm chip may cost \$600 million or more. The high price of development has stirred interest in exploring more cost-effective options.

In addition to cost, packaging is an issue. In 2019, the VLSI Symposium surveyed attendees regarding semiconductor integration using 3-D packaging technologies. Specifically, respondents were asked about the use of advanced packaging integration for logic, logic to memory, or logic to analog RF technologies, or all the technologies combined. They all indicated significant interest in shifting advanced packaging intervention via chiplet integration.

How can electronic package design, using a chiplet approach for heterogeneous integration, lead to cost savings or other advantages?

At the forefront of savings is reduced die size. The smaller processor die size reduces the cost of the processor. Less silicon is used when designing to the higher nanometer ratings. A smaller die size leads to higher yield and increased reliability. Using different technology nodes for the processor – vs. the memory – can also realize cost savings.

With a more generic approach using chiplet integration, a chip can be shared across multiple products; design once, then spin off into multiple different ver-

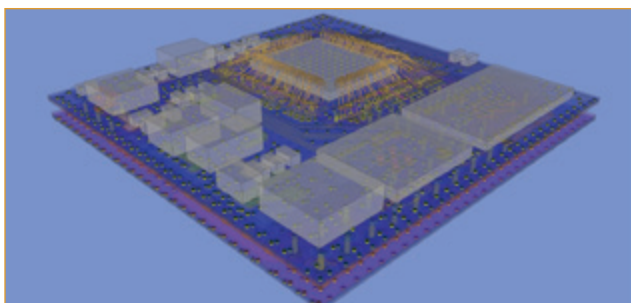


FIGURE 1. Example of a system-in-package (SiP) design.

sions. The design is economized.

### Chiplet Integration Advantages

When it comes to package design, the following advantages of chiplet integration have been identified.

1. Achieve partitioning to create multi-chip “floor plans”:
  - Consider power distribution, both for package die and off-die.
  - Achieve desired power efficiencies within specification.
  - Attain verifiable connectivity to support standard protocols.
  - Reduce or minimize crosstalk and noise.
  - Evaluate and manage any thermal issues.
  - Support a power delivery architecture aligned with the specifications.
2. Achieve heterogeneous integration and consider all factors influencing SiP design:
  - Resolve multiple interfaces between different tools for the chip design and SiP design.
  - Enable feasibility studies at the conceptual design phase.
  - Rapidly evaluate different approaches and determine the best path forward via feasibility studies.
  - Verify any information from the proposed design against original details, giving due consideration to different tools used. **[FIGURE 2]**
3. Achieve a more flexible design environment:
  - Establish a seamless integration between the IC or chip, package, and PCB.
  - Enable an ability to move between different fabrics as quickly as possible.
  - Be able to merge fabrics as needed and verify their respective connectivity is aligned.
  - Ensure rapid analysis capability exists in the initial design phase.

- Check that design goals and objectives are being met, and the overall design approach is viable.
4. Achieve rapid prototype design objectives:
    - Enable the iteration of feasibility studies with a short turnaround time with chip and package prototyping design performed simultaneously.
    - Enable autorouting between chiplets and chip to package, and determine tradeoffs and changes as needed.
    - Ensure seamless power and signal integrity verifications during design to allow front-loading of the design and converge viable configurations.
  5. Achieve efficient bump placement:
    - Achieve design bump placement and I/O cell floor planning while ensuring routability and electrical characteristics.
    - Synthesize bump placement, bump net assignment, and I/O cell placement within specified design constraints.
    - Allow flexible tile configurations to

converge on an ideal solution.

- Incorporate bump changes due to die or package optimizations without restarting the design flow.

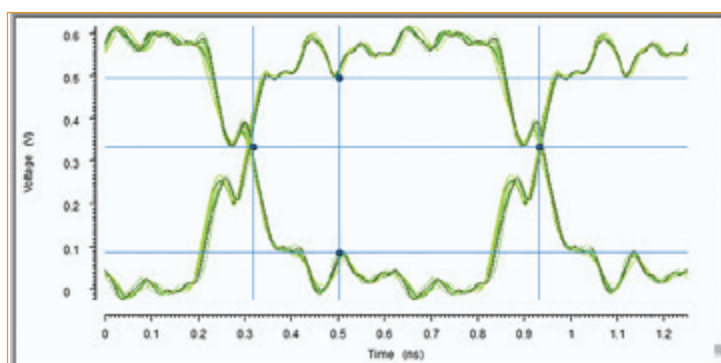
### Practical Use Cases

The scalability afforded by a chiplet approach to heterogeneous integration has led to cost and power savings in specific applications:

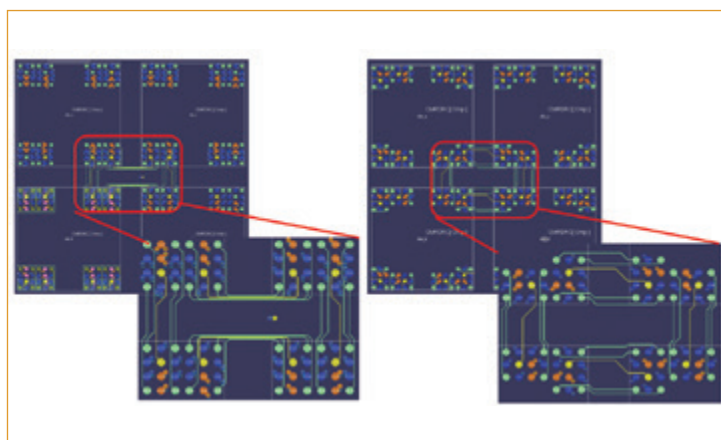
- Intel’s embedded multi-die interconnect bridge (EMIB) or Foveros (Foveros is a high-performance 3-D integrated circuit), or a hybrid of the two, enables Intel to restrict die size and permits it to be economically manufactured with a conventional yield.
- AMD has a 32Mb core “Zen” architecture. With a design split into four chiplets, the cost is reduced by as much as 60%.
- Nvidia produces a ground referenced signaling (GRS interconnect). It permits low-power data transfer among the dies, with scalability. This scalability enables notable cost savings.

Virtually prototyping ICs is inexpensive and cost-effective. We tested a situation where CPU core chiplets were placed on a fan-out wafer-level packaging (FOWLP). The chiplet size was 2.5mm x 2.5mm. The chip had eight interface blocks facing downward, upward, right and left. The interface block was 0.45mm x 0.6mm. The SiP or package size was 15mm x 15mm with four layers and lines and spaces of 5µm.

In chiplet prototype design, the top bump cells were created and utilized as templates for bump placement. Chiplet bumps in I/O cell floor plans were then synthesized. I/O cells were then placed in consider-



**FIGURE 2.** Waveform analysis of signals on the SiP.



**FIGURE 3.** SiP-level routing of the two different configurations under consideration.

*continued on pg. 44*

# Are OLDER STANDARDS Still Valid, or Holding the Industry Back?

That's one of the questions the new leadership at HDP plans to address in 2021. by **MIKE BUETOW**

This month Marshall Andrews stepped down as the longest-serving head of The High-Density Packaging (HDP) User Group. But as Larry Marcanti assumes the role of executive director of the decades-old electronics consortium, don't expect big changes.

On Andrews' 15-year watch, HDP's membership increased by more than 30 companies, to reach more than 50 total. The ongoing project portfolio rose from five to an average of 25 member-driven activities.

Despite the Covid-19 lockdown, HDP is coming off one of its most successful years yet, having completed 13 projects.

Marcanti and HDP facilitator John Davignon gave an update of the consortium's latest work and future plans in an exclusive interview with *PCD&F/CIRCUITS ASSEMBLY* in December.

**MB:** Larry, you've taken over as executive director from Marshall Andrews. Do you see any major changes to the goals of the organization going forward?

**LM:** We had a pretty successful run with Marshall at the helm. I don't see any major changes going forward, except maybe bringing in more from a "technology futures" perspective. Our members are interested in understanding more about where the technology is going. We are looking at ways to talk to other groups and consortia to view where they are and cover that with our membership to look at the key future technologies.

Automotive is an example of that. We (HDP) don't have any automotive-centered companies. We had a webinar where we had different folks from the automotive sector come in and talk to better understand it ourselves. We have many suppliers and OEMs in our group. We've traditionally been focused more on networking equipment. Covid has thrown us for a loop. We had planned for an automotive workshop in Europe this past May to get more automotive representation. We wanted to get more of the supply chain involved. Automotive companies are also more proprietary about what they are doing insofar as electronics is concerned.

**MB:** And that industry has changed a lot over the past few years. It's not just Tesla. All the automakers are getting into electric vehicles, and the electronics for EVs aren't like your everyday Honda Accord. These are really high-power boards.

**LM:** Right. We're talking about performing CAF testing at 1500V and not electrocuting the testers. We have problems like that, which most folks in our industry haven't faced head-on before.

We developed a skeleton automotive project and are looking to get OEM input for it. We have reached out to several companies for input. That project is focused on providing a high current/voltage guideline for building PWBs for the 800V+ EV and HEV automotive industry.

We have an outline of a project now, but to make it relevant, it takes someone working in that business to give us input on their key issues. We are in the infant stages of that now.

Longer-term, we'd like to get back out like everyone else and do more traditional networking and collaboration.

**MB:** How do you ensure there's no overlap or redundancy with consortia like iNEMI that are also working on automotive electronics?

**LM:** We communicate quite a bit with them. We collaborated with iNEMI on the Harsh Use Environment Alloy project. It's not smart for our members to have two separate projects doing the same thing.

We will have a similar approach to automotive.

We also have a class of projects called emerging technology. We've looked at novel ways of building PCBs. We have also looked at products that are used in harsh-use environments. New solder alloys are touted to be better for harsh-use environments. Autos operate in harsh-use environments, and automotive electronics companies may see a benefit in the future.

**MB:** I suppose Covid interrupted a proper send-off for Marshall.

**LM:** We plan on doing that at our next opportunity to meet face to face. We are targeting that for spring.

**MB:** Is Marshall retiring?

**LM:** He is taking a different role. Marshall will still be active in HDP. His title is executive director emeritus. He will give counsel to me and give his two cents to the board of directors whether it's asked for or not. (laughs)

**MB:** Was his decision a recent one or something that he planned?

**LM:** Marshall let the board know. They did an executive search for a new leader. I was successful in getting that position.

**MB:** What else should we be looking for from HDP in 2021-22?

**LM:** I see 22 active projects right now. We completed 13 projects last year – that's a record. Maybe because everyone was home. (laughs) We always have new projects coming. There are three new ones.

The Harsh Use Alloy Evaluation 2 project is looking at increased dwell times. Some of these materials have very different metallurgies. The typical ATC testing uses a 10-minute dwell time; we are now looking at a 60-minute dwell time to better understand alloy degradation using a dwell time more characteristic of service conditions.

Then there's the Automotive PWB project and a new one for copper peel strength.

**JD:** We are looking at standards and guidelines for some of our projects. The Copper Peel Strength and Glass Type Comparison projects are looking at older standards. We are questioning if they are still valid, or are they holding the industry back? For copper peel strength, what's the peel strength you really need to build a board, and are they keeping the copper suppliers and OEMs from moving into higher speeds?

For glass, it's questioning all the new glasses, like low-loss and low Dk glasses; are they an entire class by themselves, and does UL need to test everything coming our way? Or are their fundamental properties similar to e-glass, and can they be allowed without retesting? You can imagine how upsetting it

will be if everything must be requalified because of the e-glass style changes. If the property changes more than the limits allow, they might have to retest, which will be a burden for the industry. We are evaluating if that's a need.

**MB:** With regard to the glass type comparison, can you talk about how those evaluations are done? Will new tests be needed?

**JD:** That's a good question. Right now, UL 746A allows a 15% difference in flexural/tensile/impact strength and 10% for dielectric strength. If there's a >15% difference, UL considers

it to be a different material. We are just getting the results now to determine whether the new low Dk glass laminates are inside or outside that range. We may learn whether we need a different type of test, but at this time, we are evaluating the standard test protocol. Glass was never really thought of because it was always "e-glass"; it was "just an inert structure of the composition." Many standards didn't look at this; it was always the resin and fillers that required new testing. But that's changed. UL

is the HDP project leader on this, so it's not a matter of having to sell them. They are helping to make this determination. We have an HDP member who is really asking the question, and we have a lot of suppliers and OEMs who always have a lot of skin in the game to help with samples.

**MB:** Is the 15% limit arbitrary, and if so, do we need to change that?

**JD:** I can't comment on that. We are in the data-gathering phase. If everything came up 18%, should we move the cutoff to 20%? I don't know. UL is there to make sure things are safe, and the industry is protected. I don't know how they would arbitrarily move a spec, but once we get the data, we might be able to do that analysis. Maybe the mechanicals aren't the only way to look at it. Perhaps long-term aging, which has always been a significant part of the testing, will give more insight. It's hard for me to imagine the glass would affect the resin/filler structure for that, but we are right at the cusp of finishing the



Does the industry need to change the way it assesses e-glass?

*continued on pg. 38*

# PCB Chat

## Recent Chats:



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with  
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**Changes in the Mainstream PCB CAD Market**  
with  
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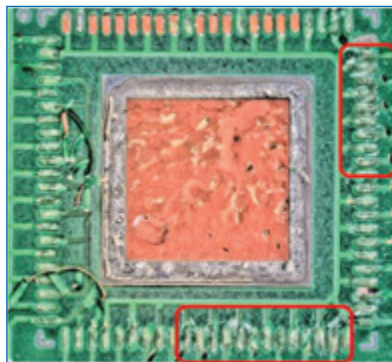
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# PROCESS CONTROL PLAN to Monitor Acceptable Levels of Flux and Other Residues

Because electrochemical failure risk is site-specific, different components need different plans. by **BILL CAPEN, JASON EDGAR, DR. MIKE BIXENMAN and MARK MCMEEN**

Highly dense electronic assemblies incorporate bottom-terminated components. Miniaturized components create numerous challenges, resulting in a shorter distance between conductors of opposite polarity, solder sphere size reduction, low-standoff gaps, flux entrapment under the bottom termination, blocked outgassing channels, and more significant potential for leakage currents.<sup>1</sup>



**FIGURE 1.** QFN-88 that failed SIR testing.

In the presence of humidity, moisture (mono-layers of water) hydrogen bonds with ionic contaminants to create an electrolytic solution. Ions such as flux activators can dissolve metal oxides present in the flux residue at the soldered connection.<sup>2</sup> When

the system is in operation, the electrical field attraction of the positively charged metal ions migrate to the negative conductor. These metal ions can plate small dendrites, resulting in leakage currents and/or parasitic leakage. As such, ionic residue testing is used to test for problematic residues that could hinder reliable circuit function.<sup>3</sup>

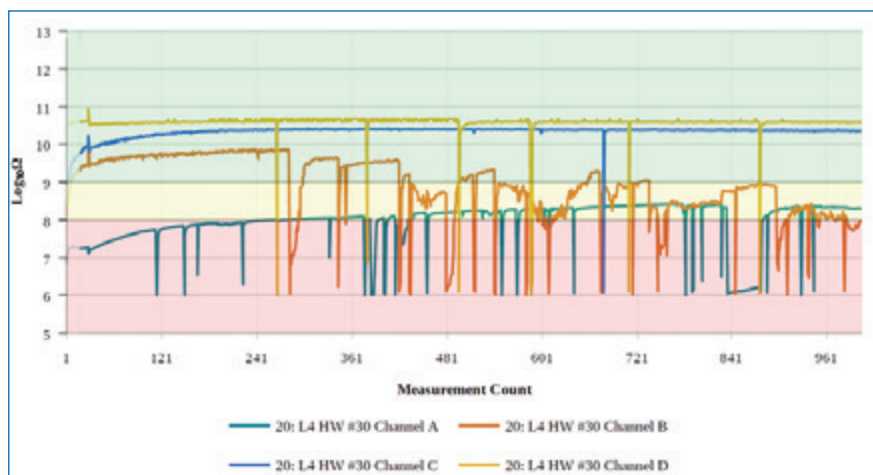
The core concept for materials compatibility and residue acceptability is a qualified manufacturing process (QMP).<sup>4</sup> In a QMP, the manufacturing materials and processes used to produce electronics hardware have been benchmarked and validated against electrical performance in hot/humid conditions. The art of characterizing what chemical residues exist on a manufactured assembly allows an assembler to determine the impact of those residues on electrical performance. The test methodology is useful in developing a risk profile.

After a manufacturing process has been qualified, the next step is to define how to monitor that qualified manufacturing process for ionic residues. The establishment of an ionic process monitoring plan is a requirement for mission-critical, high-reliability electronic products. The sampling plan for ionic residues should be periodic, and with sample sizes such that a manufacturer has confidence, the process is in control.

## High-Performance Electronic Products

The classification we build products to is IPC Class 3/A. Class 3/A boards call for very stringent manufacturing criteria, since the boards must remain operational in critical conditions. The electronics must provide continued performance and performance on demand. When deployed, there can be no equipment downtime. The products must work correctly every time.

Processes for building the electronics must be qualified and validated. No process residues are accept-



**FIGURE 2.** Failed SIR testing result.



able. Once validated, there must be a process control plan. Site-specific characterization on components with the highest probability of electrochemical failures is required to ensure every component is reliable.

Materials characterization must be in compliance with IPC J-STD-001 [Rev. F – H] Amendment 1, *Cleanliness*. Testing requires custom test boards that detect electrochemical reliability across different component designs. Once qualified, there must be a process control plan to monitor for cleanliness on challenging components and processes that are representative of production hardware.

Highly dense electronics are now designed with miniature components. Designs require leadless and bottom-terminated components. These component types create numerous challenges. The problem is these components trap flux residues under the bottom terminations. They are harder to clean. With a tighter pitch, there is a shorter distance between conductors of opposite polarity. Tighter pitch poses a greater risk to reliability.

**FIGURE 1** is a QFN-88 component that had partially cleaned flux residues left under the bottom termination after cleaning. Surface insulation testing detected leakage currents. The components were sheared off the board and inspected. Monitoring for these types of defects on high-risk components offers a useful process control method.

## Process Control Plan

Temperature-Humidity-Bias (SIR test method) was studied for use in developing a process control plan. Our operations favor electrical resistance measurement methods. The reason: Electrical resistance measurement permits detection of process residues that are both ionic and non-ionic. These process residues are located under the components' termination and commonly bridge conductor pathways. The residue is not visible to existing process control methods, specifically the resistance of solvent extraction (ROSE). We are looking for process deviations. Is our process consistent lot-to-lot? Is there variability?

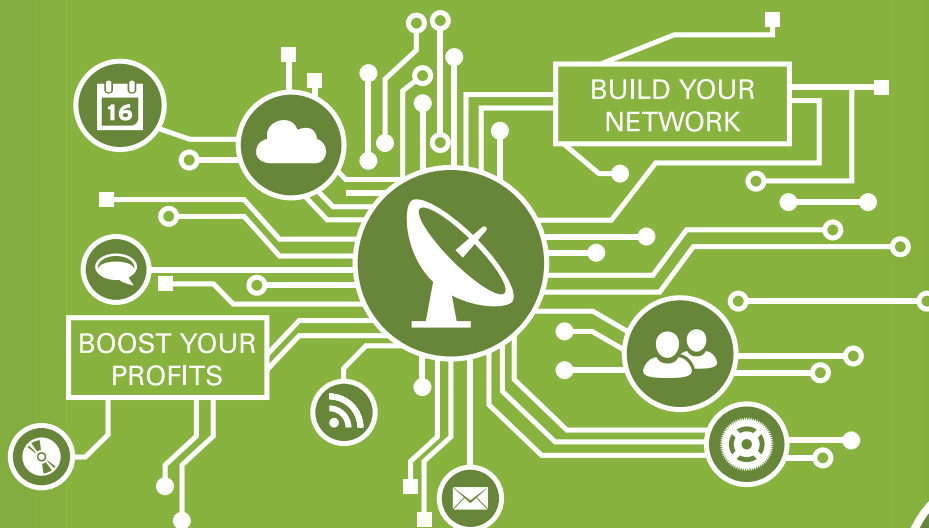
IPC pass/fail for SIR testing is  $8 \text{ Log}_{10}\Omega$ s. For this experiment, we decided to build in a margin of safety by setting the lower SIR limit at  $8.5 \text{ Log}_{10}\Omega$  resistance. **FIGURE 3** illustrates the mean insulation resistance on a specific component. The lower and upper limit was set from  $8.5 \text{ Log}_{10}\Omega$ s to  $12.0 \text{ Log}_{10}\Omega$ s. The chart shows all 10 boards tested were within the specification range.

## Research Hypotheses

The following are our temperature/humidity/bias hypotheses:

1. Electrical resistance measurements under bias and elevated environmental conditions are long-accepted quality metrics.

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2. The first hours of a test card subjected to temperature/humidity/bias voltage represent the most ionic activity/change.
3. This change can be used to determine the similarity of the process. (Similarly cleaned and produced boards should have similar starting resistance values, end resistance values, and general curve shape.)
4. Deviation in process should be visible as a change.

**Test board.** QFN-88 and QFN-124 components were selected for this study. A custom SIR test board was designed with the QFNs horizontally positioned in Q1 and Q2. The QFNs were rotated 45° in Q3 and Q4 (**FIGURE 4**).

The 0.5mm pitch QFN 88 chip is representative of production hardware (**FIGURE 5**). The tight pitch and large thermal lug are useful in defining cleanliness levels under similar component package styles. This part can be used to test no-clean flux systems for SIR cleanliness levels and to determine whether the cleaning process is capable and efficient in achieving the desired SIR levels for these types of component packages.

The 0.5mm pitch QFN-124 BTC has a dual-row pin-out with ground lug, which makes this particular BTC more challenging than the standard QFN package style, which is a single row around the periphery of the package (**FIGURE 6**).

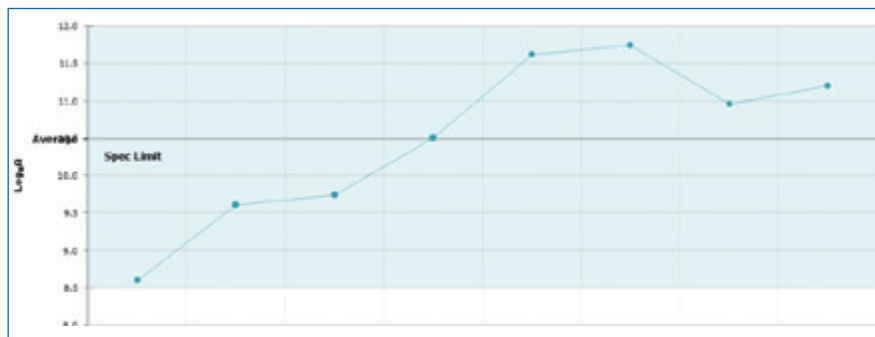
## Experimental

Phase 1: Data collection.

- Perform a series of temperature-humidity-bias tests with the same card to monitor process deviations.
- Perform ROSE as a direct comparison.
- Collect the raw data and analyze the data for statistical significance within several blocks of time: first 30 min., first hour, 2 hr., 6 hr., etc.

Phase 2: Process deviation monitoring.

- Tests must all be run under the same conditions.
  - Ramp speed of the chamber will be a factor, so it will be critical all tests are run with the same chamber.
  - Chamber control feature should be used on a powered-down chamber to ensure all tests start under the same ambient conditions and rise in a similar fashion.
- Tests must all end at the same time.



**FIGURE 3.** Electrical resistance of 8.5 – 12 Log<sub>10</sub>Ωs.

- For this experiment, analyze the data within defined periods.

The SIR testing unit process control module allows the user to create and manage their test boards. Specific fields enable one to set up a particular process control profile. For each channel on the test board, the user can name the profile, and set an upper and lower specification limit. Other settings include time duration, measurement interval, temperature, relative humidity, bias voltage, and measurement voltage.

## Data Findings

Twenty test boards were assembled and cleaned using defined process settings. The test boards were subjected to SIR testing using the following settings:

- Temperature: 40°C
- Relative humidity: 90%
- Bias voltage: 5V
- Measurement voltage: 5V
- Measurement interval: 5 min.

Results were analyzed over a variety of periods. Baseline ROSE testing was performed on test samples.

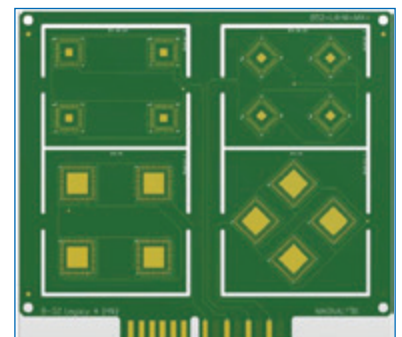
**FIGURE 7** is a chart of the SIR results for board #11. Channels A&D represented the QFN-88, and Channels B and C represented the QFN-124. The QFN-88 values were below the lower limit, which is not acceptable. The QFN-124 values were acceptable.

In a review of the data, we noticed parallels between the early-stage data and the full 168-hr. data that supported our hypothesis. **FIGURES 8** to **11** show the mean data for each of the 4-channels on all 20 test cards in our data set.

Following SIR testing, each of the 20 boards was ROSE tested (**FIGURE 12**).

## Data Analysis

- Data was initially plotted in its entirety to look at overall trends.
- A smoothing function was applied to visualize the trend in the data better.
- General observations:
  - The dual-row QFN-124 SIR profile appears to be more promising due to a tighter standard deviation.



**FIGURE 4.** SIR test vehicle.

- QFN-88 had a relatively uniform spread of data over the range of 7 to 11 Log<sup>10</sup>Ωs. Many data points were below the lower limits. Clearly, the cleaning process was not properly dialed in to clean this part within the upper and lower specification limits.
- The higher variation QFN-88 results in a higher standard deviation. A higher standard deviation indicates a lack of consistency with regard to ionic residue present at the signal pins and under the component termination.

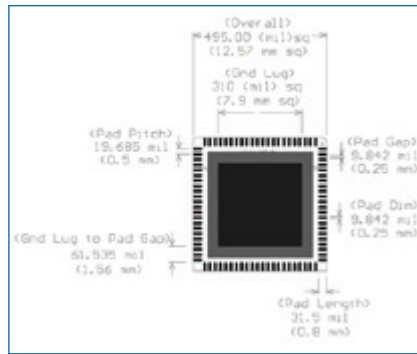


FIGURE 5. QFN-88 single row dimensions.

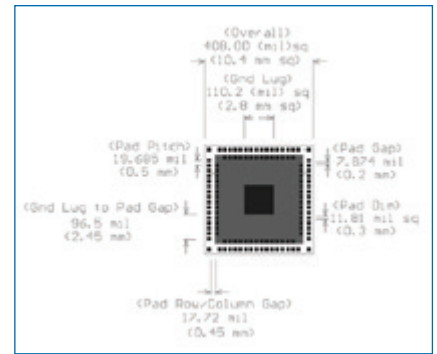


FIGURE 6. QFN-124 dual-row component dimensions.

FIGURES 13 and 14 represent the average SIR values per hour of testing. The mean and standard deviation were plotted over time (FIGURES 15 and 16). The following observations were made:

- SIR value tends to start to flatten out around 50 hr.
- Specific periods had larger variation than others.
- This is probably noise-related.

**Inferences from the data findings.** Electrochemical risk factors are not consistent across a printed circuit board; instead, they are specific to components that trap residues under the bottom termination and next to signal pins. The data find different meaningful results between the QFN-88 and QFN-124.

In this study,

- QFN-88 was harder to clean.
- There was higher variability.
- QFN-88 had many unacceptable results.

Temperature-Humidity-Bias Environment

- Induces defects from ionic residues on targeted components.
- Induces defects from non-ionic residues on target components.
- These defects are reflective of undesirable process deviations.
- Electrochemical risk is by nature site-specific, rather than an average risk assessment.

Inferences include:

- The large standard deviations on the QFN-88 component require more work to optimize the cleaning process.
- Temperature-humidity-bias testing is useful to determine the similarity of the process.
- A shorter SIR test time can detect process deviations.
- Contamination is not consistent across the PCB.
- Some component types are at greater risk of electrochemical failure.
- ROSE testing is not a predictable method for site-specific testing.

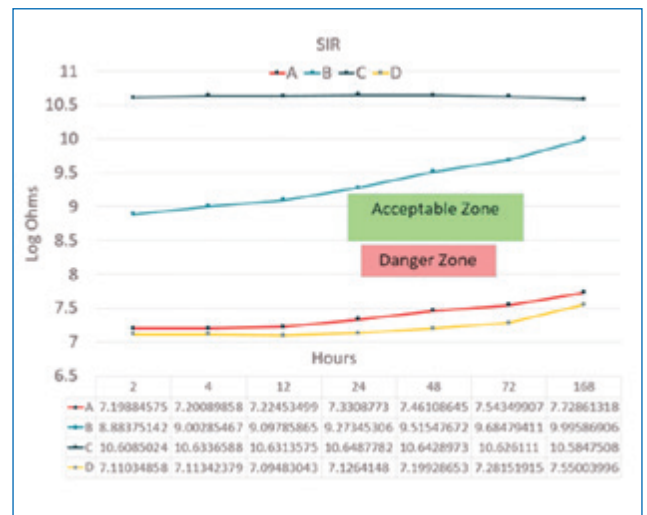


FIGURE 7. SIR test values for board #11.

## Research Hypotheses

Hypothesis #1: Electrical resistance measurements under bias and elevated environmental conditions are long-accepted quality metrics. Hypothesis #1 is accepted for the following reasons:

SIR testing is considered the gold standard for detecting ionic contamination. SIR is the best test method for determining the electrochemical reliability of:

- High-density interconnected board designs populated with miniaturized leadless and bottom-terminated components.
- Multiple soldering operations that include SMT components on the top and bottom side of the board.
- Through-hole processes using both wave and selective soldering.
- Rework and repair operations.
- Conformal coating materials characterization.

Hypothesis #2: The first hours of a test card subjected to temperature/humidity/bias voltage represent the most ionic activity/change. Hypothesis #2 is accepted/rejected for the following reasons:

Accepted: When ionic contamination is present, SIR will be lower at the beginning of the test. The QFN-88 insulation



**FIGURE 8.** QFN-88 Channel A charts plotted over different time periods.

resistance had lower insulation resistance at the beginning of the test. As the test ran, the insulation resistance improved due to the ionic residue drying out and not being mobile in monolayers of water present in the humid environment.

Rejected: A short test period does not detect leakage currents and dendritic formations. These typically require longer test time to form and propagate.

Hypothesis #3: This change can be used to determine the similarity of the process. (Similarly, cleaned and produced boards should have similar starting resistance values, end resistance values, and general curve shape.) Hypothesis #3 is accepted for the following reason: The research finds that much can be learned from careful analysis of the first hours of the long



**FIGURE 9.** QFN-124 Channel B charts plotted over different time periods.

accepted SIR test method. The first hours clearly detect process contamination that reduces insulation resistance.

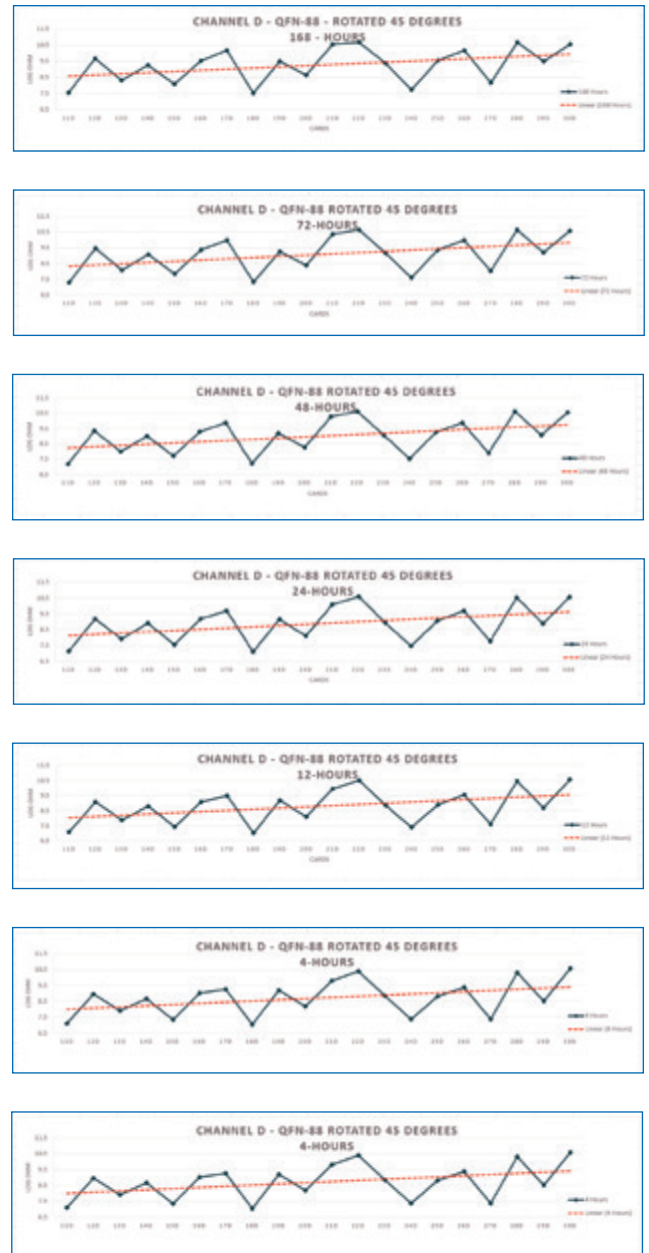
Hypothesis #4: Deviation in process should be visible as a change. Hypothesis #4 is accepted for the following reason: The QFN-88 was clearly different from the QFN-124. Process contamination was detected.

## Conclusion

Electrical testing results, with power on during extremes of temperature and humidity, detect the presence of ionic contamination. The challenge industry faces today is the risk factor for electrochemical failures is not the same across a PCB. The risk is site-specific, being more problematic across



**FIGURE 10.** QFN-124 rotated 45° Channel C charts plotted over different time periods.



**FIGURE 11.** QFN-88 rotated 45° Channel D charts plotted over different time periods.

different components.

Process control requires an objective sampling plan for measuring ionic residues of the process. This study looked at two test methods. The ROSE bulk extraction test method is a nondestructive test method that can be used on the actual product. The problem is this method is not consistent in detecting problematic residues across site-specific components.

Electrical testing using SIR temperature-humidity-bias is a far superior test method. The problem with this method is it cannot be used on the actual production board. This method requires a test board or coupon that is representative of the complex components used on production hardware. When using a representative test board or coupon, this test method can be used to monitor and control the process with accuracy.

**Follow-on research.** Follow-on research is needed to develop a “process control plan.” The research team plans to perform a series of tests by first developing the “golden image” to define upper and lower process limits. Using the same test card, the process will be varied to validate the method work for detecting the cleanliness state.

### Acknowledgments

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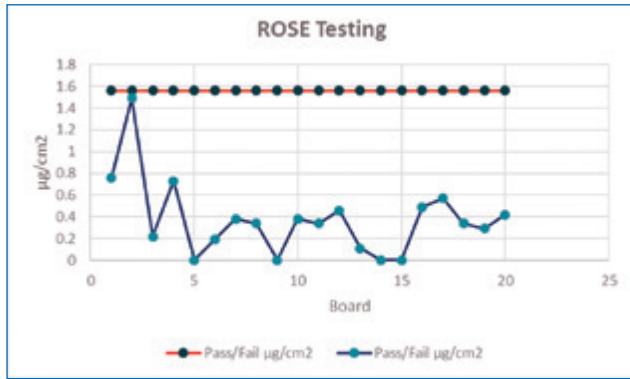


FIGURE 12. ROSE testing for each board.

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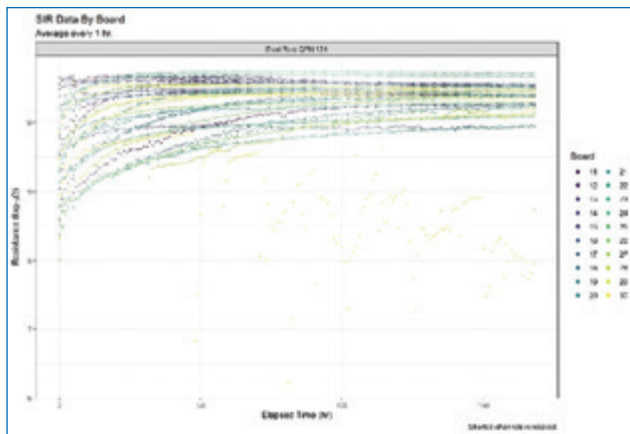


FIGURE 13. QFN-124 average per hour.

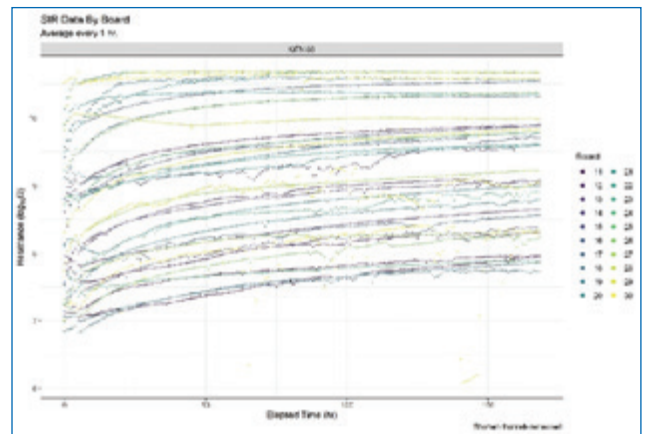


FIGURE 14. QFN-88 average per hour.

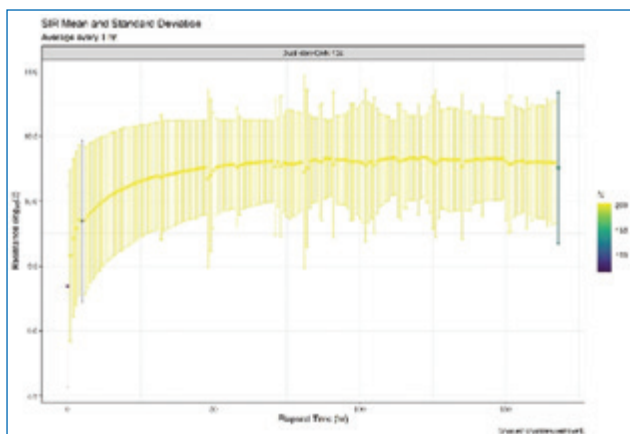


FIGURE 15. QFN-124 mean and standard deviation averaged every hour.

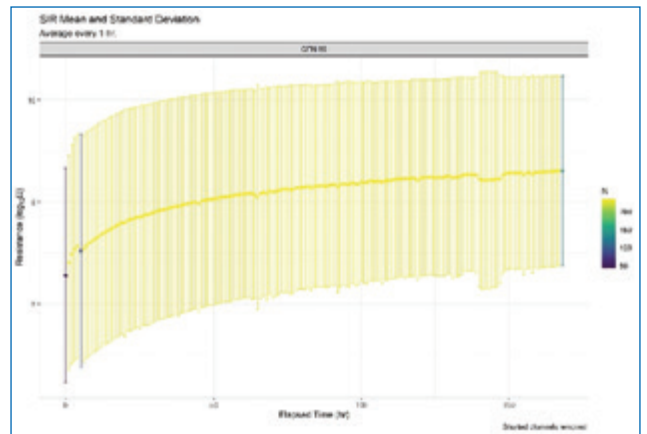


FIGURE 16. QFN-88 mean and standard deviation averaged every hour.

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# Lights Out at USI

The EMS behemoth is on the cusp of an all-automated future.

BY MIKE BUETOW

By almost any measure Universal Scientific Industrial is an EMS behemoth. Yet most of the press surrounding USI over the past few years has been tied to its recent acquisition of AsteelFlash. The deal, completed last month, added 17 manufacturing sites and about \$1 billion in topline revenue. For the first time, USI will have sites in the US, Africa and Western Europe.

Today, USI has 27 manufacturing locations in 10 countries, over 24,000 employees and revenue of more than \$7 billion. That's good for the 11th spot in the current CIRCUITS ASSEMBLY Top 50 rankings. There's no missing the company now.

Yet for all its size, USI could just as easily be recognized for its technical prowess. The company is on the cutting edge of so-called lights-out manufacturing, where few if any staff are found on the factory floor where hundreds of SMT machines run seamlessly, connected by sophisticated software and AGVs feeding the cells on a just-in-time basis.

Jim Cao, general manager of the Greater Shanghai and Smart Manufacturing/SiM business unit, USI, is charged with developing and overseeing the company's worldwide Smart manufacturing strategy. The company is entering year six of the plan, and the progress is notable. He spoke about how Industry 4.0 has changed the way the EMS firm operates with CIRCUITS ASSEMBLY in late November.

**MB:** In a press release on Nov. 10, you said, "USI is adopting Smart manufacturing to enhance our competitiveness through the digitalization of our production processes, including the automation of infrastructure and logistics using robotics and automated guided vehicles." What does Smart manufacturing mean to USI?



**FIGURE 1.** All inspection machines from SPI to AOI are linked and constantly driving process improvements.

**JC:** At USI, we have a very detailed Industry 4.0 Smart manufacturing plan and roadmap. We call it Worldwide 5 Star I4.0 Smart Manufacturing Roadmap and Management System. It lays out our stage-by-stage plan over the next five to seven years to bring up the Smart manufacturing level of our worldwide factories. Every year we measure the progress we made. We have month-by-month reviews of the system, and at the end of the year we do a more careful rating of all the factories of the progress made toward the goal.

Our Smart manufacturing definition is based on the Industry 4.0 contents, and it has four pillars:

1. Automate all machines. The focus is to reduce manual labor and minimize any manual handling costs and issues.
2. Industry 4.0 data automation. Data automation is the essence of I4.0. It digitizes and connects all data to the central server, so we have real-time data from all production equipment and process SPC data and RMS (recipe management system). Every production lot is scan-in and scan-out at every process station using 2-D barcode. One hundred percent of the units, through the entire production line, also have a 2-D barcode system, and are scanned and loaded in a central server. We know exactly, for every unit we ship out, if there is any issue coming back; it is easy to trace back to

which unit, which shift and which hour.

3. Our Automatic Material Handling System. That fully automates our entire components incoming to the warehouse and dispatched by AGV to each SMT pick-and-place in JIT mode, right before a pick-and-place machine runs out of components (**FIGURE 1**). We have eliminated the kitting room and associated labor. Every machine we have is linked



to a production floor management system we call Shop Floor. Shop Floor is connected to our ERP system. Our data automation is integrated with Shop Floor, so we know exactly to the minute when every machine is running out of material. The system would automatically dispense the right components from Smart Storage driven by robots by retrieving right corresponding component reels and put the reel on a cart, which carries them to the corresponding machine.

- 4. AI-based learning system. We are just getting started. It's a major undertaking. We see huge potential there as well, to have the machine at a certain level, automatically adjust the inspection criteria, to reduce or reject, and also eliminate under-rejects, to inspect and fine-tune the parameters, because there are so many variables (FIGURE 2). For instance, the substrates we use have thickness variations within a certain spec range, and components do as well, so if we keep fine-tuning the process parameters within our specifications, driven by the SPI, we can improve our quality.

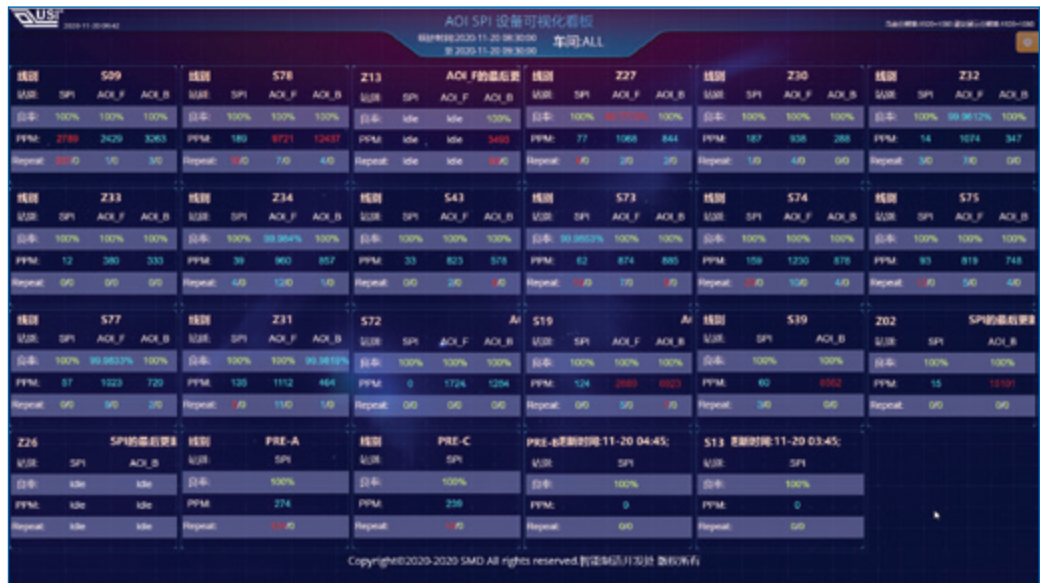
**MB:** Do all the facilities use the same equipment sets?

**JC:** We have factories worldwide. If you look at our US reporting, our business is pretty much two portions. The first part, which is the major part, is the so-called system-in-package (SiP) miniaturized modules. The second part is the EMS business.

For EMS, the equipment is less complicated than the SiP factories. The SiP factories' process flow is very similar to typical IC assembly and test factories. The only major difference is we use SMT instead of wirebond. The rest of the backend and test processes are very much the same. It's much more difficult to make modules than single-chip IC products.

Not all the factories are at the same level yet. My philosophy is we use the Zhangjian factory in Shanghai, where our Smart manufacturing development team is located, to develop all the common platforms. We use a common platform strategy to standardize the data automation protocols and equipment, which produces our development lead times and costs as well. Our strategy is to develop the common platforms, then fan out to the worldwide factories, as each factory needs it.

**MB:** Was the software, which is extensive, developed in-house, or do you start with machine software and modify it to meet your needs?



**FIGURE 2.** Robotic cells replaced hundreds of technicians and markedly improved speed and quality.

**JC:** We do both. For all the automation equipment, we migrated from the original third-party design and programming. Now a majority is in-house design and programming. Obviously, we have to integrate all the standard, off-the-shelf, third-party production software, but we work with them and integrate together, mainly through two methodologies. The first is the SECS/GEM protocol. Not all the equipment has SECS/GEM, especially the older equipment (five to seven years old). We also developed our own protocols to use with LORA IoT through machine signal tower, so we know machine status: for example, green light, yellow light, red light. SECS/GEM is by far the most flexible, comprehensive machine tool central server data communication platform. It offers two-way data transfer. The central server can control the machine, and the machine provides real-time data to the server. For older machines without SECS/GEM, it's pretty much a one-way communication from the machine to the server. It was limited data transmission from the server to the machine, unless we can work with the supplier to have access to their PLCs and machine-level PCs.

**MB:** Are the AGVs you use purchased from traditional electronics factory suppliers or from outside our industry?

**JC:** We use a third-party supplier based in China. That technology is pretty mature now. It's been in the market for the last 25 years. In my career, I first saw the AGV in the Intel factory in Chandler, Arizona, about 22 years ago. It's now popular in China.

**MB:** We in the US are way behind you.

**JC:** I'm not so sure. I worked in the States for close to 30 years. When you say the US is behind, I think the main reason is the loss of most of the manufacturing jobs, which moved to China,

initially for the cheap labor. But the China labor rate is inflating every year, and every China company is under pressure to speed up their own automation to stay competitive.

**MB:** You talked about some of your recipes. How deep does that go? Are you able to go back all the way to the component distributors or even the component OEMs and tie your inventory needs on the line, as they are starting to wear down, all the way back to the component supplier level so the just-in-time is as tight as possible?

**JC:** The answer is not yet. Let me explain a little bit. Our material planning system is very much SAP-based. We do not typically store months and months of inventory. Especially for the products we make, the material supply is quite tight. We use SAP to manage that material demand. In our Five Star I4.0 Roadmap, the last stage would be exactly what you said. We plan to integrate with our customer's ERP system, so that when the customer dumps their forecast for the next six months, by connecting their ERP with our ERP, our system automatically checks the inventory, calculates yield loss, and cuts it down to the particular component-level demand for the next six months, and automatically transmits to the suppliers' ERP system. That's a fully integrated supply chain. We are not there yet. Obviously, the reason is very much dependent on our customers' readiness and, more importantly, our suppliers' readiness.

**MB:** Have you found that component manufacturers are eager to get to that point, or are they concerned that would create less clarity for the inventory levels because of concerns of double or triple ordering during tight inventory times? How trusting are they of software-driven inventory pulls?

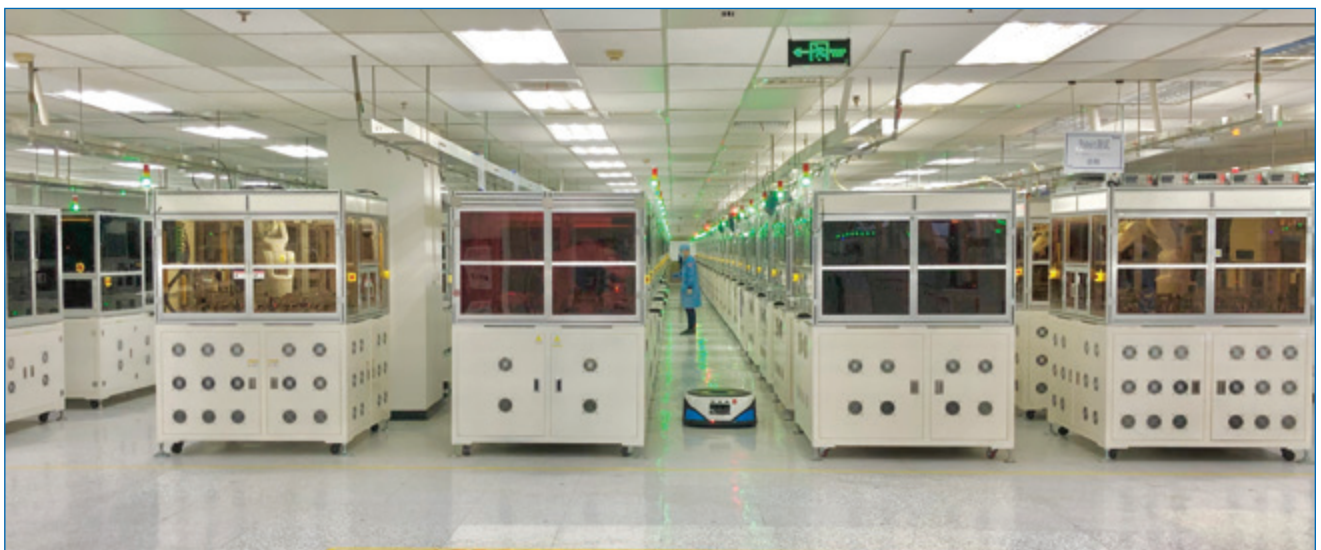
**JC:** It's a good question. Our suppliers are mostly the IC manufacturers. Our customers mostly are fabless. They typically do assembly and test in one of the major OSATs. They are not pushing that heavily yet.

In terms of their trust of their system, I think it would be much more trustworthy to them because, if we have the fully integrated customer forecast to the supplier demand system fully linked, it would take out a lot of the human errors or manipulations. It would be data to data. It's a real B2B. It would be much more accurate and trustworthy to our suppliers in terms of demand numbers. Right now, everyone is moving slowly in that direction. It will happen. There's no doubt. It will improve the productivity of our customers and suppliers and ourselves as well.

**MB:** You talked a bit about what the AGVs are doing in the factory. Are there any other areas where you have implemented robots, and if that's the case, what are you having those robots do?

**JC:** The product we make are modules. It's a system, not an individual IC. The test time for each can be very long ... a couple minutes. Each robot can support eight to 10 test sockets for long-test-time module testing. We have hundreds and hundreds of robots (FIGURE 3). In the old days, three to four years ago, we had hundreds and hundreds of operators manually inserting parts into the socket, closing the socket, pushing the button. It's a lot of human errors. Now those hundreds of human operators are gone, replaced with robots, with much higher efficiency and much higher productivity.

You probably see the AGV on the floor (Figure 3). That's the project we are working on right now. My plan is to have USI's first lights-out test floor factory next year. We're going to have at least 91 of those test systems totally lights-out, all product loading and offloading and machine status done remotely.



**FIGURE 3.** AGV move component trays hands-free across multiple floors to feed assembly machines.

We use AGVs to carry carts similar to the one on the right in Figure 1 upstairs to an elevator and then to a system next to the machine that needs the parts. It's a fully integrated AMHS system. At the heart of that is the so-called Smart Storage system (FIGURE 4). Inside are all the component reel slots, which are all handled by robots moving quite fast, managing all the component reels. They are put on the shelves and retrieved as needed, then moved on the automatic conveyor connected to the robots at the other end to put on the AGV carts.

We have lots of dashboards around the factory. One is the AMHS Smart Storage dashboard (FIGURE 5). It shows how many reels are inside, the size of them and how many parts they have on them. All the data are real-time, on display in the system and fully automatic.

**MB:** I'm assuming USI does studies every time you implement an automated system. Are there standard metrics that you use to compare how much faster and accurate and higher-yielding a particular process has become?

**JC:** There's a day-and-night difference in terms of accuracy. When we have human labor to do the work, the accuracy is way off. There's no comparison. The robot we typically use has higher repeatability, placement accuracy, +/-20 microns. Humans wouldn't be close. They're not as dependable as machines in terms of material handling.

**MB:** Regarding the Five Star Rating System, how did that name come about?

**JC:** The "five stars" name is commonly used for hotels, and

there's clear definitions in terms of what we use for one star, two stars, or a half star. Typically the measurements include the manufacturing process automation rate. For each production machine, we divide it into three steps: loading, process, and uploading. Each station has three steps.

If we automate the processing part, we still need a keyboard to load the parts, offload parts, so we only count as one of three. If we automate all, it would be three steps. So, the measuring system is doing all the manufacturing process systems. The percentage of machines connected to the data system network, we call it connection rate. It's machine downtime reduction, or MBTF-based. With I4.0 data automation, we have very much reduced machine downtime because when you have hundreds of thousands of equipment on the production floor, a lot of things are happening. When a machine goes down, the equipment technician or engineer may not know which machine is waiting for assistance.

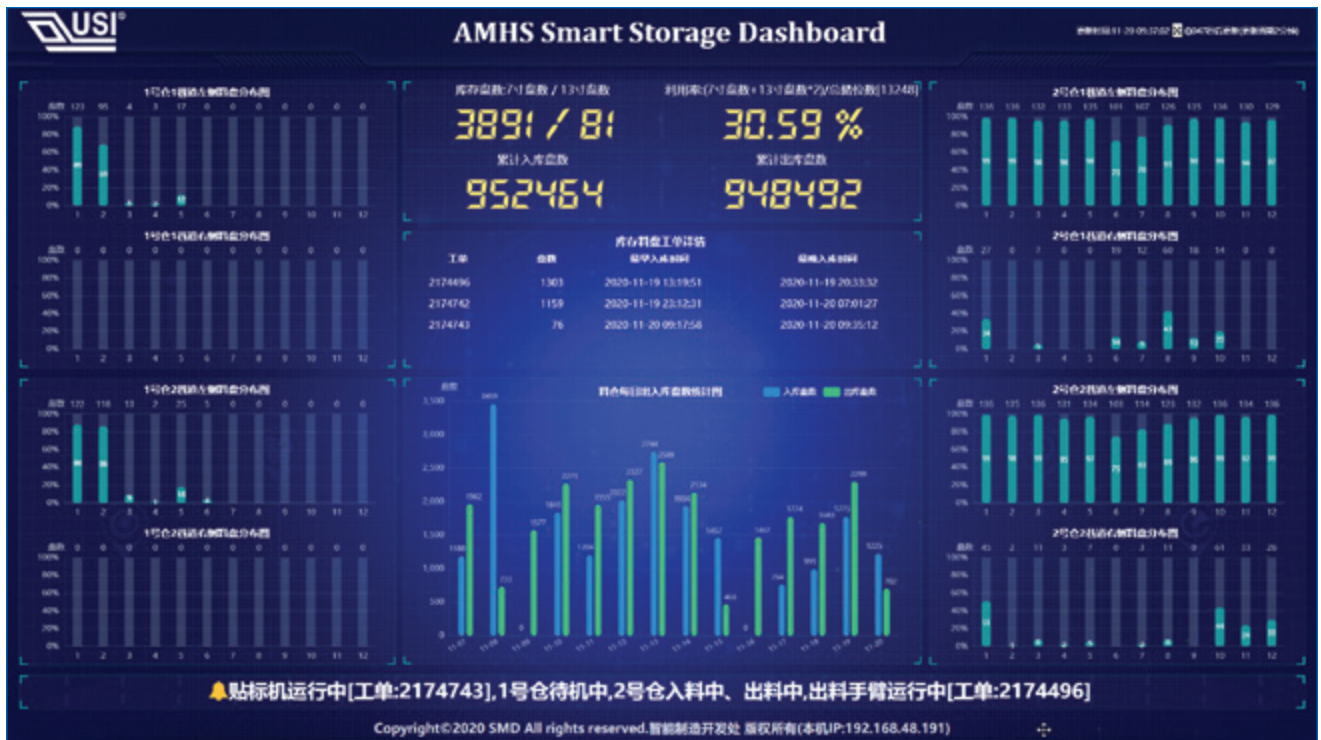
Now we have a system to send automatic text messages to the responsible engineers, so they know immediately which machine is down and what kind of problem, so they can quickly fix it, instead of wasting a lot of machine time waiting for a human. We also measure the DL [direct labor] and IDL [indirect labor] headcount reduction, which is a fundamental objective to improve productivity. How many headcounts did we reduce? What percentage? How many technicians do we use to collect data, to go to the production floor and collect SPC and yield data, for instance, and write it down on a piece of paper, go back to an office and enter in a computer, which is not productive? Now we have real-time data collection and transmission to a central server and displayed on the dashboard, on your office desktop computer or even your smartphone. We have a comprehensive system to measure the bottom-line results from I4.0 Smart manufacturing.

**MB:** In the Zhangjian factory, is SMT assembly laid out in a straight line?

**JC:** We probably have best SMT production lines in the world in terms of speed and accuracy. We have multiple lines grouped together by process in order to maximize machine efficiency (FIGURE 6). We do not link the front-end machine to the backend machine dedicated through a conveyor belt, which is very old-fashioned and not so flexible because, very simply, if one of the machines in the chain goes down, the WIP will start piling up. The other machines upstream and downstream all go down. We focus very much on efficiency and machine utilization.



**FIGURE 4.** Parts are stored on reels inside intelligent storage systems in USI's component warehouses.



**FIGURE 5.** Among the data the AMHS Smart Storage dashboard shows are the number of reels, their size and how many parts they contain.

**MB:** I count at least eight placement machines in that configuration.

**JC:** Yes.

**MB:** That would be a single product being shipped through all those machines?

**JC:** Correct.

**MB:** And the line is running from left to right. How many printers would feed that configuration?

**JC:** One. The products we build are miniaturized. It's actually smaller than your fingernail.

**MB:** I'm surprised that one printer can keep up.

**JC:** It can. To maximize our productivity, we use a large-size PCB. Typically, we use a 95 by 240mm substrate. On the substrate, depending on the size of the product, we have anywhere from 100+ to 400 units. We just print at the PCB level instead of the unit level.

The smallest components we use in production are 01005 or 008004. It's very, very high density. Each module typically has 100 to 200 different components, or even more. The smallest module we make typically has 800+ components. It's very high density.

**MB:** You've referred in press releases to a parameter

management system.

**JC:** The first parameter management system we have implemented is the inline SPC. The SMT line in the photo has an inline SPC system in terms of the component placement accuracy. We measure, collect the data, and feed it to the SPC control module, so we know when the process is going to deviate. As you can imagine, we have hundreds and hundreds of vacuum cups on those pick-and-place machines. If any of the vacuum cups are worn out or the component is off, then we catch that because we have the fully integrated AOI machine there, so we know exactly which vacuum cup caused the problem. It's our first step we are implementing. Down the road, the parameter management system will allow the spec to fine-tune the machine parameters based on certain self-learning capabilities.

I'll give you another example. We have fully automated all the outgoing cosmetic inspection processes. We are very particular about any cosmetic defects, such as a very fine scratch or a tiny black dot that we could not see with our eyeballs. We have fully automated that. On the day-by-day fine-tuning of the parameters, we still have over-reject and under-reject rates. Our next step is to implement what I called the closed-loop machine-learning-based parameter management system. Based on the outcome of the over-reject and under-reject rates that came from the system, the machine is going to fine-tune the inspection parameters to narrow the defects.

**MB:** How long did it take to design and implement all of this?

**JC:** We started five years ago. One of my responsibilities is to lead the worldwide manufacturing effort. I do have a dedicated team to develop all the machine and data automation and help to implement those. It's been about five years.

**MB:** How close to the original schedule are you?

**JC:** We are very much on schedule. On average last year, the worldwide factories improved about a quarter star. Some factories made more progress, some less. It very much depends on

the business situation. Each factory is different. If the factory is booming, the manager is more willing to invest capex in automation. We are making progress very steadily toward our goal.

We take 4.0 Smart manufacturing very seriously. We invest a lot of resources and capex. We want to upgrade our manufacturing capabilities and improve our competitiveness. We are marching toward our final goal. We are on the way. □

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**FIGURE 6.** A single printer can feed eight SMT placement machines. USI says up to 400 highly dense SiP modules may be processed on a single substrate.

### *Material Gains, continued from pg. 16*

hybrid and all-electric propulsion. Airbus has been flying experimental platforms of various configurations since 2010 and, in 2015, successfully crossed the English Channel between France and England, with the E-Fan 1.0 all-electric single-seater. It's a tremendously significant route, recalling Louis Blériot's historic channel crossing of 1909. He completed the 24-mile journey less than six years after the Wright brothers achieved the first-ever powered flight, managing to stay airborne for less than one thousand feet.

Those early pioneers could hardly have imagined what was to come. And neither, I am sure, can we. □

### *HDP, continued from pg. 25*

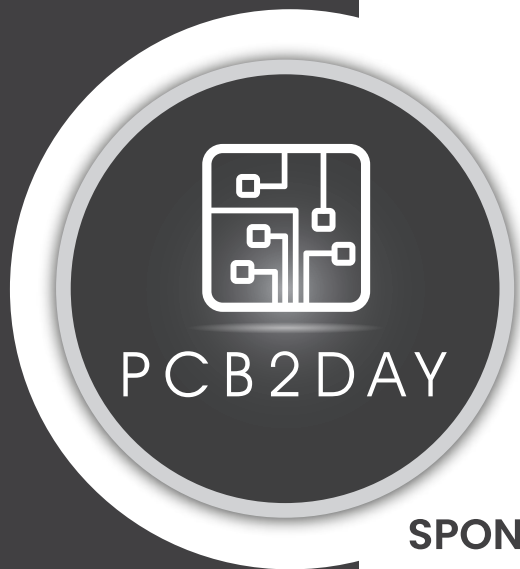
mechanical testing and will be analyzing the data prior to moving to the long-term aging phase.

Some of these projects directly affect the industry as a whole, not just the pursuit of higher technical knowledge for our members. For some of these problems, we are trying to determine if it affects the industry, not just HDP members. But HDP members always gain from this information.

**LM:** HDP is a member-driven organization, so we listen to what they want us to do. We have quite a few different projects going on right now. Some are proprietary, and some are open. More information about the projects is available here: <https://bit.ly/3qSnTuY> □

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# Optimizing Design for Manufacturability Analysis

A near real-time feedback loop between layout and assembly.

**TWO CORE TENETS** of Lean manufacturing philosophy are eliminating defect opportunities and minimizing process variation. Consequently, most companies embracing Lean principles do some form of design for manufacturability (DfM) analysis to identify manufacturability issues either during design or in the new product introduction phase. In some cases, this is an automated feature of design software. In other cases, this is done manually.

SigmaTron has adopted a hybrid process that uses software automation to speed basic analysis, followed by an engineering review. This E-DFM software tool reduces the time it takes to create a detailed report from several days to a few hours and works with SigmaTron's existing Valor software platform.

Automating the process improves efficiency, since the engineering team reviews the automatically generated reports and suggests solutions for accuracy instead of individually performing a full analysis themselves. They then can make suggestions to further optimize the recommendations, as needed. The tool has been customized from industry-standard PCBA design rules and SigmaTron's equipment/process-specific manufacturing guidelines, so it reflects equipment and process constraints.

The report output identifies the issue, explains the consequence if the issue is not corrected, displays a visual image of the issue, and suggests a solution. Its programming covers SMT and through-hole technologies.

SigmaTron has long flexed its engineering resources among facilities for better resource utilization and to take advantage of the expertise a core team may have developed based on the projects they've typically encountered. For example, test engineers in Chicago and China support SigmaTron's operations in Vietnam when test complexity exceeds the latter's capabilities. In this case, the engineering team in China supports enhanced DfM requests for all facilities.

Another benefit of this process is enhanced focus on common DfM mistakes and the ability to educate customer engineering teams on issues to avoid in layout. For example, the top three issues the engineering team saw in its third quarter 2020 analyses were:

- 90% of projects had issues with component packages not matched with recommended land patterns. When this issue isn't discovered early, it can result in project delays, particularly if long lead-time parts are involved. Attempting to work around this issue can cause defects and other issues such as:
  - Open circuits, if the pins fall outside the land pattern
  - Tombstoning, if the chip's package is smaller than its land pattern
  - Insertion problems, if the PTH pin diameter is larger than the holes
  - Inability to use a component when the wrong package is specified.

- 70% of projects had via-in-pad issues where exposed via-to-pad clearance was too small. This results in the solder paste being wicked into the via, creating an insufficient solder situation for the SMT component.
- 50% of projects had insufficient pad-to-pad spacing or circuit-to-circuit spacing. The exposed pad-to-pad spacing is too narrow for adequate separation of solder paste on each pad, resulting in solder bridging during reflow.

It is not unusual for OEM design teams to focus on product fit, form and function, without considering manufacturability. The E-DFM tool helps shorten the DfM feedback response time back to OEM engineering teams, so recommendations can be considered as early as possible in the design cycle.

The feedback is color-coded and prioritized by severity. The ranking scale is:

- Red – Critical: will affect reliability
- Brown – Hot: will increase cost or affect reliability
- Orange – Warm: impacts cost and creates process inefficiencies
- Light green – Cold: suggested as a future design improvement
- Dark green – Closed: violation has been closed.

The ranking scale helps teams better understand each violation in terms of its likely impact on product and quality, which can be important in situations with time or cost constraints associated with adopting DfM recommendations. It also helps create a path to improved manufacturability on future design iterations.

From a Lean perspective, eliminating defect opportunities and issues that create process inefficiency prior to production makes sense. From a practical perspective, resource constraints, short product development timelines and the cost of design approval processes can prevent DfM analysis from occurring or limit the recommendations that are subsequently adopted. Entirely automating the process may provide too generic an approach. It is the classic equation of a good versus a fast solution. Blending customized automation with an experienced engineering team enables a solution that is both good and fast, providing the level of documentation design teams need to evaluate the recommendations and the speed needed in short product development cycles. □

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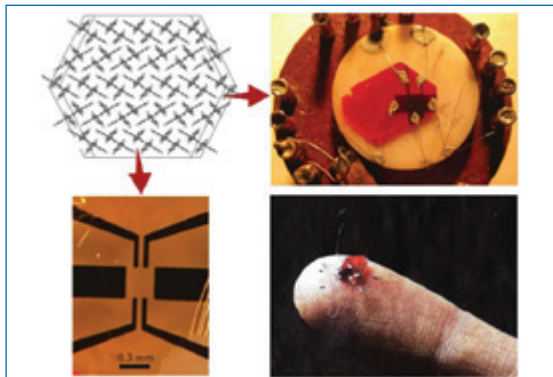


# State-of-the-Art Technology Flashes

Updates in silicon and electronics technology.

*Ed.:* This is a special feature courtesy of Binghamton University.

**Bending an organic semiconductor boosts electrical flow.** Organic transistors based on single crystals of rubrene can double the speed of electricity flowing through them when a crystal is slightly bent (strained). This behavior cannot be easily achieved with traditional semiconductors made of silicon. Rutgers University researchers found molecules of rubrene are arranged in a herringbone pattern (upper left in figure), forming highly ordered semiconducting molecular crystals that can be used to create rigid or flexible high-performance organic transistors, based on thick or ultra-thin single crystals, respectively. An example of a freestanding rubrene transistor is shown on a fingertip. This method could benefit next-generation electronics. (IEEC file #11946, *NASA Tech Briefs*, 10/1/20)



## Fluoride materials for extra-thin computer chips.

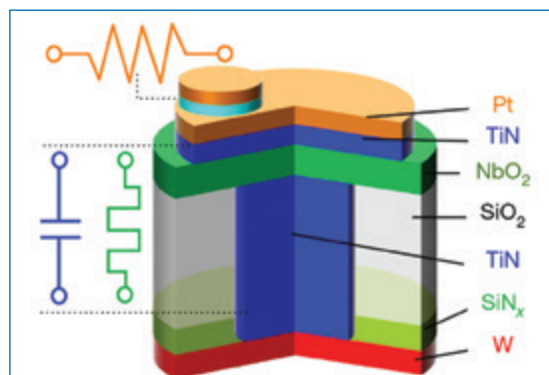
To make electronic components smaller, semiconductor two-dimensional (2-D) materials can be combined with new types of insulator materials. Smaller is the direction in which computer chips are moving. 2-D materials are considered to have great potential since they are as thin as a material can possibly be and, in extreme cases, only one single layer of atoms. This makes it possible to produce novel electronic components with tiny dimensions, high speed, and optimal efficiency. 2-D materials can only be used effectively if they can be combined with suitable material systems such as special insulating crystals. Researchers at the University of Vienna analyzed this problem and developed a transistor prototype with a calcium fluoride insulator. (IEEC file #11947, *NASA Tech Briefs*, 10/1/20)

## Optical polymer waveguide backplane for high-performance computers has zero bit-error count.

Optical communication technology can boost the speed of data transmission in many ways such as inter- and intra-datacenter and inter and intra-chip connections. An important part of this architecture is the computer backplane, which connects PCBs together to form a computer bus. Optical communication can greatly raise data transmission rates, helping to enable high-performance computers (HPCs). Researchers from Huazhong University have developed a high-speed, large-capacity, compact optical backplane based on optical polymer waveguides that use vertical-cavity surface-emitting lasers (VCSELs) emitting at 850nm for data transmission. The backplane network reaches 15Gb/s error-free data transmission via eight parallel channels; in the optical backplane, the 10 Gb/s in a channel is processed error-free by field-programmable gate-array chips. (IEEC file #11945, *Laser Focus World*, 10/13/20)

## Memristor breakthrough: First single device to act like a neuron.

Analog computing with neuron-like devices could efficiently solve problems traditional computers struggle with. One thing that's kept copying the brain's power efficiency is the lack of an electronic device that can act like a neuron. Hewlett Packard researchers have invented a device that meets those requirements. The most crucial part is the nanometers-thin niobium oxide ( $\text{NbO}_2$ ) layer that combines resistance, capacitance, and what's called a Mott memristor. It's predicted that if the possible device parameters were mapped, there would be regions of chaotic behavior between regions where behavior is stable. At the edge of some of these chaotic regions, devices can exist that do what the new artificial neuron does. (IEEC file #11950, *IEEE Spectrum*, 10/1/20)



## GARY MILLER

is technology analyst at IEEC, Binghamton University. He has over 40 years' experience in electronic packaging. He previously was the chief mechanical engineer at Lockheed Martin; gmiller@binghamton.edu.

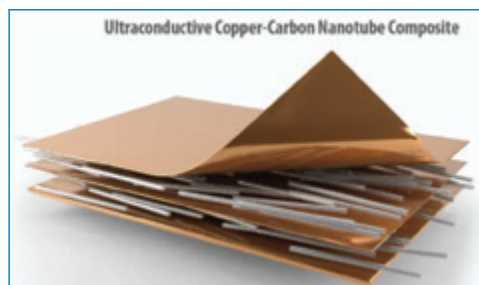
## INTEGRATED ELECTRONICS ENGINEERING CENTER (IEEC)

is a New York Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging. Its mission is to provide research into electronics packaging to enhance partners' products, improve reliability and understand why parts fail. More information is available at binghamton.edu/ieec.

**Carbon metal wires create path to carbon-based computers.** Transistors based on carbon rather than silicon could potentially boost computing speed and cut power consumption more than thousandfold. University of California researchers have created the last tool in the toolbox, a metallic wire made entirely of carbon, setting the stage for a ramp-up in research to build carbon-based transistors and computers. This has been one of the key things missing in an all-carbon-based integrated circuit architecture. The team has worked for several years to make semiconductors and insulators from graphene nanoribbons, a structure composed entirely of carbon atoms arranged in an interconnected hexagonal pattern resembling chicken wire. (IEEC file #11949, *Design Fax*, 10/20/20)

**Colorful perovskites: Thermochromic window technologies.** Department of Energy NREL researchers report a breakthrough in developing a next-generation thermochromic window that not only reduces the need for air conditioning but simultaneously generates electricity. The technology, termed “thermochromic photovoltaic,” permits the window to change color to block glare and reduce unwanted solar heating when the glass gets warm on a hot, sunny day. This color change also leads to the formation of a functioning solar cell that generates on-board power. Thermochromic photovoltaic windows can help buildings turn into energy generators, increasing their contribution to the broader energy grid’s needs. The newest breakthrough now enables myriad colors and a broader range of temperatures that drive the color switch. This increases design flexibility for improving energy efficiency, as well as control over building aesthetics that is highly desirable for both architects and end users. (IEEC file #1196, *Science Daily*, 10/20/20)

**New composite energizes the electric vehicle market.** A new composite from Oak Ridge National Laboratory increases the electrical current capacity of copper wires, providing a new material that can be scaled to improve energy-efficiency in electric vehicles. With an improved performance, manufacturers have the ability to reduce volume and increase the power density in advanced motor systems. The material can be deployed in any component that uses copper, including bus bars and smaller connectors for electric vehicle traction inverters, as well as for applications such as wireless and wired charging systems. To produce lighter weight and great conductive properties, the team created lengths of composite copper-carbon nanotube materials, then deposited and aligned carbon nanotubes on flat copper substrates. (IEEC file #11924, *NASA Tech Briefs*, 9/29/20)



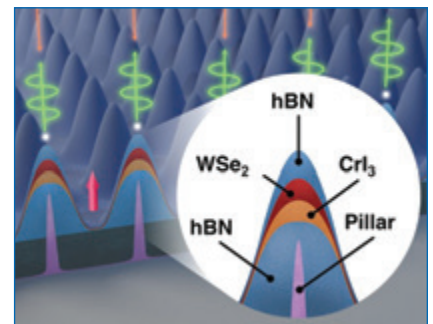
applications such as wireless and wired charging systems. To produce lighter weight and great conductive properties, the team created lengths of composite copper-carbon nanotube materials, then deposited and aligned carbon nanotubes on flat copper substrates. (IEEC file #11924, *NASA Tech Briefs*, 9/29/20)

**Solar-powered smart dust.** Industrial ubiquity of MEMS, increasing computing power of chips, the miniaturization of lab-on-a-chip devices, and increased connectivity, combined with the emergence of nanotechnologies, gave rise to the concept of *smart dust*, sub-millimeter-scale autonomous computing not larger than a grain of sand. An individual smart dust particle is a tiny sensor and computer, self-powered and wirelessly connected to a large network. Each particle can be left unattended and collects environmental data such as light, temperature, pressure, vibrations, the existence of toxins, etc. and transmits this data wirelessly. Smart dust can lead to autonomous artificial intelligent computation near the end-user, such as authentication, medical procedures, and healthcare monitoring, sensing, and tracking, industrial and supply chain monitoring, and defense applications. (IEEC file #11967, *Nanowerk*, 10/27/20)

**High-pressure glass processing could reduce fiber-optic signal loss by 50%.** Data transmission over optical fibers can be significantly improved by producing the silica ( $\text{SiO}_2$ ) glass fibers under high pressures, according to Penn State University researchers. They found that large voids form between silica atoms when the glass is heated and then cooled (quenched) under low pressure, but when this process occurs under 4 GPa, most of the large voids disappear, and the glass becomes a uniform lattice structure. Results show signal loss from silica glass fibers can be reduced by more than 50%, which could dramatically extend the distance data can be transmitted without the need for amplification. This would be a huge advance for the fiber-optic industry. (IEEC file #11968, *Laser Focus World*, 10/19/20)

**Light-driven quantum network promises faster, enhanced communication.** Using magnetic and semiconducting materials, researchers at the University of Rochester and

Cornell University designed a nanoscale node capable of using laser light to emit and accept photons to interact with other nodes. The development capitalizes on light’s physical properties to deliver a faster, increasingly efficient method to perform computations and detections. They arranged semiconductor and magnetic materials to form a platform that consisted of an array of pillars, each 120nm in height. The pillars mark the location of a distinct quantum state that can interact with photons and allow the photons to contact other locations across the device and with similarly constructed arrays at various locations. (IEEC file #11992, *Photonics Media*, 11/9/20)



**Flexible self-charging battery under development.** Strategic Elements is developing a self-charging battery technology through its collaboration with the University of New South Wales. The battery cells create electricity from humidity in the air or skin surface to self-charge themselves within minutes. No manual charging or wired power is required. Created with a printable ink, they are ideally suited for use in internet of things (IoT) devices. The battery ink is developed by integrating significant existing ink formulation and printed electronics intellectual property from the company's Nanocube Memory Ink technology with an advanced graphene oxide material. Strong potential competitive advantages exist over lithium-based batteries that suffer from weight, safety and the need for constant power supply to recharge. (IEEC file #11969, *Printed Electronics World*, 10/19/20)

**Bonding method attaches gallium nitride to thermally conductive materials.** Georgia Institute of Technology researchers have developed an easier way to attach wide bandgap materials such as gallium nitride (GaN) to thermally conducting materials such as diamond. This would boost the cooling effect on GaN devices and lead to better performance through higher power levels, improved reliability, and lower manufacturing costs. The technique could have applications for wireless transmitters, radars, and other high-power and high-frequency electronic devices. The technique, called surface-activated bonding, uses an ion source in a high-vacuum to clean the surfaces of the GaN and diamond; it also activates the surfaces by creating dangling bonds. Introducing small amounts of silicon into the ion beams lets the process create strong atomic bonds at room temperature, direct bonding the GaN and single-crystal diamond to make a high-electron-mobility transistor (HEMT). (IEEC file #12008, *Machine Design*, 3/25/20)

## Market Trends

**VCSEL market to grow to \$2.7 billion by 2025.** The VCSEL market is expected to be worth \$1 billion in 2020 and to show an 18.3% CAGR between 2020 and 2025 to reach \$2.7 billion. While 3-D applications for mobile and consumer are still booming, automotive, medical and AR/VR applications are emerging. Mobile 3-D sensing will represent around 75% of overall VCSEL revenues in 2020. In the VCSEL market, telecom and infrastructure applications, mainly datacom, are expected to reach \$516 million in 2025, a CAGR of 13.2%. Other applications are not significant yet but could emerge in the mid- to long-term, such as automotive applications like LiDAR or driver monitoring systems. (IEEC file #11941, *Electronics Weekly*, 10/12/20)

**Researchers develop graphene-based Covid-19 sensor.** Caltech researchers have designed a new sensor that can enable at-home diagnosis of Covid-19 infection. With the coronavirus disease a highly contagious disease transmissible even by people who do not display symptoms, subsequently responding to people infected with it is both challenging and time critical. Rapid testing kits cut down on the time needed to assess

whether someone carries the coronavirus, with or without symptoms. The team designed a multiplex testing method and incorporates a low-cost sensor that can diagnose Covid-19 in 10 minutes or less. (IEEC file #11937, *Science Times*, 10/2/20)

**Flexible electronics are the future in wearable health monitoring.** In a new research report, analysts find significant opportunities for flexible electronics to be applied to healthcare. They forecast the market for healthcare products containing flexible electronics to be worth over \$8.3 billion by the year 2030. A significant market trend is toward decentralized healthcare and utilizing technologies to monitor and care for people remotely. During the Covid-19 pandemic, healthcare systems around the world rapidly deployed remote care services in the form of telehealth. Such efforts often need to be supported by devices in the home capable of providing medical-grade data. But ultimately, monitoring efforts rely on the correct use of the devices. (IEEC file #1196, *Medical Design Briefs*, 10/2/20)

**LG's rollable OLED-R TV.** If you happen to live in South Korea and have \$87,000, LG has a rollable OLED TV for you. LG has been demonstrating its rollable display technology since 2014. At CES 2019, this technology was sufficiently mature for commercial launch. The LG Signature OLED R is the world's first rollable TV and will be made available at "several premium consumer electronics stores" located across South Korea. The 65" screen can be rolled up into its brushed aluminum casing. (IEEC file #11957, *PC Mag*, 10/20/20)



**Advanced packaging market to have steady growth of 8% to \$40 billion by 2026.** The advanced packaging market is set to grow from its current market value of \$25+ billion to over \$40 billion by 2026. Advanced packaging was developed to improve the performance of a device and simultaneously shrink the packages. It is termed as a general grouping of a variety of different techniques such as system-in-package, 3D-IC, 2.5D, and fan-out wafer-level packaging. Semiconductor packaging materials are known to be a class of electronic solutions utilized to form the connection of IC chip to the packaging substrate. The advanced packaging

market is bifurcated in terms of packaging type, application, and regional landscape. With respect to packaging type, the advanced packaging market is classified into 2.5D/3-D, fan-out, embedded-die, fan-in WLP and flip-chip. The fan-in WLP segment will witness considerable growth. (*IEEC file #11954, Semiconductor Digest, 10/9/20*)

**Implantable sensor could measure bodily functions and then safely biodegrade.** Penn State University researchers have designed a highly sensitive flexible gas sensor that can be implanted in the body and safely biodegrade into materials that are absorbed by the body. The flexible and implantable sensor monitors various forms of nitric oxide (NO) and nitrogen dioxide (NO<sub>2</sub>) gas in the body. The team added a twist to their sensor design by making it from materials that are not just implantable, flexible and stretchable, but also biodegradable. The researchers say future work could look at designing integrated systems that could monitor other bodily functions for healthy aging and various disease applications. (*IEEC file #12000, Science Daily, 11/10/20*)

## Recent Patents

**Liquid cooling through conductive interconnect (assignee: Intel Corp.) pub. no. 16/379619.** Embodiments include semiconductor packages and cooling semiconductor packaging systems. A semiconductor package includes a second die on a package substrate, first dies on the second die, conductive bumps between the first dies and the second die, a cold plate and a manifold over the first dies, second die, and package substrate, and first openings in the manifold. The first openings are fluidly coupled through the conductive bumps. The semiconductor package may include a first fluid path through the first openings of the manifold, where a first fluid flows through the first fluid path.

**Flexible printed circuit to mitigate cracking at through-holes (assignee: CommScope) patent no. 10,798,819.** Flexible fingers for flexible printed circuits improve the crack resistance of prior art designs. The crack resistance can be improved by encapsulating the trace inside additional layers such that the outer two layers include only the lands of the through-hole, and all other copper is etched away. The crack resistance can also be improved by strategically adding copper on layers other than the trace layer, including attaching it to the land of the through-hole as a stub. These two designs can be combined to include a stub trace into a four-layered design.

**Method for 3-D integrated wiring structure and semiconductor structure (assignee: Yangtze Memory Tech.) pub. no. US10796993.** Embodiments of methods and structures for forming a 3-D integrated wiring structure are disclosed. The method can include forming an insulating layer on a front side of a first substrate; forming a semiconductor layer on a front side of the insulating layer; patterning the semiconductor layer to expose at least a portion of a surface of the insulating layer; forming a plurality of semiconductor structures over the front side of the first substrate, wherein the semiconductor

structures include a plurality of conductive contacts and a first conductive layer; joining a second substrate with the semiconductor structures; performing a thinning process on a backside of the first substrate to expose the insulating layer and one end of the plurality of conductive contacts.

**Active package substrate having anisotropic conductive layer (assignee: Intel Corp.) patent no. 10,790,257.** Semiconductor packages, including active package substrates, are described. In an example, the active package substrate includes an active die between a top substrate layer and a bottom substrate layer. The top substrate layer may include a via, and the active die may include a die pad. An anisotropic conductive layer may be disposed between the via and the die pad to conduct electrical current unidirectionally between the via and the die pad. In an embodiment, the active die is a flash memory controller, and a memory die is mounted on the top substrate layer and placed in electrical communication with the flash memory controller through the anisotropic conductive layer. □

## Encrypted Opinions

What's more in need of rehabilitation? The bonepile, or supplier gateway?

*HELLO, I WOULD like to get some information about your capabilities for Bonepile Rehabilitation. I have some legacy circuit cards that were previously tested on a FACTRON 750. Can you reverse engineer the schematics/gerbers from a known good board? Once you have diagnosis (sic) the problem on a failed board, can you also perform the repair? Are you cybersecurity certified for ITAR data?*

This is how an unsolicited customer engagement often begins. No unusual requirements here, other than the obvious need for remedial grammar lessons.

“Yes, yes and yes.”

*Good. Then you may be able to assist us. What is your process?*

Bonepile rehabilitation and reverse engineering in our world are two different things. When we say bonepile rehabilitation, we are usually talking about troubleshooting boards that have failed, either in the field or in functional/system test, and using the tools we have here at our facility to troubleshoot, repair, and restore them to service. In most cases design documentation (bill of materials, CAD, schematic, Gerber files, etc.) still exist, and are used in this activity, especially to develop test programs (flying probe, JTAG/boundary scan, etc.).

I would classify what you are asking for more as reverse engineering, in that (I assume) documentation and data are mostly or completely gone, due to time, business transitions, or recordkeeping ineptitude. Full restoration of a doc set, compared with bonepile rehabilitation, is a more difficult, time-consuming, and, by nature, expensive task. It typically involves various forms of flying probe testing, CT scanning of individual layers, followed by re-layout and redesign using the forensic data our tools provide. If copy exact methods are required, the process will not work. Time and faded memory demand some latitude of interpretation. Projects like these usually start at about \$10,000 per part number (very simple part numbers), and go up from there, frequently way up. If it is a bargain you seek, you're in the wrong place.

To give you a definitive answer whether we can help you with a particular board, I would need to see it. Ideally, I'd need to see one assembled board and one bare board at a minimum.

That is our process.

We are ITAR registered and AS9100 certified. Matter of fact, we just had our AS9100D transition audit two weeks ago. Regarding data security, I'm assuming you are asking whether we meet NIST 800-171 and related DFARs. Today we do not, but we have

developed a roadmap toward meeting the NIST standard, which we would be happy to share if a project goes forward.

Meanwhile, if you would like to proceed further, send me an NDA and I'll review and sign it immediately. Then we can discuss in depth the particulars of your project.

Any questions? Does this sound like a plan? When can we get started? Tomorrow? Next week?

*We're interested. You'll be hearing next from our security and purchasing groups, the first to establish your bona fides, the second to install you in our ERP system as a vendor. This is urgent.*

That was September. Our next communication arrived in February. Urgent indeed.

*Greetings Robert: Our company wishes to discuss and potentially engage in the process of CCA rehabilitation with your company, and to further pursue and release details I am enclosing our Standard Bilateral NDA for your review and execution. How many weeks will it take your legal department to review and amend and sign this document?*

“About 10 minutes.”

*Seriously? How can you do that so fast and without the assistance of legal counsel?*

“I see one to two of them every week. That's 50 to 100 per year. I know what to look for and what the pinch points are. The review takes no time at all if you know what you're looking for. It's in the attorneys' best interest that you remain ignorant of that. Anyway, I should have a signed, scanned copy of your NDA ready for countersigning back to you within the hour.”

*Good. Once the NDA is received, you will receive an invitation to become a vendor from our ERP system. You will also receive a security notification asking that you authenticate yourself and your company.*

Sure enough, next day comes the email prompt.

You have been invited by a Member of our Supplier System to join their select supply network. You were nominated by a Customer Buyer. Please supply your Federal Tax ID Number; your DUNNS number; your CAGE Code; a copy of your DDTC (ITAR) letters and your ISO9001/AS9100 certifications for review.

Invited? Nominated?

Or condemned?

*In order to transact with a Supplier System Customer, you must complete all of the actions indicated below. All potential/pending purchase orders will be held pending completion of the vendor profile and two-factor authentication registration. Failure to complete all of these listed actions, in the sequence*

**ROBERT BOGUSKI** is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.



described below, will result in immediate rejection of this application with no appeal.

In plain English, don't screw it up.

1. Register with our Supplier System (SS), which provides supplier profile and user identity management services for Our Company Pay to Play (P2P) transaction system via the Monitored Access Gateway Arrangement or MAGA. A link has been provided in a downloadable document for you to initiate the registration process. You will need to set up a login and password with the Download Advanced Management Node, or DAMN, in order to retrieve this document.

If you have trouble accessing either URL, an alternate URL is available by contacting our Help Desk. In every case described above, in order to access each site, you will first be prompted to accept Our Company's 180-day payment terms. If you do not select "accept," you will be jettisoned from the system and this transaction will cease immediately with no right of appeal.

In all transactions, please reference the 37 character transaction codes and confirmation codes provided in the downloadable document retrieved from DAMN. For security reasons, the system will not respond without prior insertion of these codes, twice.

To assist you with the Supplier System (SS) vendor registration process, the following help documents are available: (1) SS Vendor Registration Checklist (SSVRC) and (2) SS Vendor Registration User Guide (SSVRUG). Both are accessible through the DAMN Portal, once you have established an account and accepted our payment terms. Please use a high-speed internet connection, as each document exceeds 350 pages and contains both PowerPoint and video content.

2. In order to securely access Our Company's Pay to Play (P2P) and Supplier Systems (SS), it is required to either purchase or be in possession of an approved 2-Factor Authentication credential. For more information on the process and recommended/approved credentials, please see the Supplier System Pay to Play (P2P) 2-Factor Authentication Support Site located on Our Company's Website. You will need to produce a scanned copy of a federally approved and authorized Real ID and a birth certificate (notarized) in order to be granted access to the P2P section of the website. Please note that UPS Store notarizations are invalid for this purpose. Bank notarizations with gold certificate stamp are preferred.

Additional Instructions (if any):

If you have any questions regarding this request or need assistance with completing these actions, please contact SS Customer Service.

The SS Customer Service team is available online via the SS Customer Support Self-Help site. The Self-Help site

is also accessible via the P2P section of the website. The same access credentials noted above apply, with the addition of a signed, notarized letter on company letterhead authorizing access to SS Customer Support, and stating the precise reasons for seeking support. Allow 10-15 working days for replies to letters seeking customer support. Your SS Customer Service Team sincerely believes we are the final solution to procurement security, and we truly appreciate your endurance.

So this is what Hell feels like.

In all the foregoing excitement, I'm also forgetting what it is they want from us in the first place.

One month later:

Rodger, how are you coming with the SS setup process?

"I'm not. I tried three times, and it kicked me out after the third failed attempt in 45 days, saying I lacked correct or sufficient login credentials. Also, between the time of my first attempt and my last, the two-factor authentication requirement has inflated to a **three-factor** requirement. And we've changed presidents and gone from English to metric. Because I made three failed attempts in 45 days, I cannot make another try at registration for 90 business days. Two of my associates then took over for me and made the same attempt, and were similarly, and regrettably, ejected. Oh, and it's Robert."

Right. This is extremely hot. We need to reverse-engineer these boards and have new archives within the next 24 months. Otherwise things that fly won't. Federal dollars are riding on this and need to be spent. It's an urgent national security issue.

"Your Supplier Portal is a national security issue too. As in, nobody with room-temperature IQ, much less the Russians, can access it and do business with you. Congratulations."

We've seen that comment before in a few supplier surveys. Have you done one of ours? We use SurveyMonkey. Cool stuff.

"Then I guess you have a cost/benefit calculation to make. Do you need our services, or don't you? If the latter, we're done. If the former, what's it worth to you to set us up? Your call."

I have emergency authorization to bypass the system and set you up on a 30-day provisional basis. Give me a login first and password second that you want to use. In both please use at least 8 characters and also be sure they are a combination of numbers, letters (both lower case and caps) and symbols. Do not use roman numerals as they are symbols of a failed empire. Our system doesn't like that.

"L!v!d!666. I!0@TH3pw\$!!!!!"

Much obliged. Give me 5 minutes and you'll be all set. Look for the DocuSign prompt on your email with 10 pages of government disclaimers and 12 signature lines. Please sign and return immediately so we can send downloadable data to you to quote.

I'm always here to help our vendors. We are all about making it easy for them to do business with us. Have a blessed day! Warm regards, Frederick Kafka. □

# Resolving Intermittent Area Array Packages with Video Simulation

Excessive temperature or moisture may be to blame.

**OPEN CONNECTIONS ON** area array packages can be difficult to spot, particularly if they are intermittent electrical failures like the examples in **FIGURE 1**. One or more open joints can occur between the package and solder sphere or at the PCB pad interface. Reflow soldering with either convection or vapor phase can cause packages to move and separate. This can be caused by warping of the package or in some cases

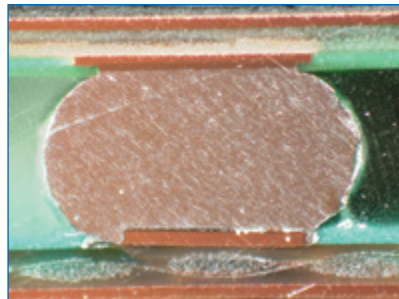
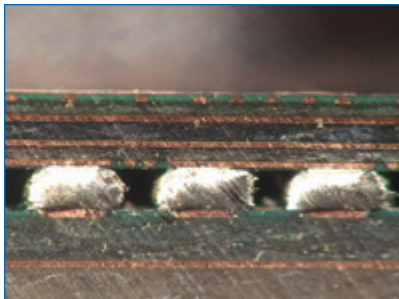
minor popcorning due to moisture. Both faults can be simulated and recorded with video for reference.

Secondary reflow of solder joints can cause intermittent connections of packages. This occurs when adjacent packages are reworked or when the board passes through wave or selective soldering under excessive soldering temperature. Using video simulation in the process can be helpful to solve process defects. In such instances, while

soldering boards, the operator is also observing reflow optically or with x-ray. See <https://bit.ly/3mZsSYw> for an example.

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at [youtube.com/user/mrbobwillis](https://www.youtube.com/user/mrbobwillis). □

**BOB WILLIS** is a process engineering consultant; bob@bobwillis.co.uk. His column appears monthly.



**FIGURE 1.** Opens on a BGA package.

*Chiplets, continued from pg. 23*

ation of bump assignment and the RDL routability of the assigned nets.

In package prototype design, the chiplet design data can be placed directly as a component with no need for spreadsheet communication. Creating a connection between chiplets when placing these components is also possible. This facilitated a scalable multi-die integration, escape routing from bumps, die-to-die, and die-to-ball routing via autoroute functions, all within a short turnaround time within the prototype design.

The SiP was then similarly merged with the prototype PCB for validation and viability evaluation. After implementing critical signal physical data, the electrical characteristics and power integrity were checked during the prototype with embedded simulators.

**Favorable results.** Two tiled test cases were created with different depths from the chip edge of the tile bumps cells while considering the routability of the SiP and its power constraints. One iteration had three columns and four rows of bumps.

Another had four columns and three rows of bumps. Also, two different floor plans with different tile arrangement methods were created for evaluation.

Two test cases of the SiP prototype designs for the chiplets were created (**FIGURE 3**). Since the design was performed on a common platform, elements were confirmed on the SiP while feeding changes to the chiplet as needed, allowing the user to turn around various configuration changes quickly. Each of these sample iterations took approximately 30 min. to create.

Potential performance of the prototype design was judged using some factors such as trace length and latency:

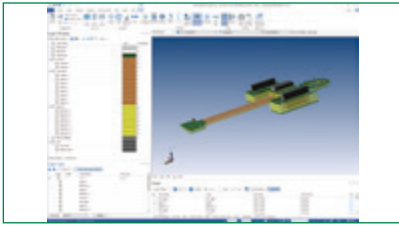
- In case two, the bump depth was reduced to shorten the escape route length.
- The route length between chiplets was more closely matched.
- Compared to case one, case two confirmed that the critical signal length variation of 20 signals was reduced by 90% or more.
- The total routing length was reduced by 25%.

- The interface signals between the chips were selected, topology extracted, and signal integrity analysis performed.
- Signal latency was confirmed by its better physical implementation as improved in case two.
- More desirable electrical characteristics could quickly be determined during this prototype design phase.

Electronic designers have a newfound capability to rapidly generate feasibility studies and obtain visibility into the performance of different configurations. Signal integrity and power integrity may be evaluated quickly, with their interfaces in place to assess designs at a more granular level using the simulation tool of choice.

In one platform, we can now simultaneously examine configuration and tradeoffs with visibility into the entire SiP, to allow intelligent and expeditious decision-making. This ensures that targets for cost and performance are met while adhering to the design schedule. □

**STEVE WATT** is manager of engineering operations, SOZO Center at Zuken USA ([zukenusa.com](https://www.zukenusa.com)); [steve.watt@zukenusa.com](mailto:steve.watt@zukenusa.com).



### DOWNSTREAM CAM350/DFMSTREAM V. 14.5

CAM350/DFMStream v. 14.5 now supports importation and visualization of CAD designs containing flex, rigid-flex and embedded component data in both 2-D and 3-D views. Imports and visualizes flex/rigid-flex data created by PCB CAD tools in 2-D and 3-D view ports, as well as documenting rigid/rigid-flex stack-ups; can share documentation with fabricators. Features include import/export ODB++ and IPC-2581 modification; import/export modification to support PCB core material data; stack-up visualizer modification; 3-D view port modification; area tool modification; DfM analysis modification; parametric solder and paste mask generation; assembly panel creation.

DownStream Technologies

[downstreamtech.com](http://downstreamtech.com)



### ORBOTECH APEIRON

Apeiron performs UV laser drilling on flexible printed circuits in a roll-to-roll manufacturing configuration. Multi-path technology with two laser beams and four large-scan-area drilling heads can drill in four locations simultaneously. Internal roll-to-roll using roll-inside technology. Provides built-in beam validation tools for size, roundness and energy distribution with continuous beam uniformity technology. Offers roll-to-roll and sheet-by-sheet handling of thin flex cores with capacity to drill two panel sheets side by side. Optional roll widths of 260mm and up to 520mm. Minimum via size is 20 µm. Footprint is 5 sq. m.

Orbotech

[orbotech.com](http://orbotech.com)



### INNOLAS LINEXO

Linexo laser processing workstation is for R&D and smaller substrate production, e.g., ceramic PCBs. Features fixed optic or scanner setup, single- or dual-process heads, process gas (N<sub>2</sub>, O<sub>2</sub>, Ar, etc.). Can process one or more substrates in parallel. Other features include automatic camera calibration, automated routines for reference runs, automated process control, and automated vision system for precision alignment and scaling, offset, trapezoidal and rotation compensation. Comes as standalone or integrated in production line.

Innolas Solutions

[innolas-solutions.com](http://innolas-solutions.com)

## OTHERS OF NOTE

### MACDERMID HELIOFAB AG 7921

HelioFab AG 7921 silver electroplating process for leadframe-based LED packages is said to consistently deposit highly reflective silver with measured GAM values around 2.0 over a current density window of 10 to 70ASD. Bath produces a stable deposit over the standard 100 AH/L industry bath life metric. Deposit passes all standard testing for LED performance such as 1,000-hr. luminous decay, as well as assembly functional testing for gold wire bond pull and die attach shear strength.

MacDermid Alpha Electronics

[macdermidalpha.com](http://macdermidalpha.com)

### DOWNSTREAM BLUEPRINT-PCB V. 6

BluePrint-PCB v. 6 has a 2-D/3-D environment for improved PCB post-processing. Is designed to automate, streamline and improve PCB documentation. Common database among all DownStream products allows easy file-sharing and transitions. New user interface for continuity.

DownStream Technologies

[downstreamtech.com](http://downstreamtech.com)

### EASYLOGIX PCB-INVESTIGATOR V. 12

PCB-Investigator v. 12 CAD/CAM includes new plugin for DfT preparation. Defines test probes for fixture and fixtureless devices using different rules and can be exported for Seica, Takaya and HP3070 machines. Extended design report: more images, analyze results, and intelligent linking. Fully supports Gerber X2.

EasyLogix

[pcb-investigator.com/en](http://pcb-investigator.com/en)

### VISHAY VEMD4010X01, VEMD4110X01

VEMD4010X01 and VEMD4110X01 surface-mount automotive-grade silicon PIN photodiodes come in 0805 case size with 0.7mm profile. Offered in black packages, opaque side walls eliminate side illumination to increase signal-to-noise ratio. Are RoHS-compliant, halogen-free, and MSL 3.

Vishay

[vishay.com](http://vishay.com)

### NUMBER ONE SYSTEMS EASY-PC V. 24

Easy-PC v. 24 ECAD has more than 50 new enhancements. Delivers performance in schematic capture and PCB layout and is simple to learn. Enables control of thermal spokes on individual pads or pad styles; pads on same net can be allocated to different thermal spokes depending on size. Shows net details.

Number One Systems

[numberone.com](http://numberone.com)

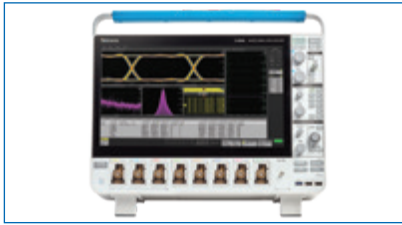
### HIROSE CX90MW CONNECTOR

CX90MW waterproof USB 3.2 Gen 1 Type-C connector is for applications that require miniaturization with resistance to liquid, vibration and/or shock. Mounting area reportedly 22% smaller than other receptacles. Is rated to IPX8. Includes front sealing gasket that prevents water penetration into shell, while potting prevents water intrusion into interior. Supports data rates up to 5Gbps.

Hirose

[hirose.com/us](http://hirose.com/us)

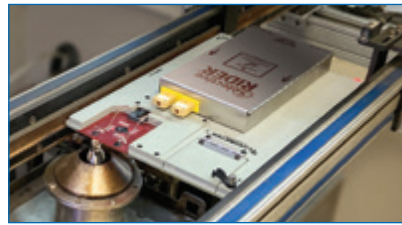




### TEKTRONIX 6 SERIES B

6 series B mixed signal oscilloscope extends performance to 10GHz and 50GS/sec. Offers signal fidelity with 12-bit ADCs and low noise, 10GHz bandwidth and up to 8 FlexChannel inputs. Contributes less than 51.1µV of noise at 1mV/div and 1GHz and less than 1.39mV of noise at 50 mV/div and 10GHz. Bandwidth is more than 2GHz with 4, 6 or 8 channels. Built-in digital down converters behind every channel enable multi-channel spectrum analysis.

Tektronix  
tektronix.com



### ECD SELECTIVERIDER

SelectiveRider soldering process measurement pallet performs automated verification for wave, reflow and selective processes. Validates three phases of selective soldering: fluxing, pre-heating and soldering. Verifies flux location and accuracy; confirms dispense X/Y positional precision; IDs blocked or unprimed spray heads; verifies dot size, and more.

ECD  
ecd.com



### ESPEC AR SERIES

Four new models of AR series environmental stress chambers are capable of precise control over a temp. range of -70° to +180°C (with optional support for up to 200°C) and a humidity range of 10% to 98%RH. Air temp. can be raised or lowered at rate of 10°C per min. or 15°C per min. during testing between -40° and +125°C. with or without humidity control. Comply with IEC international standards and LV 124. Stable control possible for 95°C/98%RH and other high-temp., high-humidity tests.

Espec  
espec.com

## OTHERS OF NOTE

### MASTER BOND EP42HT-4AOMED BLACK

EP42HT-4AOMed Black two-part epoxy created for medical device manufacturing is biocompatible and non-cytotoxic, passing USP Class VI and ISO 10993-5 certifications. Withstands aggressive chemical sterilants, radiation and repeated cycles of autoclaving. Offers cryogenic serviceability and heat resistance with service temp. range from 4K to 400°F. Room temp. curable.

Master Bond  
masterbond.com

### DELO DUALBOND GE4918

Dualbond GE4918 light- and humidity-curing sealant for connectors for vehicle control units or sensors. Reportedly offers pin sealing properties, increases connector life and permits efficient production. Adheres to mercaptan coating and connector housing materials PA and PBT. Temp. resistance up to +150°C.

Delo  
delo-adhesives.com

### ELECTROLUBE ER6006, ER7006

ER6006 and ER7006 Bio epoxy resins provide good flow characteristics for potting of difficult and complex geometries. ER6006 is two-part high thermally conductive epoxy encapsulation resin primarily developed for encapsulation of LED driver units. Offers high chemical resistance and protection in a range of environments. Cures in 1 hr. at 100°C, 3 hr. at 60°C or 24 hr. at room temp.

Electrolube  
electrolube.in

### THERMO FISHER AXIA CHEMISEM

Axia ChemiSEM scanning electron microscope includes always-on EDS analysis. New auto-alignment and auto-focus technology lowers need for training. Chamber and stage design aids in investigation of samples of all shapes and sizes, including samples up to 10kg. Offers instant quantitative elemental information without additional setup or switching between UIs. Large, flexible chamber accommodates samples traditionally considered too heavy for investigations involving electron microscopy.

Thermo Fisher Scientific  
thermofisher.com

### HUMISEAL VIVID CURE UV6041, UV7041

Vivid Cure UV6041 and UV7041 liquid, optically clear adhesives (LOCA) provide enhanced optical properties and improved durability of optical devices and displays. Are formulated for wireless communications, automotive displays, medical devices, and aerospace and avionic controls. Properties include low shrinkage, superior and variable light transmission properties, resistance to discoloration, and resistance to both thermal and mechanical damage. Cured to final properties using UVA or visible light. 100% VOC-free.

Humiseal  
chasecorp.com/humiseal

### SHENMAO SMEF-Z3 FLUX

SMEF-Z3 joint-enhanced flux is designed for fine-pitch assembly and LED die attach. Is compatible with solder paste. Can be applied after solder paste printing and cured simultaneously during reflow process. Can be used for pin-transfer and stencil printing processes.

Shenmao  
shenmao.com

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## In Case You Missed It

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“Fully Light-Controlled Memory and Neuromorphic Computation in Layered Black Phosphorus”

*Authors:* Taimur Ahmed, *et al.*

*Abstract:* Imprinting vision as memory is a core attribute of human cognitive learning. Fundamental to artificial intelligence systems are bioinspired neuromorphic vision components for the visible and invisible segments of the electromagnetic spectrum. Realization of a single imaging unit with a combination of in-built memory and signal processing capability is imperative to deploy efficient brain-like vision systems. However, the lack of a platform that can be fully controlled by light without the need to apply alternating polarity electric signals has hampered this technological advance. Here, a neuromorphic imaging element based on a fully light-modulated 2-D semiconductor in a simple reconfigurable phototransistor structure is presented. This standalone device exhibits inherent characteristics that enable neuromorphic image pre-processing and recognition. Fundamentally, the unique photo response induced by oxidation-related defects in 2-D black phosphorus (BP) is exploited to achieve visual memory, wavelength-selective multibit programming, and erasing functions, which allow in-pixel image pre-processing. Furthermore, all optically-driven neuromorphic computation is demonstrated by machine learning to classify numbers and recognize images with an accuracy of over 90%. The devices provide a promising approach toward neurorobotics, human-machine interaction technologies, and scalable bionic systems with visual data storage/buffering and processing. (*Advanced Materials*, November 2020, <https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.202004207>)

### Solder Alloys

“Experimental and Theoretical Studies of Cu-Sn Intermetallic Phase Growth During High-Temperature Storage of Eutectic SnAg Interconnects”

*Author:* A. Morozov, A. B. Freidin, *et al.*

*Abstract:* The growth of intermetallic compound (IMC) layers is considered. After soldering, an IMC layer appears and establishes a mechanical contact between eutectic tin-silver solder bumps and Cu interconnects in microelectronic components. Intermetallics are relatively brittle in comparison with copper and tin. In addition, IMC formation is typically based on multi-component diffusion, which may include vacancy migration leading to Kirkendall voiding. Consequently, the rate of IMC growth has a strong implication on solder joint reliability. Experiments show the intermetallic layers grow considerably when the struc-

ture is exposed to heat. Mechanical stresses may also affect intermetallic growth behavior. These stresses arise not only from external loadings but also from thermal mismatch of the materials constituting the joint, and from the mismatch produced by the change in shape and volume due to the chemical reactions of IMC formation. This explains why in this paper special attention is paid to the influence of stresses on the kinetics of the IMC growth. The authors have developed an approach that couples mechanics with the chemical reactions leading to the formation of IMC, based on the thermodynamically sound concept of the chemical affinity tensor, which was recently used in general statements and solutions of mechanochemistry problems. The authors start with a report of experimental findings regarding the IMC growth at the interface between copper pads and tin-based solder alloys in different microchips during a high-temperature storage test. Then the growth kinetics are analyzed by means of a continuum model. By combining experiment, theory, and a comparison of experimental data and theoretical predictions, the authors finally find the values of the diffusion coefficient and an estimate for the chemical reaction constant. A comparison with literature data is also performed. (*Journal of Electronic Materials*, September 2020, <https://link.springer.com/article/10.1007/s11664-020-08433-y>)

### Thermistors

“Inkjet Printing of Perovskites for Breaking Performance-Temperature Tradeoffs in Fabric-Based Thermistors”

*Authors:* Shujie Li, Alex Kosek, Mohammad Naim Jahangir, Rajiv Malhotra and Chih-Hung Chang.

*Abstract:* A novel low-temperature route is developed for inkjet printing of the perovskite  $\text{Cs}_2\text{SnI}_6$  to create wearable negative-temperature-coefficient thermistors with unprecedented performance on thermally sensitive fabrics. A low processing temperature of 120°C is achieved by creating a stable and printable ink using binary metal iodide salts, which is thermally transformed into dense  $\text{Cs}_2\text{SnI}_6$  crystals after printing. The optimally printed  $\text{Cs}_2\text{SnI}_6$  shows a temperature measurement range up to 120°C, high sensitivity (4400K), temperature coefficient of resistivity ( $0.05^\circ\text{C}^{-1}$ ), and stability under ambient environmental conditions and bending. The approach breaks a critical tradeoff that has hindered wearable fabric-based thermistors by enabling damage-free fabrication of devices with commercially comparable performance, evincing significant applications in multifunctional textiles and beyond. (*Advanced Functional Materials*, September 2020, <https://onlinelibrary.wiley.com/doi/10.1002/adfm.202006273>)

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

The logo for PCB WEST 2021 features the letters 'PCB' in white on a purple square background with three white dots below it. To the right, 'WEST 2021' is written in white. Below the main title, 'Conference & Exhibition' is written in a smaller white font.

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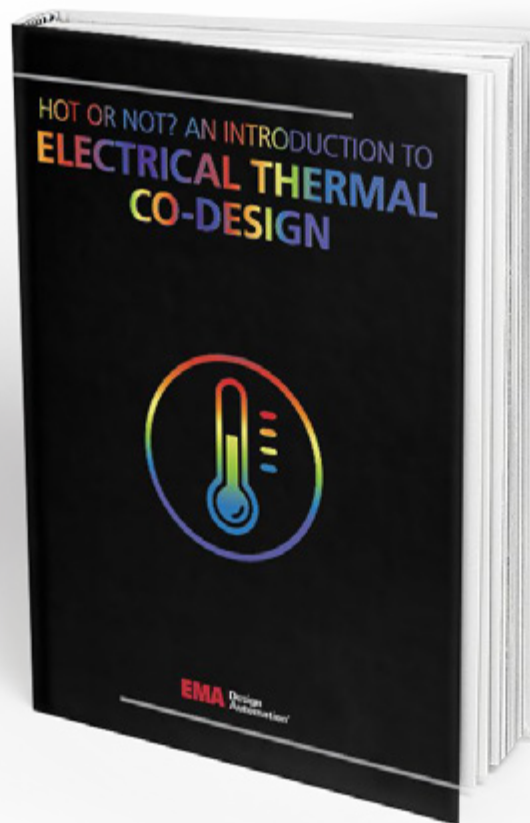
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